An approach to produce a stack of photo definable polyimide based flat UTCPs

[1]S. Priyabadini, [1]T. Sterken, [1]L. Wang, [1]K. Dhaenens, [1]B. Vandecasteele, [1]S. Van Put, [2]A.E. Petersen, [1]J. Vanfleteren
[1]CMST (Affiliated with IMEC and Universiteit Gent), Technologiepark 914a, B-9052 Gent, Belgium
[2]Oticon A/S, Kongebakken 9, DK-2765, Smørum, Denmark
Tel: 0032- 92645355, Fax: 0032- 92645374, Email: swarnakamal.priyabadini@elis.ugent.be

Abstract

Getting output of multiple chips within the volume of a single chip is the driving force behind development of this novel 3D integration technology which has a broad range of industrial and medical electronic applications. This can be achieved by laminating multiple layers of spin-on polyimide based ultrathin chip packages (UTCPs) with fine pitch through hole interconnects.

Introduction:

In the framework of the European Project TIPS, this 3D stacking of UTCP process was developed to provide another way to fabricate devices with miniaturized package volume. An overview of this concept was reported previously by Priyabadini et al. [1]. This process having a very low production yield (7%) was based on conventional UTCPs which is a chip embedding technology within two spin-on non-photo definable polyimide layers [2]. The result of failure analysis confirms that die cracking within the stacks is the main reason for this huge loss in yield. Die cracking can be introduced due to non-uniform pressure distribution on the overall surface of multiple non-flat packages during lamination process. To eliminate this process induced risk and achieve faster production rate with high yield, IMEC has developed a photo definable polyimide based flat UTCP concept.

In this work, the ICs are thinned down to ~20 µm and embedded within 3 layers of spin-on photo definable polyimide thin film by using BCB as adhesive glue for chip bonding on the PI substrate, to produce ~60µm thick flexible sheet of flat UTCPs. In order to reduce the costs and achieve a faster production rate, many chips are placed precisely on the 1st polyimide layer. Backside illumination of the central polyimide (flattening layer) enables producing self-aligned cavities for the chips. The vias on the contact pads of all the chips are opened on the top polyimide layer by a single photolithography step. Contact to the external world is made by a fan-out metallization on the package which is achieved by deposition and patterning of an 8µm thick copper layer. The yield per substrate can be verified before releasing the sheet of UTCPs from the carrier which solves Known-Good-Die issues. Four of these sheets with two additional flexes on top and bottom are stacked together with 25 µm thick adhesive films in-between. All of the layers are placed precisely within a dedicated lamination tool for bonding by vacuum lamination technology. The interconnection to each of the embedded packages is made by laser drilling through hole vias on the external contact pads, followed by metallizing them by electroless-galvanic Cu deposition and patterning them using lithography. This results in the production of a ~400 µm thick stacked module with 4 dies embedded inside.

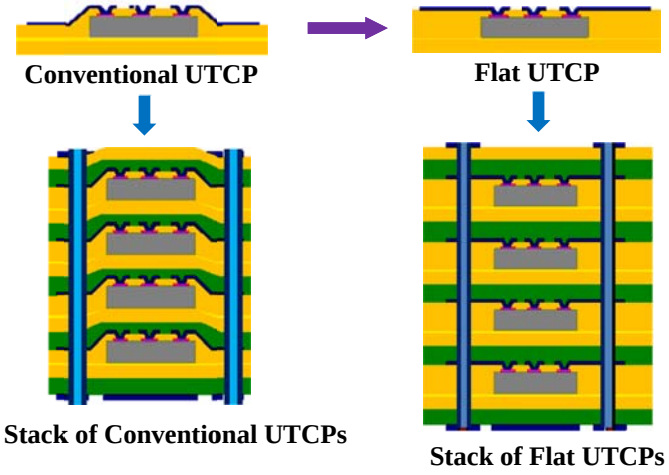


Figure 1. Schematic overview of stacking of flat UTCP approach

Stacking of Conventional UTCPs:

The 1st batch of stacked UTCPs produced by using this process (Fig. 1, left) showed very low production yield which was reported by Priyabadini et al. [1]. Failure analysis proves that die cracking during the lamination process can be the reason behind such a massive loss of yield. As the UTCP itself has an in-built risk of non-uniform package thickness due to chip height, when pressure is applied at the adhesive flow stage during the lamination process, the liquefied glue on the top of chip package squeezes out from the chip area leaving a very thin layer on the top of the chip (Fig. 2). This results in a non-uniform pressure distribution on the overall surface of the embedded packages during lamination process which could be a reason for chip cracking.

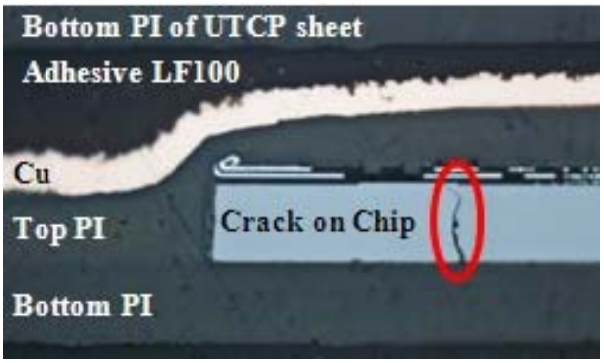


Figure 2. Thin die cracking found during failure analysis of the stacks of chip packages

To overcome this problem of pressure non-uniformity, all the layers to be laminated have to be flat enough to reduce the risk of die cracking. This can be achieved by introduction of thicker glue material in between the packages which can

compensate for the thickness offset at the chip edge of the non-flat UTCP during the adhesive melting step of the lamination process, finally resulting in a uniform thickness all over the stack area.

The result of this approach has been verified by use of 50 µm thick Adhesive glue (Pyralux LF 200) replacing the standard one, 25 µm thick LF 100 used in the previous batches. As cited in the Fig. 3, it leaves the glue uncured at the chip edge of the stacked packages after the lamination process. Additionally, chance of die cracking may not be avoided by this process which can be verified from the Fig. 3 showing crack on the top most embedded die of the stack. To get a better result, the whole lamination process has to be monitored with a close view on the adhesive flow step and applied pressure.

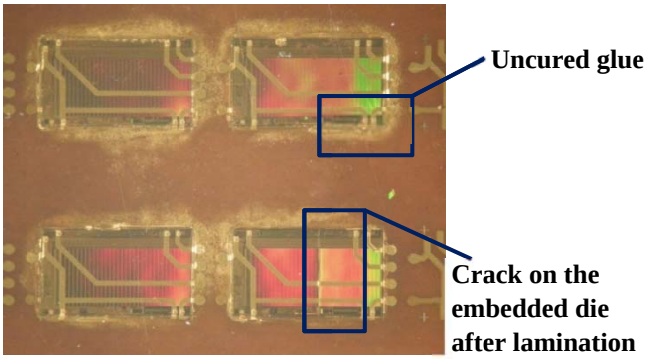


Figure 3. Top view of the laminated stack of non-flat UTCPs by using 50µm thick LF 200 as bonding material

Stacking of Flat UTCPs:

The next approach can be use of flat UTCPs by spinning an extra layer of polyimide of a thickness equal to that of the thinned dies in-between the base and top layers of the chip packages [3-6]. The embedding capability of the Flat UTCPs has already been confirmed by IMEC in the past couple of years [4-6]. A recent development in this technology confirms a 95% production yield by 3D-integrating this Flat-UTCP in standard flexible circuit board (FCB) [6].

Considering photolithography as an easy and faster way in the fabrication technology, use of photosensitive polyimide as this flattening layer makes the whole process faster in comparison to other processes like laser ablation or dry etching of non-photosensitive polyimides. For this approach, a HD 4110 from HD Microsystem was chosen for its advantages (particularly, negative photosensitivity, the high viscosity and self-priming property) over other commercially available polyimides [8]. After chip bonding on the base polyimide, this PDPI is spun and illuminated through the glass substrate from the backside. In this way the chip serves as the mask and during development only the non-illuminated PI on top of the chip is dissolved in the developer, thus creating a self-aligned cavity. Also the same polyimide is used as the subsequent covering layer (3rd layer) to open vias on the contact pads of all the chips by a single alignment and photolithography which reduces via patterning efforts and avoids the risk of damage during laser drilling. Considering the symmetry and CTE of the whole package the bottom layer (1st layer) is also chosen to be the same polyimide. The overview of the whole process is illustrated schematically in Fig. 4.

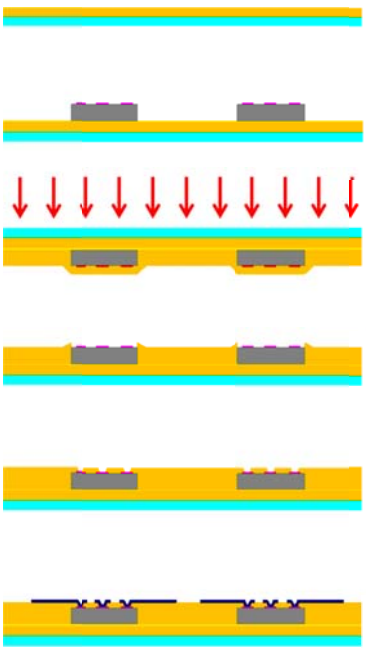


Figure 4. Process flow for producing multiple UTCPs on a single carrier

By use of this principle in fabricating UTCPs, the metal routing from the chip region to the external region has been significantly improved which avoids damage at the chip edge of the package. Additionally, photolithography as a well-controlled micro-via structuring technology enables to open vias down to 30µm diameter on the contact pads of the chip with an alignment accuracy of 5µm [7].

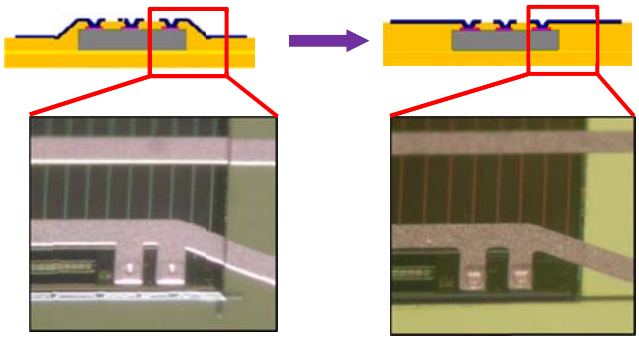


Figure 5. The transition from conventional UTCP to flat UTCP showing the improvement in via structuring on the contact pads of EEPROM memory die and non-uniformity in the package thickness at the chip edge.

Considering the self-priming property of the polyimide, a salt based release technology is developed and is reported by Wang et al. [7]. But this whole process has the disadvantage of shrinkage of the whole UTCP sheet after

release. Experimental and simulation results confirm that the shrinkage is higher in case of PDPI 4110 (CTE= 35ppm/C, linear shrinkage 1%) than the standard PI 2611 (CTE= 3ppm/C, linear shrinkage 0.2%). This implies for fabricating, these packages on glass carriers of higher dimension, e.g., 4" square or 6" square can lead to a total linear shrinkage of ~ 1 mm and ~ 1.5 mm, respectively. And this value is too high for the subsequent processes in 3D- integration technology in which mechanical and optical alignment are the most crucial steps. Additionally, this adds another risk of chip cracking after fabricating it in large area (4", 6", or higher). Due to high CTE mismatch between this PDPI and the carrier material (0.7mm thick glass, CTE= 8.7ppm/C), sometimes the entire 4" carrier with PDPI based UTCP on it warps in the direction of the package build-up. This makes it difficult to handle large samples in subsequent production processes, e.g, during mask alignment for via structuring.

Modified Process Flow for multiple Flat-UTCP

By considering all the above said process related issues, fabricating PDPI 4110 based multiple Flat UTCPs in large area is possible, if this stress due to high CTE difference between carrier and PI can be minimized. To achieve a better result, the large area multiple packages can be divided into pseudo-small islands of single packages during the PI processing phase by introduction of stress release grooves in the PDPI layers.

An experiment has been designed to produce 4 flat-UTCPs on a 2" carrier embedding 20µm thick EEPROM memory dies. In this new process, a thin metal pattern of TiW (50nm) is processed on the glass carrier which has both alignment layer for precise placement of chips and stress release patterns for polyimide processing. This pattern contains horizontal and vertical lines of width 100µm with a separation of 1.5mm which can be printed on both the flattening layer PI and/ or top covering layer of PI by back side illumination of UV through the glass carrier (Step3, Fig. 4). The mask design for this alignment layer can be visualised in Fig. 6.

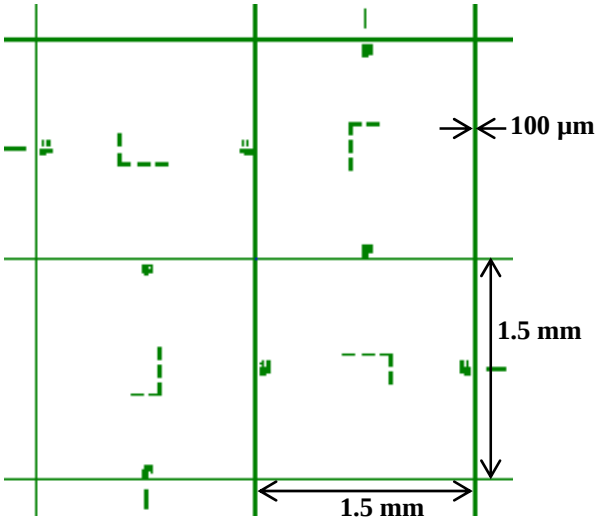


Figure 6. Design made for precise placement of 4 chips and stress release grooves on PI of width 100µm

This design has been realized in placing 4 chips on the base PI spinned and cured on a 2" glass carrier containing this alignment pattern, following the basic process flow [6-7]. For chip bonding on the substrate, BCB 3022-46 was used as adhesive material which was spun on the PI at 500 rpm for 10" ensuring uniform spreading, followed by 3000 rpm for 30" to get a thickness of ~3 µm and soft baked on a hot plate at 100°C for 1 min in clean room atmosphere. The 20µm thick EEPROM memory dies are picked, aligned and placed by Tresky Bonder with 10 µm alignment accuracy.

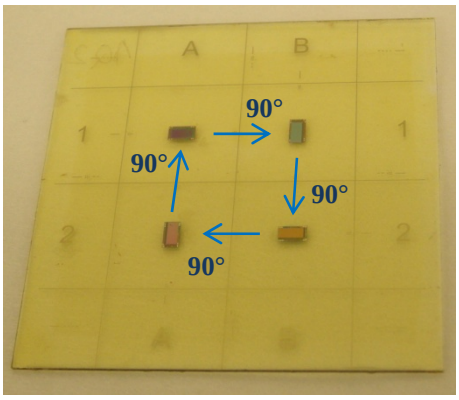


Figure 7. Orthogonally rotated 4 chips placed precisely on semi-transparent PDPI 4110 base layer looking through the alignment pattern on the 2" glass carrier

Furthermore, instead of making 4 separate mask designs for 4 different metal layouts on the chip package, a single design is made containing 4 orthogonally rotated layouts on the same mask (Fig. 8).

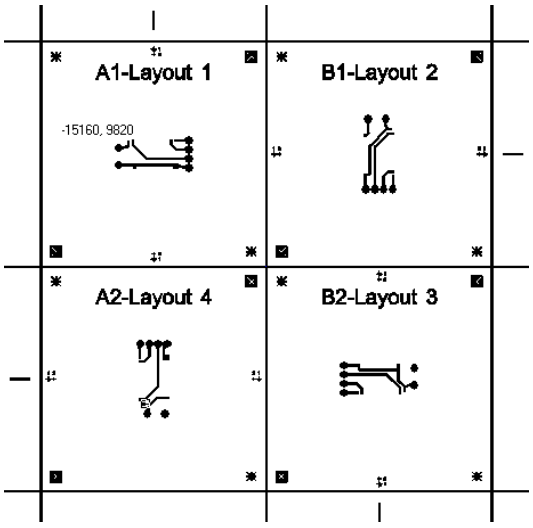


Figure 8. Design with 4 different layouts for metal patterning on the single substrate with 4 orthogonally rotated UTCPs

The schematic cross-section of the multi-UTCPs with stress release grooves is shown in Fig. 9. This contains stress release grooves of width ~100 µm and depth ~30 µm if it is patterned on both top and fattening layer of PI. The layer below this groove is base PI layer having a thickness of

~20um which may not provide sufficient strength after release from the carrier. To avoid this issue, these grooves can be filled with electroplated Cu (CTE ~ 16.7 ppm/C, less in comparison to PDPI 4110) up to certain depth (~10µm) during the same metallization and patterning step as in UTCP process flow.

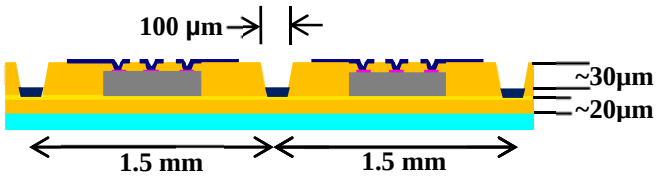
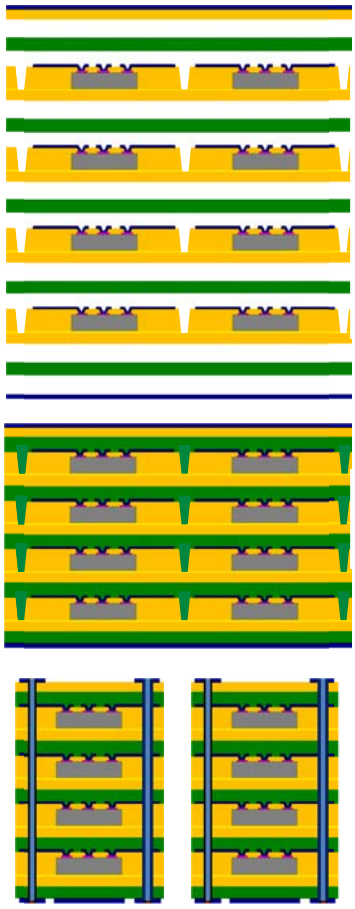


Figure 9. Schematic cross-section of Multi-UTCP with stress release grooves on flattening and top PI layers.

After releasing, a single panel will contain 4 islands of UTCPs with different metal layouts. Four of such panels with orthogonally rotated multiple chip packages can be aligned optically by sequential rotation of 90 degree and stacked together with an adhesive glue Pyralux LF 100 as bonding material in between each two panel of packages. Rest of the process flow includes micro via formation on the stacked outer contact pads by drilling through holes, plating, patterning and singulating the stacks. The schematic overview of the process flow is illustrated in Fig. 10.



Aligning the 4 layers of orthogonally rotated multiple UTCPs and additional Cu flexes on top and bottom with LF 100 as bonding material in between each two layers

Stacking of all layers by vacuum lamination technology

Singulated stacks after making through hole via interconnection by Laser drilling, followed by plating and patterning

Figure 10. Schematic overview of stacking of flat UTCPs process flow

Conclusions:

A recent development in the stacking of ultra thin chip package technology is being reported in this contribution. With an assumption to get a better yield, some experiments are still ongoing to produce stacks of Flat-UTCPs.

Acknowledgments:

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