

Excellent thermal stability by using PEALD ultra-thin Al₂O₃ film with Ta as Cu diffusion barrier on low k dielectrics

Shao-Feng Ding,¹ Qi Xie,² Fei Chen,¹ Hai-Sheng Lu,¹ Shao-Ren Deng,²
Christophe Detavernier,² Xin-Ping Qu^{1*}

¹. State Key lab of ASIC and System, Department of Microelectronics, Fudan University,
Shanghai 200433, China

². Department of Solid State Science, Ghent University, Krijgslaan 281/S1, B-9000 Ghent,
Belgium

ABSTRACT

Ultra thin Al₂O₃ films were deposited by plasma enhanced atomic layer deposition (PEALD) as Cu diffusion barrier on low-k (k=2.5) material. The thermal stability and electrical properties of the Cu/low-k system with Ta, Ta/Al₂O₃ and Ru/Ta layers with different thickness were compared after annealing. The TEM and EDX results reveal that the ultrathin Al₂O₃ films are thermally stable and have excellent Cu diffusion barrier performance. The I-V and TDDB electrical measurements further confirm that the ultra thin Al₂O₃ film is a potential Cu diffusion barrier in copper/*low k* interconnect.

Corresponding Author:

Xin-Ping Qu, Professor,

With the continuing scaling down of the line pitch in very large scale integrated circuits, ultrathin Cu diffusion barriers are necessary to mitigate the increase in the effective resistivity of the Cu interconnects due to grain boundary scattering and interface scattering. Conformal deposition of thin films in high aspect ratio trenches using traditional physical vapor deposition (PVD) technique is becoming difficult [1]. Atomic layer deposition (ALD) is considered as a promising method to get excellent conformal films with thickness control at atomic level owing to its intrinsic self-limited growth feature [2]. ALD grown metals or nitrides, such as Ru [3-4], and TaN films[5,6], have been widely studied as Cu diffusion barriers or adhesion layers. ALD grown oxides, such as TiO₂[7], Ta₂O₅ [8] and Al₂O₃ [9] have also been reported as Cu diffusion barriers due to their excellent uniformity and thermal stability. Qi Xie *et.al* reported the excellent thermal stability of ALD TiO₂. [7] P. Majumder *et. al.* reported that the ultrathin Al₂O₃ layer deposited by thermal ALD as diffusion barrier between Cu and Si substrate had excellent thermal stability.[9] However, these oxide layers were all directly deposited onto Si and the very primary properties of diffusion barriers to Cu were measured. Systematic study of ALD oxide films as Cu diffusion barrier on the low-k dielectric has been rarely reported. In this work, ultra thin Al₂O₃ films were deposited by plasma enhanced atomic layer deposition (PEALD) together with Ta adhesion layer, its properties as a Cu diffusion barrier on the *low k* dielectric ($k=2.5$) were studied.

The low k films (Novellus CORAL, $k=2.5$) were deposited on the 12" p-type Si wafers with a thickness of 220 nm. The wafers were cut into small pieces and then were cleaned in an ultrasonic cleaner with 2-propanol solution before loading to the loadlock chamber. After in-situ annealing at 250 °C for 20 minutes in the high vacuum ALD chamber, 11 or 21 cycles ($\sim 1.2 \text{ \AA/cycle}$) Al₂O₃ films were

grown by plasma enhanced atomic layer deposition (PEALD) using trimethylaluminium (TMA) and remote O₂ plasma (200W) as precursors. The growth temperature was 250 °C. After deposition, samples were taken out and sent into a PVD chamber. The details of the ALD growth can be seen elsewhere.[7] Then the Cu(50 nm)/Ta(5 nm) film stacks were deposited by DC magnetron sputtering. The thin Ta film was used as a glue layer to promote adhesion between the Cu and Al₂O₃ barrier layers. To form the patterned metal-insulator-semiconductor (MIS) structures, a shadow mask was used when depositing the Cu/Ta stacks. For comparison, the Cu/Ta stack was also directly deposited onto the low *k* substrates. A Ti(40 nm)/Pt(30 nm) bi-layer was deposited as backside electrode by sputtering. Furnace annealing was conducted in the N₂ atmosphere at 400 °C for 30 minutes. After annealing, energy dispersive X-ray (EDX) transmission electron microscope (TEM), time-dependent dielectric breakdown (TDDB), and dielectric breakdown measurements were used to characterize the thermal stability and electrical reliability of the Cu/barrier/low *k*/Si system. The capacitance-voltage (C-V) measurements were carried out using an HP 4192A impedance analyzer to evaluate the effective *k* value of the system.

The XTEM images of the as-deposited Cu/Ta/Al₂O₃ (22cycle) /low *k*/Si samples and the one annealed at 400 °C/30min were shown in Fig. 1(a) and (b). For the as-deposited sample, the thickness of the Ta and Al₂O₃ layer is about 5 nm and 2.5 nm, respectively. The interface between the Ta and Al₂O₃ layer is clear. The contrast between the Al₂O₃ layer and the low-*k* dielectric is not obvious due to the amorphous oxide structure for both Al₂O₃ and low *k*. For the annealed sample, the Ta and Al₂O₃ layer become mixed and the thickness of the barrier is 7.1 nm. The barrier is continuous but the interfaces of Cu/barrier and barrier/low *k* are obscure. Fig.2 shows

the corresponding EDX depth profiles of these two samples. It can be seen that there is no Cu signal in the low k dielectric after annealing. For comparison, we also prepared other two kinds of samples, one is sputtered Cu/Ta (5 nm) and the other is sputtered Cu/ALD Ru (7 nm)/ALD TaN(5 nm) on the low k dielectrics. All the samples were annealed at 400 °C for 30min. The experimental detail of ALD growth of the Ru/TaN bi-layer barrier can be seen elsewhere [4]. Fig.3 (a) and (b) show the XTEM images of the Cu/Ta/low k /Si and Cu/Ru/TaN/low k /Si samples annealed at 400 °C for 30min. For the Cu/Ta/low k /Si sample, after annealing at 400 °C, there appeared a diffusion region between the Ta layer and low k . The EDX results, not shown here, revealed that there were strong Cu signals, about 10% in the diffusion region. For the Cu/ low k sample with ALD Ru/TaN bilayer as diffusion barrier (Fig.3(b)), after annealing at 400 °C for 30 minutes, the Ru/TaN barrier was markedly destroyed and there was a diffusion region around 50 nm thick between the barrier layer and low k . The EDX results (not shown here) revealed that Cu signals almost appeared in every detect point, including the outside of the diffusion region. The failure of the ALD Ru/TaN stack is believed to be due to the diffusion of the Ta precursor to the porous low k dielectric during the ALD process. The diffusion of Ru precursor into the ULK during the ALD process was also observed by Heo *et.al.* [3] Although in the ALD deposition of Al₂O₃, the TMA precursor may also diffuse into the porous low k , but Al₂O₃ is very easy to form and it can act as a barrier to prevent the further penetration of precursor. Our results demonstrate that the thermal stability of the Ta(5 nm) /Al₂O₃(2.5 nm) barrier stack is not only better than the Ta film itself, but also the thick ALD Ru(7nm)/TaN(5 nm).

The surface morphologies of Cu on the Ta/low k and Ta/Al₂O₃ (2.5 nm)/low k substrates are observed by SEM. As shown in Fig.4, after annealing at 400 °C for 30

min in N₂, the Cu on the Ta/low k substrate experiences severe agglomeration; but for the samples with Ta/Al₂O₃ stack, there are no pinholes on the Cu surface. Agglomeration of the Cu films can be caused by reaction of barrier with moisture outgassed from the low k substrate, as well as the degraded Cu adhesion with barrier due to the oxidation of the barrier. [10-12] Thin Al₂O₃ films deposited by ALD used as superior moisture and oxygen barriers for organic devices has been reported. [13] Moisture barrier is also important for low k dielectrics, since the oxidation of Cu lines induced by the absorption and outgas of moisture in dielectric may degrade the electrical properties of the Cu interconnects. [14-15] Therefore, in our case, the ALD oxide layer can also suppress the moisture outgassed from the low k dielectric and enhance the Cu adhesion on Ta.

Since Al₂O₃ is a kind of high k dielectrics ($k \sim 9.0$), [16] its effect on the effective dielectric constant of the Cu/low k system was evaluated. The C-V measurements were carried out for the Cu/Ta/Al₂O₃(1.3 nm)/low k /Si, Cu/Ta/low k /Si and Cu/Ta/TaN(5 nm)/low k /Si MIS capacitor. The original k value was 2.55 after IPA cleaning. After sputtered deposition of the metal stacks, the measured effective k values (k_e) of all the capacitors were all increased. The k_e values for the Cu/Ta/low k /Si and Cu/Ta/Al₂O₃(1.3 nm)/low k samples were the same (2.8) and lower than that of the Cu/Ta/TaN(5 nm)/low k /Si (3.0). The increase of the effective k value is mainly due to the damage of the low k dielectric during the deposition and annealing process as well as the oxidation of the TaN barrier. These results indicate that using an ultra thin Al₂O₃ films as Cu diffusion barriers doesn't affect much on the k value of the low k dielectric.

The electrical properties of the Cu gated MIS structures were measured. Figure 5(a) shows the leakage current densities of the the as-deposited MIS capacitors with Ta(5

nm), with Ta(5 nm)/Al₂O₃(1.3 nm) and Ta(5 nm)/Al₂O₃(2.5 nm) as diffusion barriers and those after annealing at 400 °C for 30 minutes in N₂. The leakage current densities for all the as-deposited and annealed samples were similar under the applied electric field of 1MV/cm. Further we compared the breakdown voltages for these samples. Figure 5(b) shows the cumulative failure distribution of breakdown electric field (E_b) of the capacitors with different diffusion barriers after annealing at 400 °C for 30 minutes in N₂. For capacitors with the Ta(5 nm)/2.5 nm Al₂O₃ stack, E_b is mainly around 9 MV/cm; for those with 5 nm Ta layer and Ru/TaN, E_b is lower than 3 MV/cm. Although the E_b is similar for the samples with 1.3 nm or 2.5 nm Al₂O₃ layer, but the TDDB measurements (figure not shown here) show that the TDDB of the annealed MIS capacitor with 1.3 nm Al₂O₃ is about 2.3×10^4 s under a stressing field of 7.7 MV/cm; for the MIS capacitor with 2.5 nm Al₂O₃ layer, the TDDB exceeds 1.7×10^5 s under an higher EM of 8.6 MV/cm. Although under RT, copper is difficult to migrate under low electric field, it can move very rapidly under a high electric field through defects in the diffusion barrier. The presence of Cu in the dielectrics would greatly reduce dielectric life time. [17] Our results further indicate that the Al₂O₃ film is an excellent barrier for Cu metallization and the thickness of the Al₂O₃ film also has great effect on the Cu barrier performance.

In conclusion, by using PEALD, robust ultra thin Al₂O₃ films were deposited on the ULK dielectric as Cu diffusion barrier. The effective k value of the dielectric doesn't change by using ultrathin Al₂O₃ film. The TEM and EDX results reveal that there is no Cu diffusion in the Cu/Ta/Al₂O₃(2.5 nm)/low k sample. The breakdown voltages and the failure time can be improved greatly by using the Ta/Al₂O₃ stack as Cu diffusion barrier layer. Overall, our results demonstrate the potential of using an

ultrathin PEALD Al₂O₃ film together with a thin Ta adhesion layer as a barrier stack for the future Cu interconnects.

ACKNOWLEDGMENTS

This work was supported by National Basic Research Program of China (Grant No. 2011cba00603), State Key Research Program of China (Grant No. 2009ZX02308-005). This work was also supported by the Bilateral Scientific and Technological Corporation Project Flanders-China (01SB1809).

REFERENCES

1. D. C. Perng, J. B. Yeh, K. C. Hsu, S. W. Tsai, *Thin Solid Films*, **518**, 1648 (2010)
2. R. L. Puurunena, *J. Appl. Phys.*, **97**, 121301 (2005).
3. J. Heo, S. - J. Won, D. Eom, S. Y. Lee, Y. B. Ahn, C. S. Hwang, and H. J. Kim, *Electrochem. and Solid-State Lett.*, **11**, H210 (2008)
4. Q. Xie, Y. L. Jiang, J. Musschoot, D. Deduytsche, C. Detavernier, R.L. Van Meirhaeghe, S. Van den Berghe, G. P. Ru, B. Z. Li, and X. P. Qu, *Thin Solid Films*, **517**, 4689 (2009).
5. A. Furuya, H. Tsuda, and S. Ogawa, *J. Vac. Sci. Technol. B.* **23**, 979 (2005).
6. Q. Xie, J. Musschoot, C. Detavernier, D. Deduytsche, R. L Van Meirhaeghe, S. Van den Berghe, Y.-L. Jiang, G.-P. Ru, B.-Z. Li and **X.-P. Qu**, *Microelect. Eng.* **85**, 2059 (2008)
7. Q. Xie, J. Musschoot, D. Deduytsche, R. L Van Meirhaeghe, C. Detavernier, S. Van den Berghe, Y.-L. Jiang, G.-P. Ru, B.-Z. Li, **X.-P. Qu**, *J. Electrochem. Soc.* **155**, H688, (2008)
8. A. Lintanf Sala ñin, A. Mantoux, E. Blanquet, and E. Djurado, *J. Electrochem Society*, **156**, H311 (2009)_
9. P. Majumder, R. Katamreddy, and C. Takoudis. *Electrochem. Solid-State Lett.* **10**, H291 (2007).
10. Y. Hayashi, M. Abe, M. Tada, M. Narihiro, M. Tagami, M. Ueki, N. Inoue, F. Ito, H. Yamamoto, T. Takeuchi, S. Saito, T. Onodera, and N. Furutake, *IEEE Trans. Elec. Dev.*, **56**, 1579 (2009).
11. M. Hamada, K. Ohmori, K. Mori, E. Kobori, N. Suzumura, R. Etou, K. Maekawa, M. Fujisawa, H. Miyatake, and A. Ikeda, *Proc. IITC*, 13-4 (2010).

12. S. F. Ding, S. R. Deng, H. S. Lu, Y. L. Jiang, G. P. Ru, D. W. Zhang, and X. P. Qu, *J. Appl. Phys.*, **107**, 103534 (2010).
13. P. F. Carcia, R. S. McLean, and M. H. Reilly, *Appl. Phys. Lett.* **97**, 221901 (2010).
14. T. Watanabe, Y. Hayashi, H. Tomizawa, T. Usui, A. Gawase, M. Shimada, K. Watanabe and H. Shibata, *Proc. IITC*, p. 208 (2008)
15. M. Hamada, K. Ohmori, K. Mori, E. Kobori, N. Suzumura, R. Etou, K. Maekawa, M. Fujisawa, H. Miyatake, and A. Ikeda, *Proc. IITC*, 13.4 (2010).
16. K. B. Jinesh, J. L. van Hemmen, M. C. M. van de Sanden, F. Roozeboom, J. H. Klotwijk, W. F. A. Besling, and W. M. M. Kessels, *J. Electrochem. Soc.*, **158**, G21(2011)
17. J. R. Lloyd, C. E. Murray, S. Ponoth, S. Cohen, and E. Liniger, *Microelectron. Reliab.*, **46**, 1643 (2006).

Figure Captions:

Fig. 1 The XTEM images of (a) the as-deposited Cu/Ta(5 nm)/Al₂O₃(2.5 nm)/low-k/Si sample; and (b) the sample after annealing at 400 °C for 30 minutes.

Fig. 2 The EDX depth profiles of Cu, Ta and Al of (a) the as-deposited Cu/Ta(5 nm)/Al₂O₃(2.5 nm)/low-k/Si sample; and (b) the sample after annealing at 400 °C for 30 minutes.

Fig. 3 The XTEM images of (a) the Cu/Ta(5 nm)/ low-k/Si sample after annealing at 400 °C/30 min; and (b) the Cu/Ru(7 nm)/TaN(5 nm)/low-k/Si sample after annealing at 400 °C/ 30 min.

Fig. 4 The SEM surface morphology of the (a) as-deposited Cu (50nm)/Ta(5 nm)/low *k* /Si and (b) the one annealed at 400 °C /30min; and (c) the as-deposited Cu/Ta(5 nm)/Al₂O₃(2.5 nm)/Si sample and (d) the one annealed at 400 °C/ 30 min.

Fig.5 (a) Leakage current densities of the Cu gated MIS structures with different diffusion barriers after annealing at 400 °C for 30 minutes and 50 minutes; and (b) Cumulative failure distribution of the breakdown voltage of the MIS capacitors with different Cu diffusion barriers after annealing at 400 °C for 30 minutes. The voltage step is 1V/s.

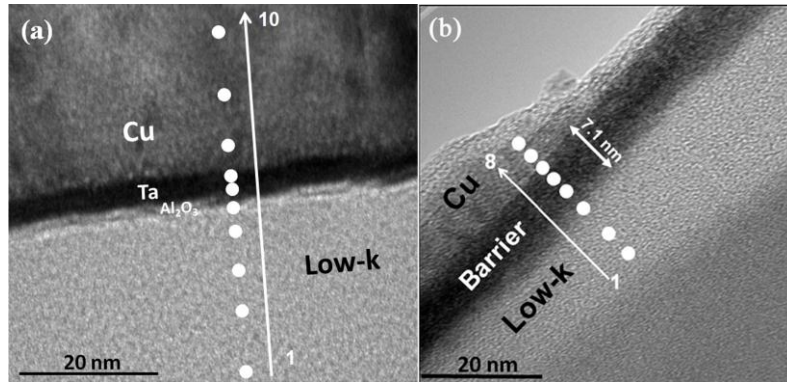


Fig. 1

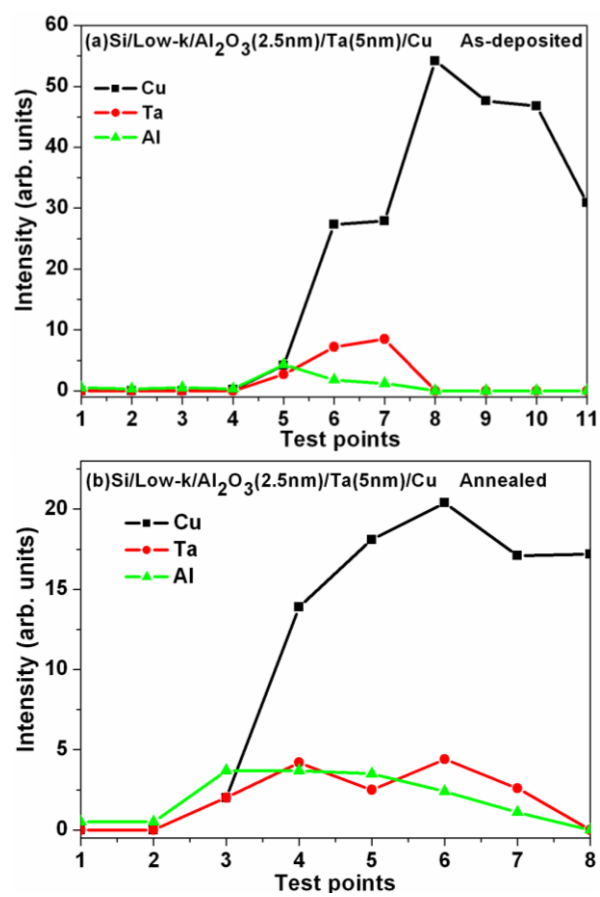


Fig. 2

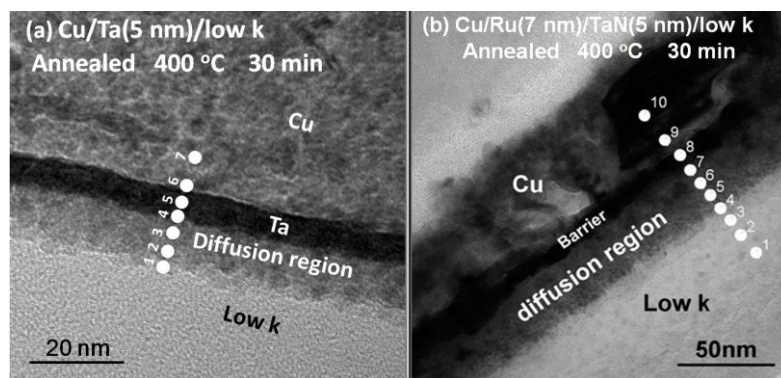


Fig.3

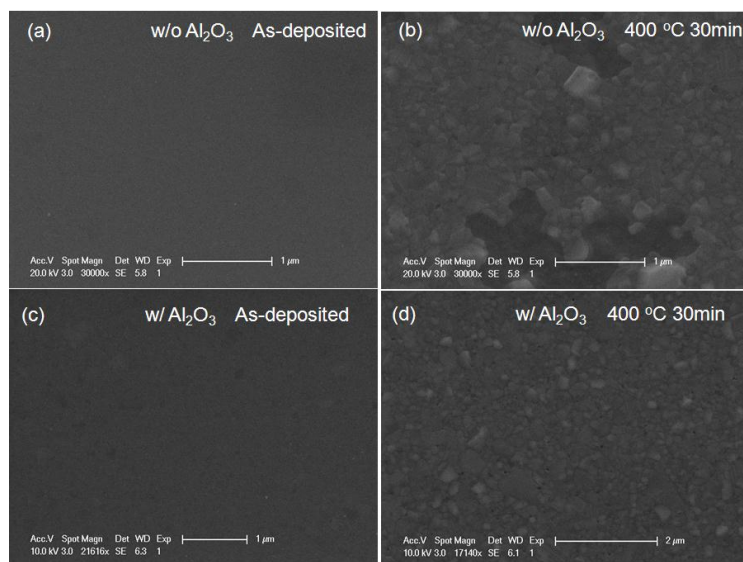


Fig.4

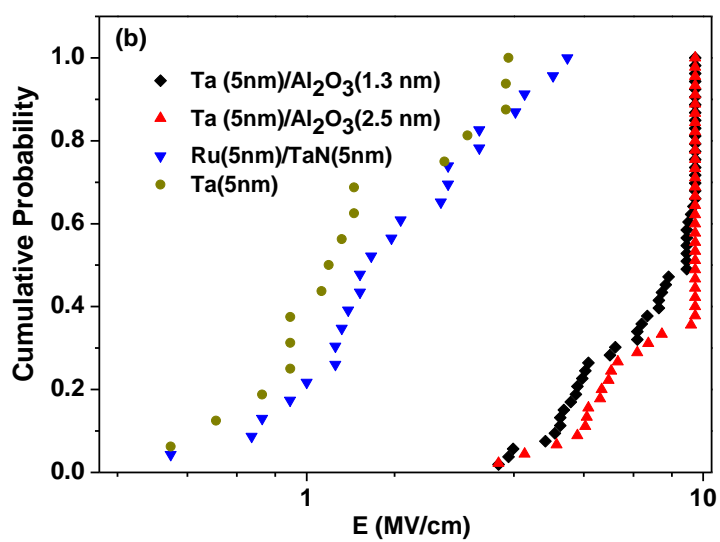
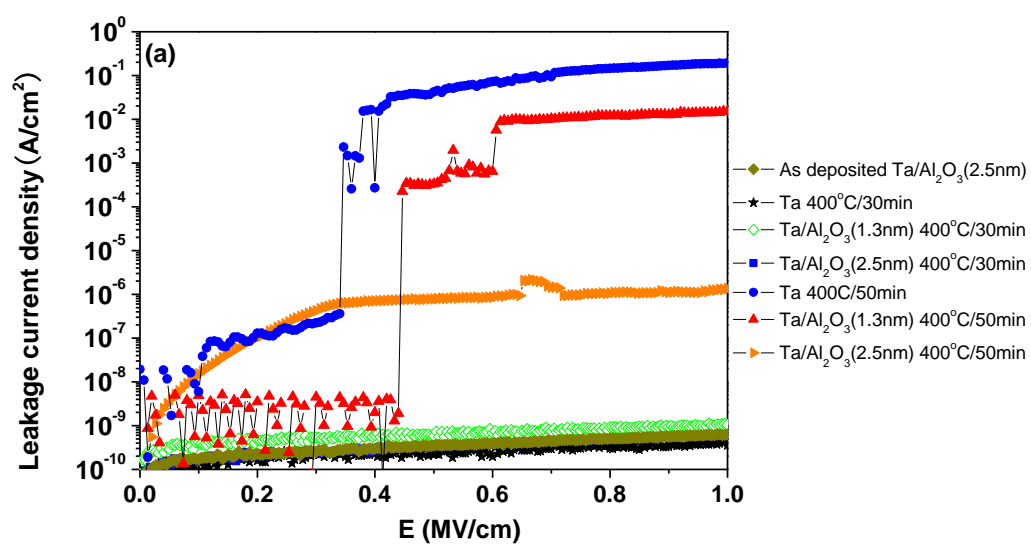


Fig.5