High Yield Embedding of 30μm Thin Chips in a Flexible PCB using a Photopatternable Polyimide based Ultra-Thin Chip Package (UTCP)

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Abstract

A thin chip package for off-the-shelf ICs is developed which enables the embedding of these chips into a flexible circuit board. The package consists of a copper fan-out on a polyimide substrate, in which the thinned IC (30μm) is embedded. These packages are subsequently integrated in a standard flexible circuit board (FCB). A microcontroller and a proprietary DSP processor are embedded using this technology. The yield of the Ultra-Thin Chip package (UTCP) was measured before embedding in the circuit board, and reaches up to 87% for the packaged microcontrollers (MSP430 family, known-good dies). The yield on the DSP processor was measured to be 62%. After embedding in the FCB, 95% of the functional UTCP-packaged dies are still functional.

Key Words: Ultra-thin chip package, flexible circuit board, polyimide, chip thinning, 3D integration

Introduction

There is a tendency in the design of electronic systems to combine more and higher level functionalities into smaller and light-weight packages. The challenge in realizing these systems does not only rely on the electronics engineer, who needs to integrate data acquisition, data processing and radio communication into a low cost, low power but highly reliable system. The success of the device also depends on the packaging engineer, who is responsible for realizing a small, light-weight and reliable package. Additional application-specific package functionalities become more popular, such as flexibility or stretchability of the packaged system, requirements often needed when considering medical devices. The fabrication of such state-of-the-art packages is not straightforward, an optimized fabrication process with high yield is essential to keep the packaging cost at an acceptable level.

If miniaturization of system dimensions is required, a good solution is found in the extension of the natural 2D character of electronics into the third dimension. This can be done on chip level [1,2], as well as on board level [3,4]. In this work we present a methodology which enables the miniaturization of a system using both novel chip level and board level packaging technology.

A commercially available die is thinned down to 30 μm and packaged in an Ultra-Thin Chip Package (UTCP). This package contains a fanout, which transforms the small pitch of the contact pads on the chip, typically ~100μm, to the larger dimensions and pitches which are used in the production of printed circuit boards (PCB) and flexible circuit boards (FCB), typically dimensions around 1mm. After die packaging using UTCP technology, functionality tests of the dies are performed, which avoids a lower final system yield –and hence extra costs- by using non-functional UTCPs.

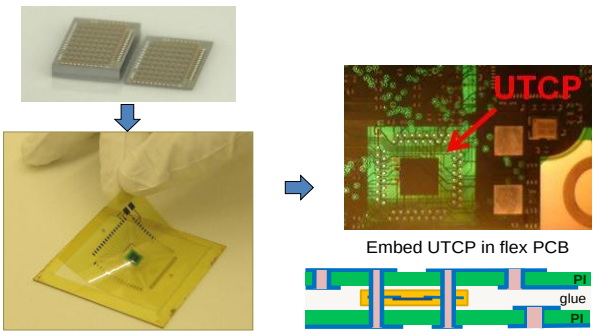

Figure 1: The raw silicon die is first thinned and packaged in a polyimide membrane. This ultra-thin chip package is subsequently embedded in a flexible circuit board.

This selection of known-good UTCPs allows also for building systems based on multiple UTCP-packaged dies with an acceptable system yield.
After testing, the functional UTCPs are released from their glass carriers on which they were fabricated, and embedded in an FCB by fixing the polyimide membrane on the adhesives used in the FCB laminating process. The FCB is finally finished by drilling the necessary vias and plating using Cu to ensure proper electrical contacts. An overview of this process is given in Figure 1.

The technology used in this paper thus provides a hybrid approach to 3D integration: the UTCP-packaged IC can not only be packaged in a flexible circuit board, which allows placing passives on top of the IC, but it also allows for stacking multiple UTCP packages on top of each other [2]. In this way a conformable system package with minimal dimensions is realized by embedding CMOS into flexible circuit boards.

Ultra-Thin Chip Package

The technology of embedding thinned dies in a polyimide foil was developed and presented by Christiaens *et al.* in 2006 [5]. The process was based on non-photosensitive polyimide PI2611 (by HD microsystems [6]), which is spincoated and patterned using laser ablation. This package was later used to demonstrate 3D integration by embedding a UTCP-packaged microcontroller MSP430F149 in an FCB [7]. The process flow and integration strategy presented in this contribution is based on this early work, however with an important additional focus on the development of the following aspects:

- Increasing the production capacity
- Improving the yield of the UTCP packaging technology
- Applicable to different types of ICs

These considerations have led to the following changes with respect to the initial process flow of 2006 [8,9]:

- The introduction of a photosensitive type of polyimide allows increasing the production capacity by exposing multiple vias, and eventually multiple dies at once, as opposed to opening the vias using laser ablation.
- The use of a new release strategy based on KCl
- Embedding the chip in a cavity improves the step coverage of the polyimide and avoids shorts in the fanout.

UTCP process-flow

To illustrate our new high-yielding UTCP process flow, two ICs are selected to demonstrate the UTCP concept.

The first IC is a commercially available microcontroller from Texas Instruments, MSP430F1611. Directly after CMOS processing, the Aluminum contact pads of the dies were covered with an electroless nickel-gold (ENIG) finish. Next, the wafers get a partial dicing step, followed by wafer thinning ('dicing-by-grinding' process) to fabricate thin single chips with a thickness of 35µm. This wafer level dicing-by-grinding process is a commercially available process offered by Disco [10].

The second type of chip is a proprietary DSP processor ASIC. The contact pads of these dies consist of standard aluminum pads. The dies are thinned on a die-level by grinding and polishing, using a Logitech PM5 lapping and polishing system. In this process the individual dies (4.2x2.1 mm^2) are mounted upside down on a glass carrier using wax as a temporary adhesive. The edges of the dies are protected by surrounding them by dummy Si-chips to prevent chipping of the silicon. The dies are thinned down to a thickness of 40µm in several steps using gradually diminishing grains sizes. To end this die thinning process, the dies are polished down to their final thickness of 35µm by CMP, in order to remove all possible micro-cracks in the silicon caused by the previous thinning steps. Note that due to the manual character of this chip thinning a variation on the thickness is measured between 32µm and 35µm. Furthermore, the dies are warped after thinning due to internal stress (Figure 2).

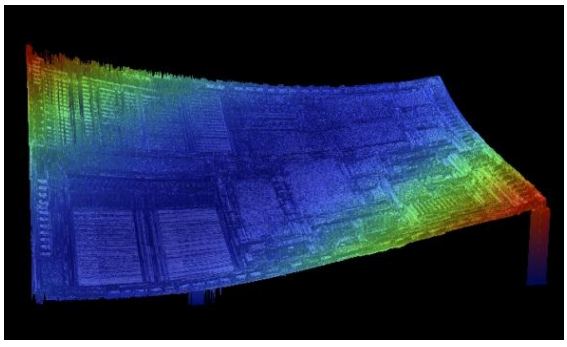

Figure 2: A profilometric scan of the MSP430F1611 microcontroller illustrates the warping of the die due to internal stress distributions, which can go up to a bending radius of 5cm. In this case the height difference between the tips and the middle of the die goes up to 120µm.

The elementary steps of the UTCP process flow are shown in Figure 3. The package is built on a 2" square glass substrate (white-float glass). Prior to processing, the substrates are cleaned from organics and particles from fabrication and transport using an RBS detergent, followed by a sequence of acetone and IPA cleaning steps. Next, the substrates are covered with a 400nm layer of thermally evaporated KCl salt, which is patterned using a shadow mask. This layer serves as a release agent at the end of the UTCP fabrication process: the photosensitive polyimide (PSPI) which is used in this process has a built-in priming function, and therefore adheres very well to the substrate on the KCl–free area. The hygroscopic nature of KCl allows an easy release of the UTCP package after processing, by making an incision in the polyimide membrane (manual cutting or by laser ablation), and dissolving the salt in water.

On top of the release layer, a layer of polyimide HD4110 precursor is applied by spinning at 1800rpm. This spinning speed results in a layer thickness of 18µm, which is reduced to 15µm after curing. The curing is performed in two stages: at first the samples are heated up to 200°C, and kept at this temperature for 30 minutes in a vacuum oven. The oven is flushed with a minor flow of nitrogen. Next the temperature is ramped up to 375°C, and the samples are cured for 1 hour. Finally the samples are cooled to room temperature in 5 hours (natural cooling of the oven). Note that the KCl release layer is compatible with these high curing temperatures of the polyimide base layer.

At this moment the thinned die is glued on the polyimide substrate using BCB as adhesive [11], as shown in Figure 3.a. BCB is selected as adhesive, since no outgassing occurs during curing of BCB, therefore no gasses are trapped underneath the thinned die. Furthermore, BCB can withstand the high curing temperatures of polyimide, which will be needed in further on in the process. During the cure of BCB a pressure of approximately 2 Bar is applied on the die in order to flatten the chip from its initial warping (illustrated by Figure 2).

The next step consists of spinning and patterning a second layer of photodefinable polyimide HD4110. The layer is once more spun at a speed of 1800 rpm for 60 seconds, only now the layer is exposed and developed before curing the precursor. The goal of this layer is to overcome the topography created by the sidewalls of the 35µm thick chip, in order to avoid step coverage problems in the last steps of the process flow. To avoid misalignment issues, the chips themselves are used as a mask for patterning of the negative tone PSPI by exposing the polyimide from the bottom side through the transparent glass substrate. The polyimide precursor is finally cured using the same procedure as was used for curing the base layer, in a vacuum oven at 375°C (Figure 3b).

The plating step in Figure 3c is executed only on the DSP processor, in order to apply an electroless nickel-gold finish on the contact pads of the IC (ENIG finish). Note that the bulk area of the IC is now almost completely sealed from the plating chemistry, thus avoiding the creation of a galvanic cell, which could be the trigger for skipping of bondpads during electroplating.

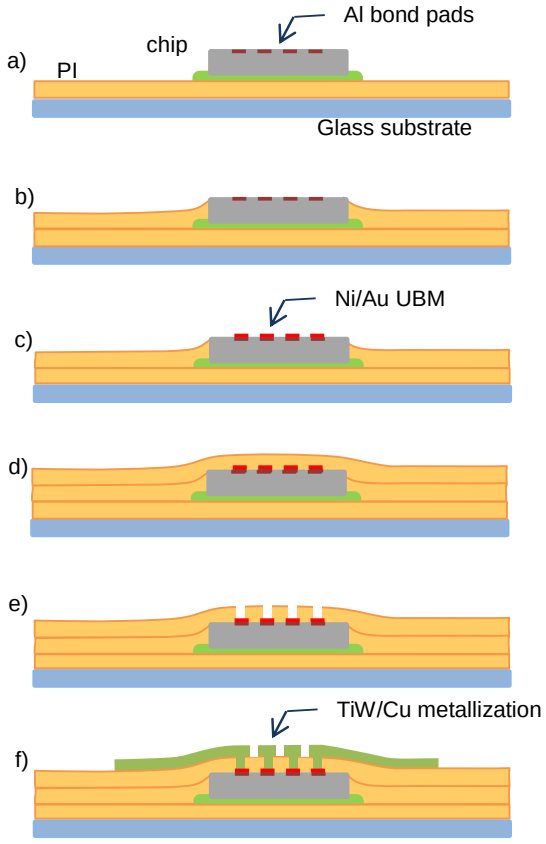

Figure 3: The elementary steps of the UTCP packaging flow.

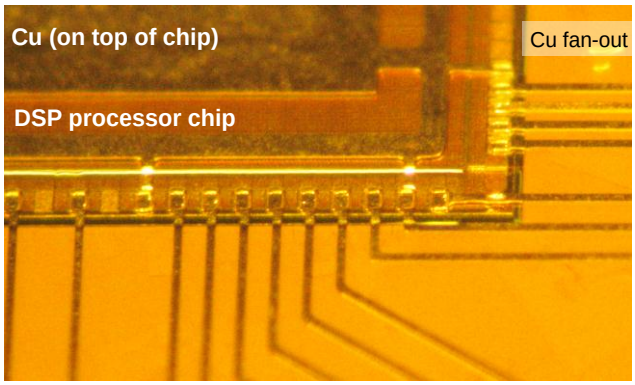

Figure 4: Photograph of the copper fanout on the DSP processor.

The top layer of photosensitive polyimide is applied after a drying step and a short plasma etching step using CHF_3 and O_2 in a 1:5 mixture. These steps are inserted to improve the adhesion of the top polyimide to the underlying layers. The polyimide layer is once more spun at a speed of 1800 rpm for 60 seconds (Figure 3d), and the polyimide is exposed and developed in order to open the vias to the gold-finished contact pads (Figure 3e).

In the final steps before UTCP release, a 50nm TiW adhesion layer and a 1µm copper seed layer are sputtered on the top polyimide. Next the copper layer is electroplated up to a thickness of 8µm, patterned by lithography and a fan-out is etched from the copper (Figure 3f, Figure 4). This thickening of the metallisation is required in order to successfully embed the UTCP package into a flexible circuit board: as the through hole vias of the FCB are drilled perpendicularly to the surface of the FCB, through the copper of the UTCP, the contact area between the via and the UTCP is defined by the height of the copper cylinder which is created by drilling the via (cfr. infra, Figure 6).

Finally the UTCP can be tested using a probecard which is mounted on the fan-out, in order to identify the failures and embed only known-good packages. Such test should be carried out prior to UTCP release, since probing a thin flexible unsupported package is rather difficult.
This test procedure is followed by UTCP release, as described above: an incision is made in the polyimide, and the sample is immersed in water. In this way the salt sacrificial layer is dissolved, and hence the sample is released from the carrier.

Test results and yield

The process flow described in the previous section was used to package 32 microcontrollers of the MSP430 family, and 16 DSP processor ASICs. In Table 1 an overview is given of the geometrical characteristics of both ICs, while Figure 4 illustrates these geometries with a close-up photograph of the UTCP-packaged dies. Besides the fan-out which is intended for embedding the dies in an FCB, our design also incorporates a second fan-out which is compatible with the test-setup used to test the functionality of the dies. It is clear that the use of a dedicated probe card for tests, which fits the small fan-out, will allow squeezing more UTCP packages on one substrate. In this way the throughput of the process can easily increase by a factor 5.

The testing of the UTCP-packaged dies is a two-step process: at first the threshold voltage of the ESD diodes of the bond pads is verified. These values give a first impression of the quality of the interconnection between the fan-out and the IC. Next, a full functionality test is performed: both ICs are programmed with test-software and the response is evaluated.

Out of the 32 processed microcontrollers, 28 or 87.5% were fully functional, as opposed to 66% in [8]. Three of the failures could be traced back to errors during processing (bad lithography, air bubbles in the BCB adhesive, broken substrate due to human error). The last failure consisted of a bad interconnection between one I/O and the fan-out, where the resistance of the interconnection was measured to be 100 Ohm.

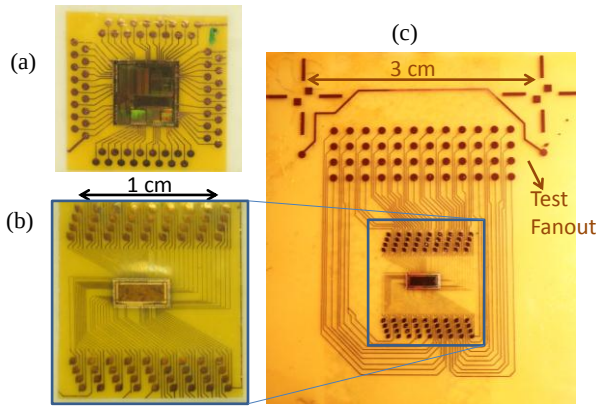

Figure 5: UTCP package with fan-out prior to embedding in FCB: (a) the microcontroller-UTCP and (b) the DSP processor – UTCP. Both UTCPs occupy only about 1.5 mm^2.
(c) same DSP chip with a second larger test fan-out allowing for extensive manual testing (large contact pitch). The larger test fan-out will be removed prior to embedding of the UTCP in a FCB.

	Die Size	*Fanout Size*	*Test pad size*	*Min. Bond pad spacing*	*# bondpads*
MSP430F1611	4.6x4.4 mm^2	1.2x1.2 cm^2	2x0.5 cm^2	25 um	64
DSP Asic	4.2x2.1 mm^2	1.4x1.2 cm^2	2.5x1 cm^2	12 um	72

Table 1: The table gives a summary of the geometry of the two ICs which have been packaged.

Ten DSP ASIC samples out of 16 processed dies were tested to be fully functional, which results in a yield of 62.5%. Three failures could be traced back to human processing errors, while the other samples suffered from bad interconnections to the bondpads, which was discovered by measuring the ESD diodes. The origins of these last failures are unknown.

FCB embedding

The embedding of a UTCP into a flexible circuit board is based on an existing process that is commercially available at ACB nv, a Belgian PCB manufacturer who specializes in high tech and short turn-around PCB manufacturing [12]. A first version of this packaging procedure was presented in In this process multiple copper cladded polyimide sheets are laminated using LF0100 as sheet adhesive. In this work a 4-layer circuit board was targeted, constructed as illustrated in Figure 6. In this build-up a double-sided metalized polyimide sheet with a thickness of 50µm is laminated to two single sided sheets

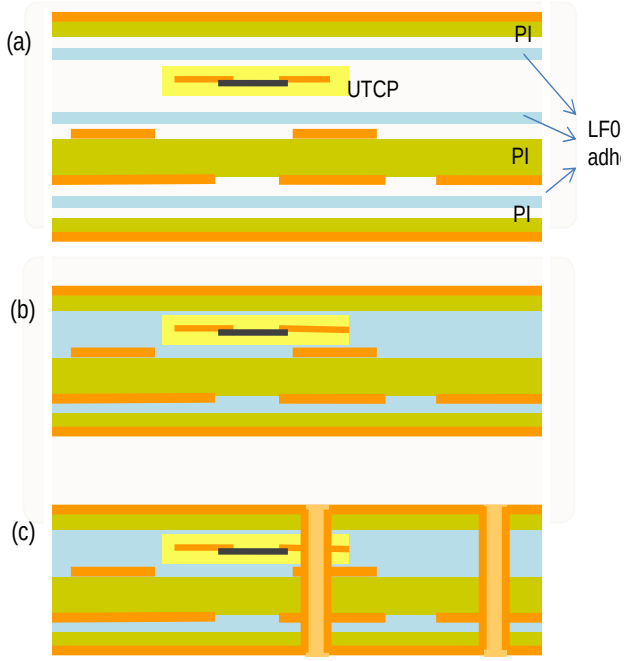

Figure 6: Schematic overview of the embedding process of a UTCP in an FCB: (a) layer build-up; (b) after lamination; (c) finished FCB

The UTCP is (manually) aligned to the metal pattern on the inner layers of the middle flex with an alignment error smaller than 25µm. The UTCP sample is fixed to the LF0100 adhesive by locally heating the adhesive. The complete stack is then laminated by applying pressure and heat in a vacuum environment. The drilling and electroplating of the vias and the optional application of solder mask or silkscreen was executed in the conventional way by ACB nv. In Figure 7 a cross-section image is given of an embedded UTCP in FCB, various height measurements are performed: the thickness of the UTCP package is 73.6 µm, which is close to the design thickness of 73 µm.

Test results and yield

In this run 10 pairs of packaged UTCPs were packaged in flexible circuit boards. To determine whether the UTCPs remained fully functional during this embedding process on FCBs, the UTCPs were tested in two ways: first the connectivity to the IC is verified by measuring the threshold voltage of the ESD diodes where possible, secondly a simple functionality test is performed by programming the DSP processor and the microcontroller, using a test connector which is mounted on the FCB. Only one UTCP embedded in FCB did not perform as expected, the failure was caused by a misalignment of the UTCP to the FCB's inner metal layers. The yield of embedding of UTCP in FCB can be estimated to be close to 95%.

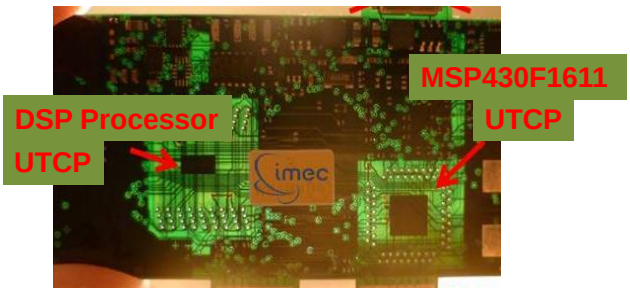

Figure 7: The embedded UTCP packages can be seen through the FCB.

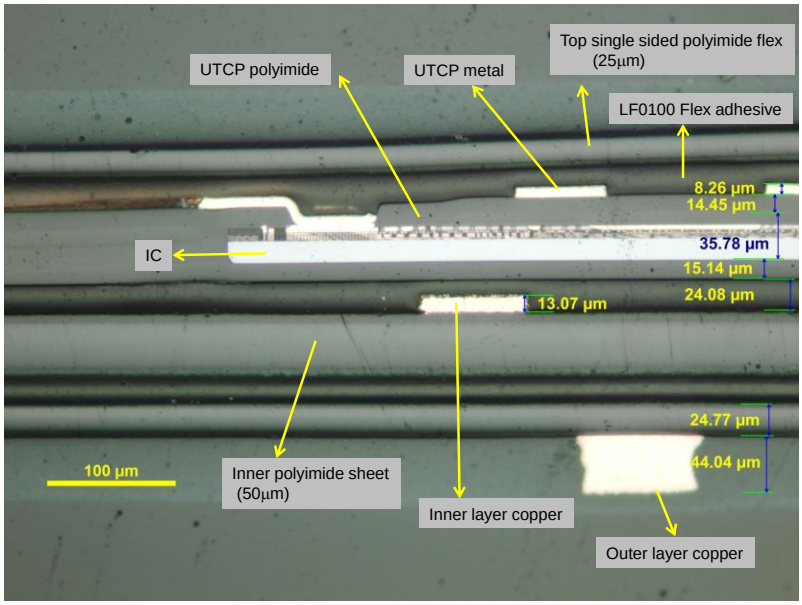

Figure 8: Cross-section of an embedded UTCP sample in 4-layer flex.

Conclusions

In previous work the concept of ultra-thin chip packaging was developed and demonstrated, as well as the feasibility of embedding such a polyimide based package into a flexible circuit board. In this contribution the process flows and embedding strategies have been altered with the aim of converting the lab-based experimental work into a process that can be transferred to a small fab. In order to demonstrate the yield of the improved process, 32 MSP430F1611 microcontrollers are packaged with a yield of 87.5%, and 16 proprietary DSP processor ASICs are packaged with a yield of 62.5%. For the packaged microcontrollers the new process flow resulted in a yield increase by more than 20%.

After selection of the know-good packages, the UTCP packages are embedded into a flexible circuit board using a flex build-up and production process which is based on commercially available FCBs. The yield of this embedding is 95%, based on a sample set of 20 UTCP packages.

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