


Foundry processes for silicon photonics

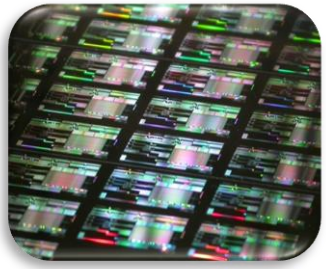
Pieter Dumon

7 April 2010

ECIO

ePIXfab

Prototyping



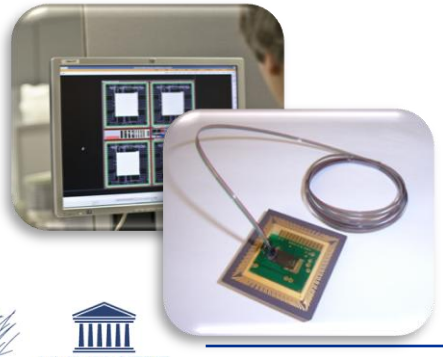
Multi project wafer access to silicon photonic technologies

- **share mask and process costs**
- **imec and LETI technologies**
- **for R&D/pre-commercial use**

Training

Basic training on ePIXfab technologies, design, and MPW operation

Supply chain



Access to supply chain:

- **design automation**
- **packaging**
- **manufacturing**

Outline

- Passive device technology & considerations
- Active device considerations
- Wafer testing
- Design
- Prototyping access

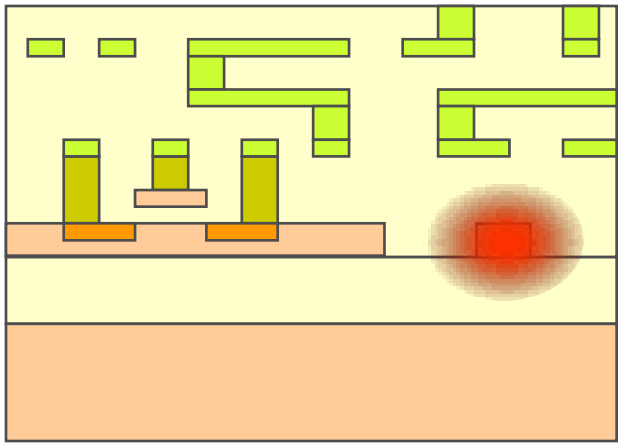
Acknowledgement

- Si photonics platform team Ghent Univ. & imec
  - Wim Bogaerts, Philippe Absil, Peter Verheyen, Hui Yu, Adil Masood, Shankar Selvaraja, Jin Guo, Pieter Dumon
- The photonics research group

PROCESS TECHNOLOGY

Options

- **Integration in existing CMOS process**
  - Today
  - Foundry MPW & manufacturing
  - Not built for photonics
  - May need some adaptations
  - Example:
    - Luxtera/Freescale



- **Custom process in your own fab**
  - Freedom
  - ~~€€€€€€€€~~
  - Example: Kotura

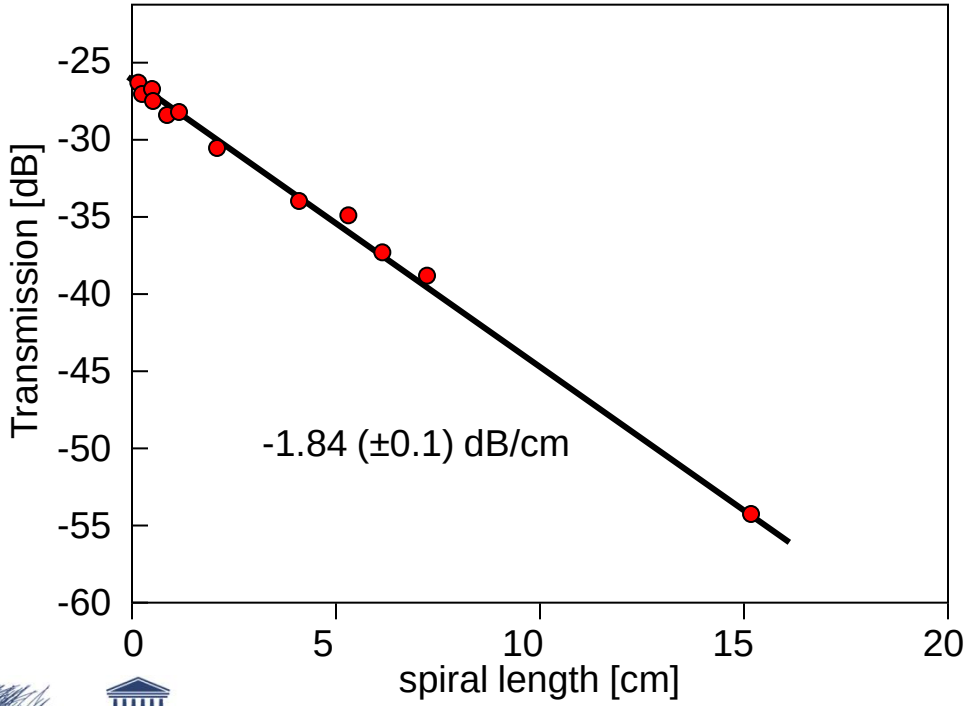
Options

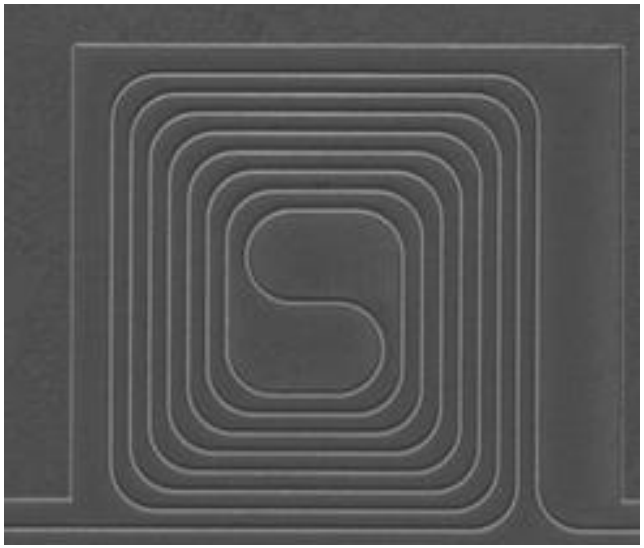
- **Semi-custom processes in standard fab**
  - **Today in MPW and LVM**
  - **Technology & PDK development by fab**
  - **Dedicated processes, transferable to foundry**
  - **Flexibility**
  - **Re-use as much as possible**
  - **Examples:**
    - **imec**
    - **LETI**

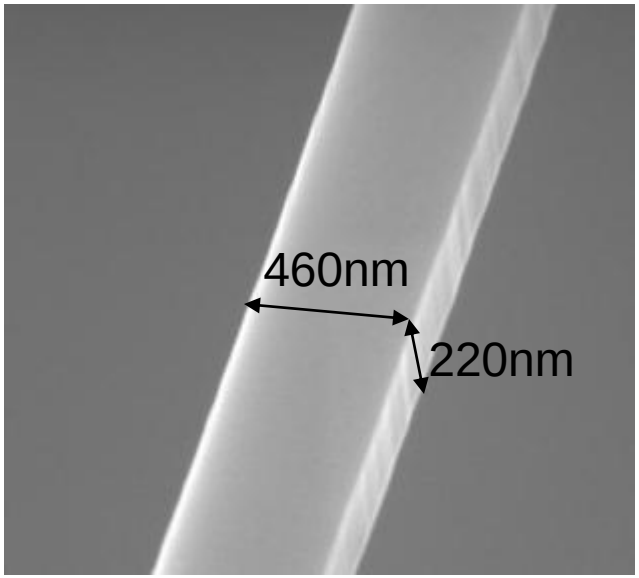
imec technology: waveguides

Etched wire in silicon

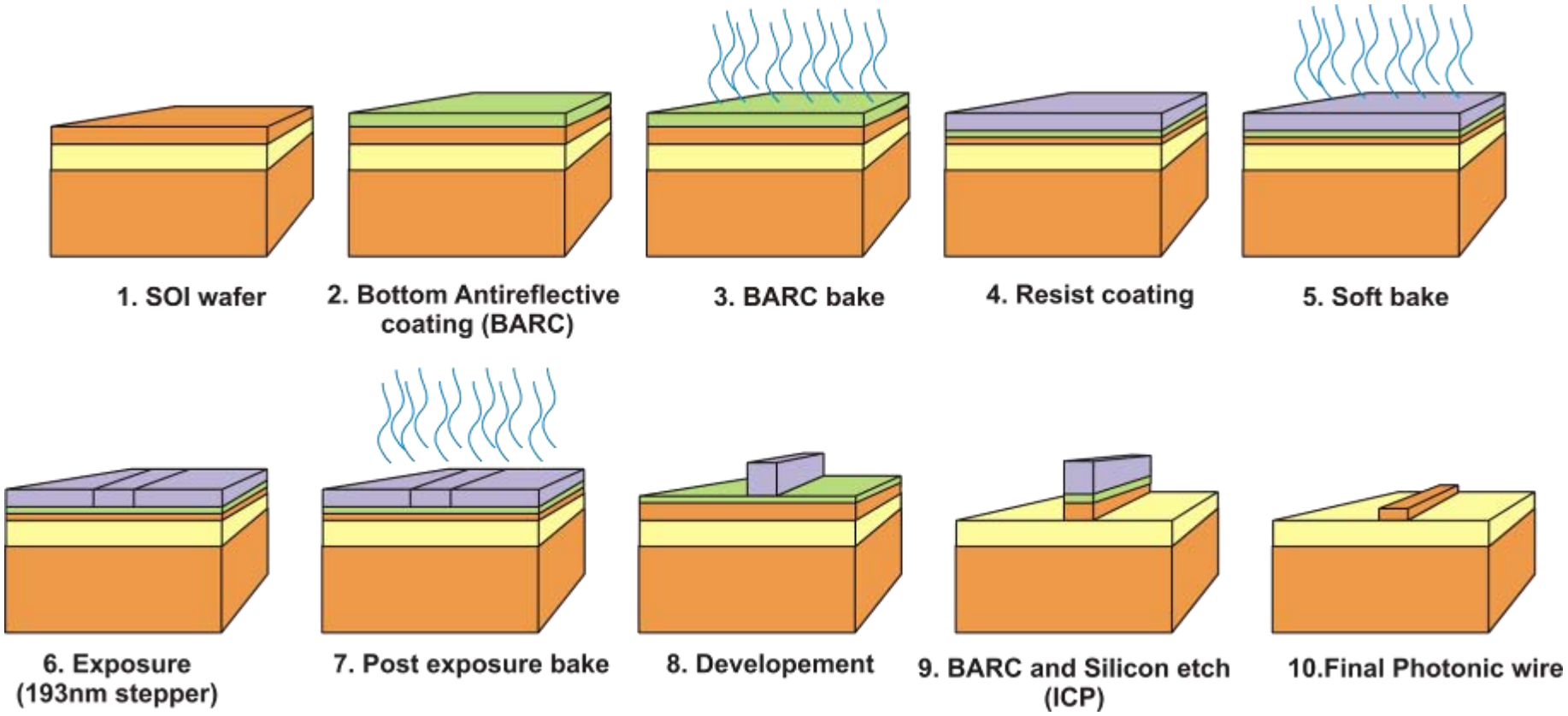
- 450 x 220 nm²
- straight loss: 1.84dB/cm
- bend losses ~ 0.01dB/90° (3µm radius)







Waveguide module



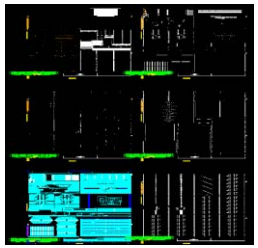
S.K. Selvaraja, JLT 27, p.4070 (2009)

Mask technology

- CMOS reticles: 0.13um, 0.18um
- 5nm design grid
- 4X reduction litho
- Design rules
- Min feature size: 100nm (0.13um tech)
- Designers deliver GDSII data
- Fracturing (MEBES data)

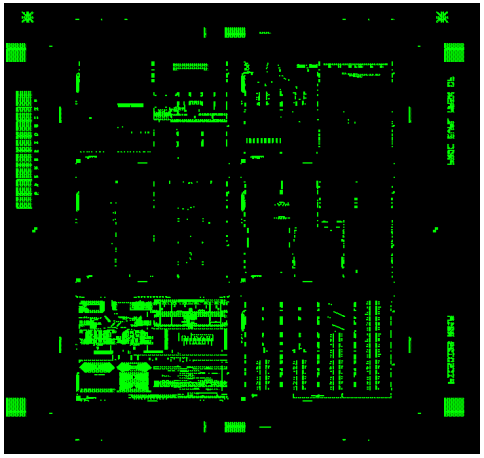
10-30 designs

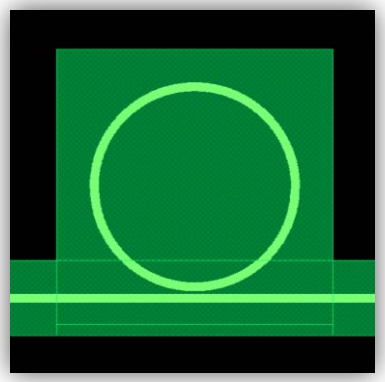
Geometric design data



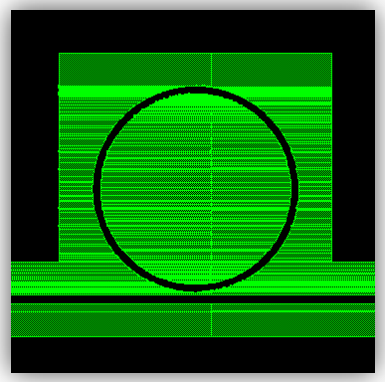
4X

maskshop data



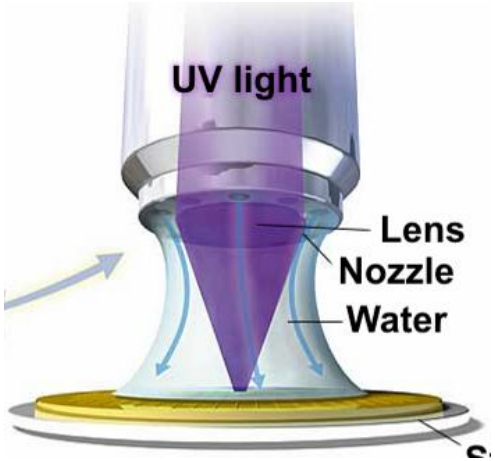


Fracturing



Increasing resolution

$$\text{Resolution} = k_1 \frac{\lambda}{NA}$$



Decrease illumination wavelength

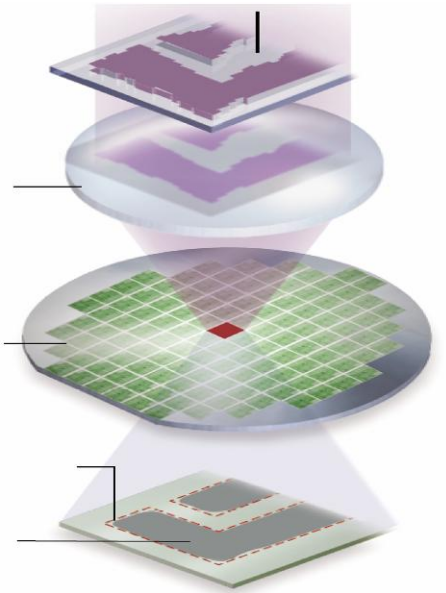
- 365nm → 248nm → 193nm → 157nm → 13nm

Increase numerical aperture

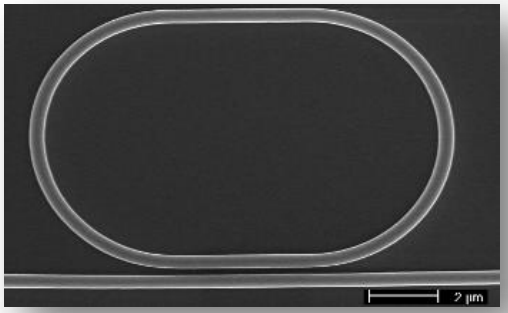
- larger lenses → 0.85
- immersion: $NA = n_{medium}.\sin\theta_{max}$

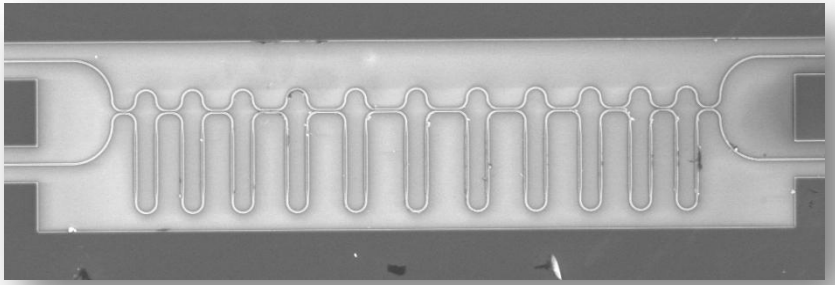
Technology Factor

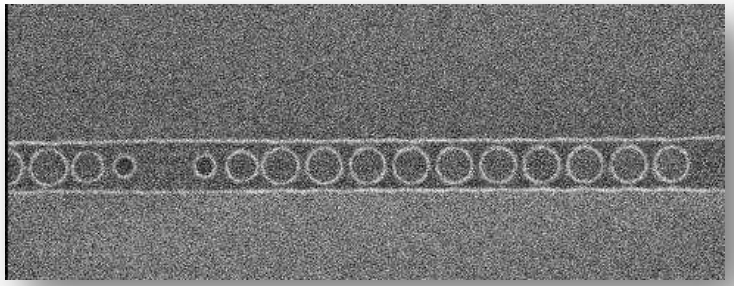
- light source (coherency, off-axis illumination, ..
- mask technology (phase shifting masks)
- mask correction (assist features, OPC)

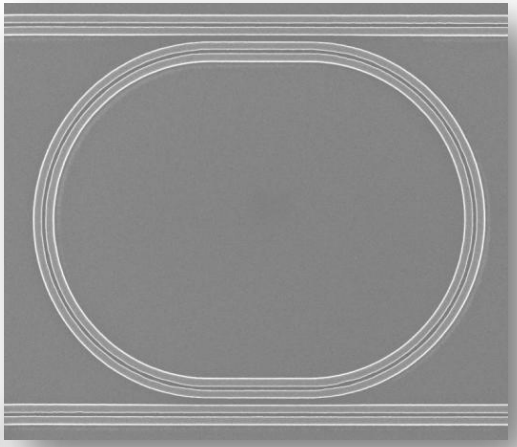


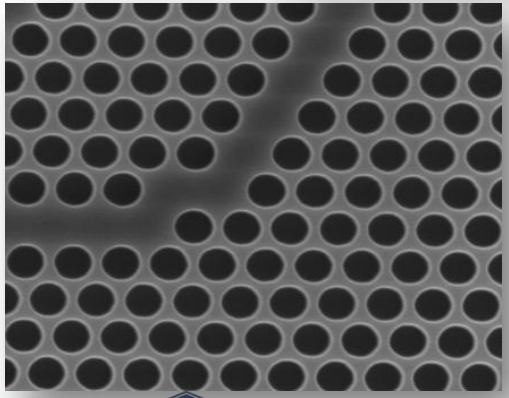
imec technology: waveguides

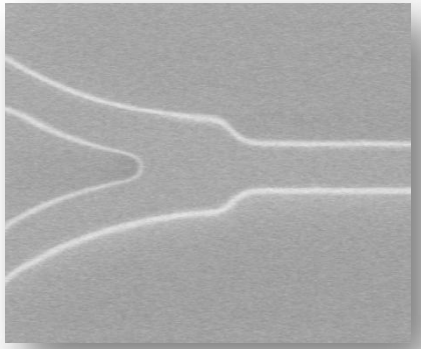












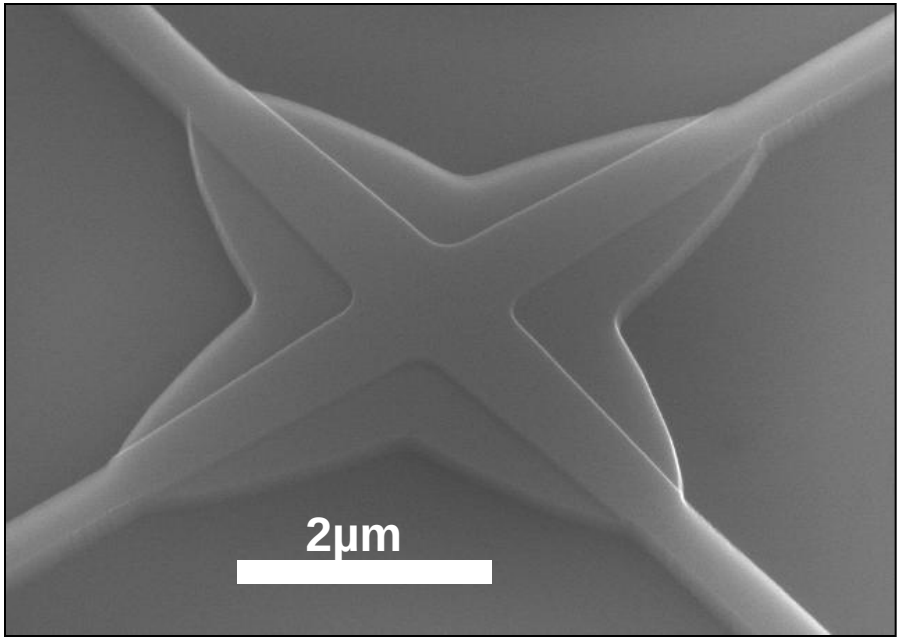
imec technology: shallow etch module

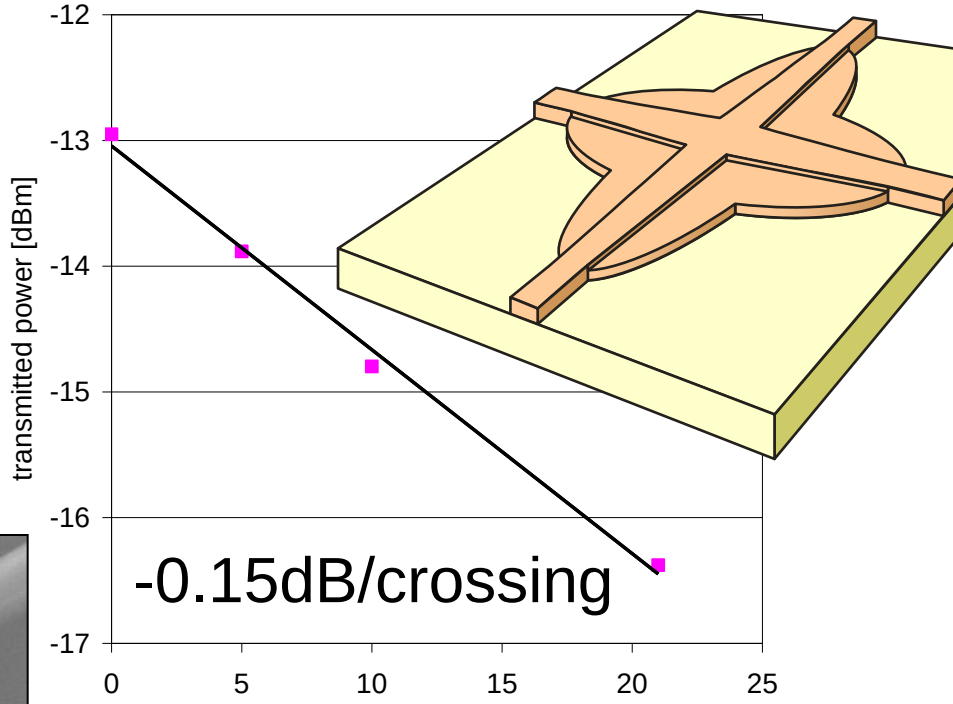
Deep & Shallow etch

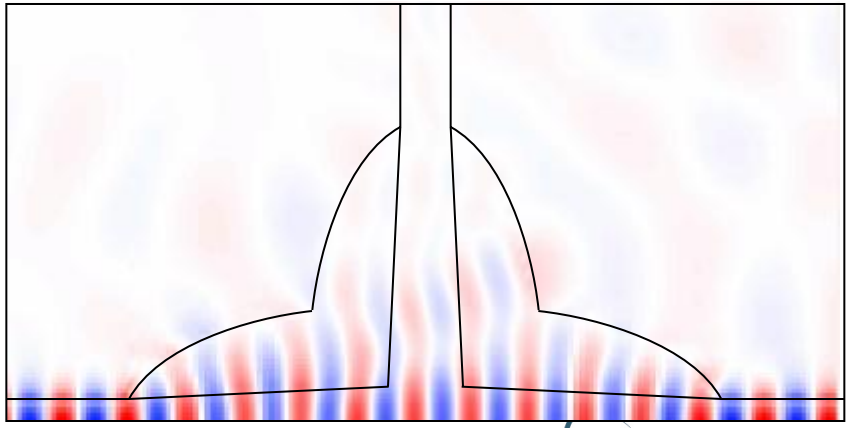
- reduce contrast locally
- keep light confined
- flatten phase fronts

-0.15dB loss per crossing

-40dB crosstalk







W. Bogaerts, OL 32, p.2801

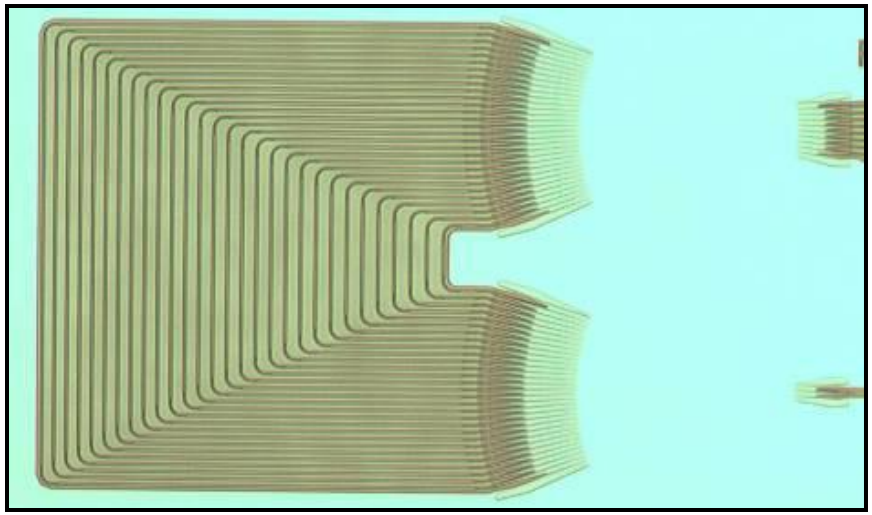
Arrayed Waveguide Grating

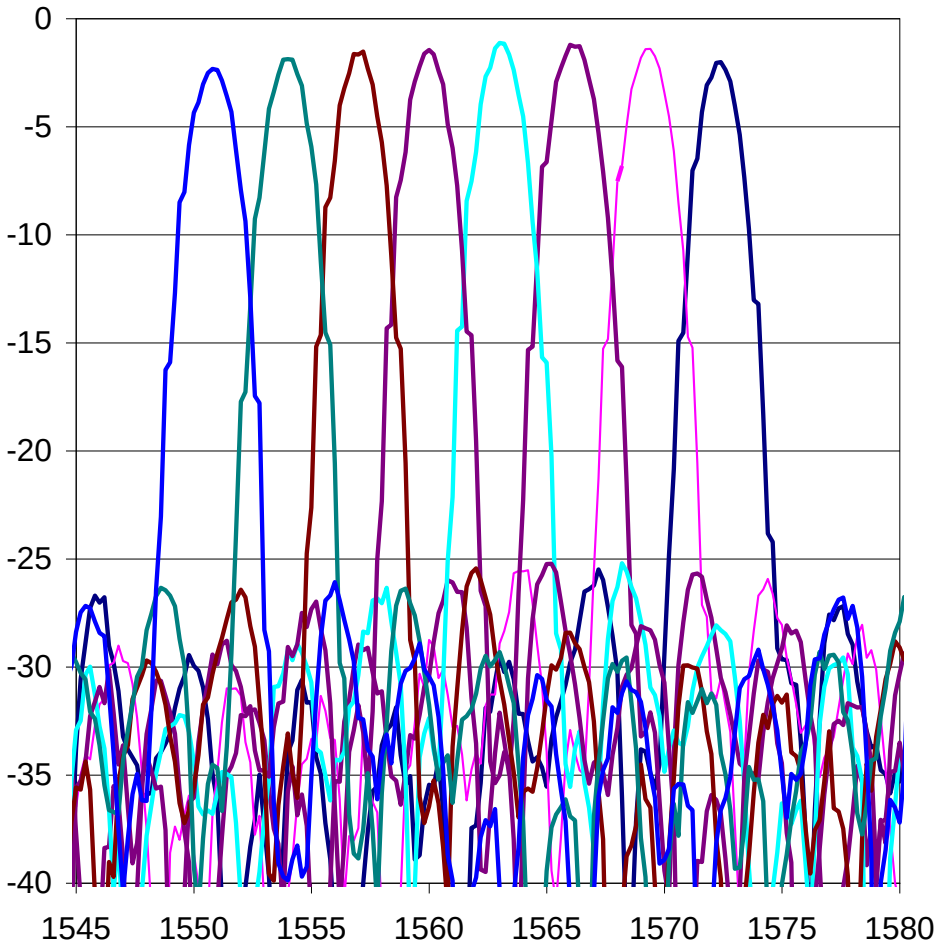
8-channel, 400GHz

FSR = 30nm

footprint = 200 x 350 μm²

- **-25 dB crosstalk level**
- **-1 dB insertion loss (center channel)**
- **1.5 dB non-uniformity**





W. Bogaerts, JSTQE (to be published)

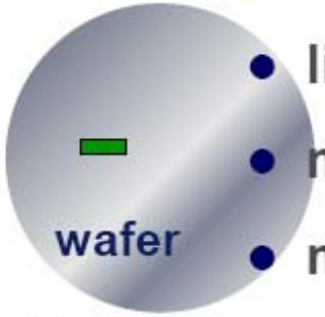
Reproducibility

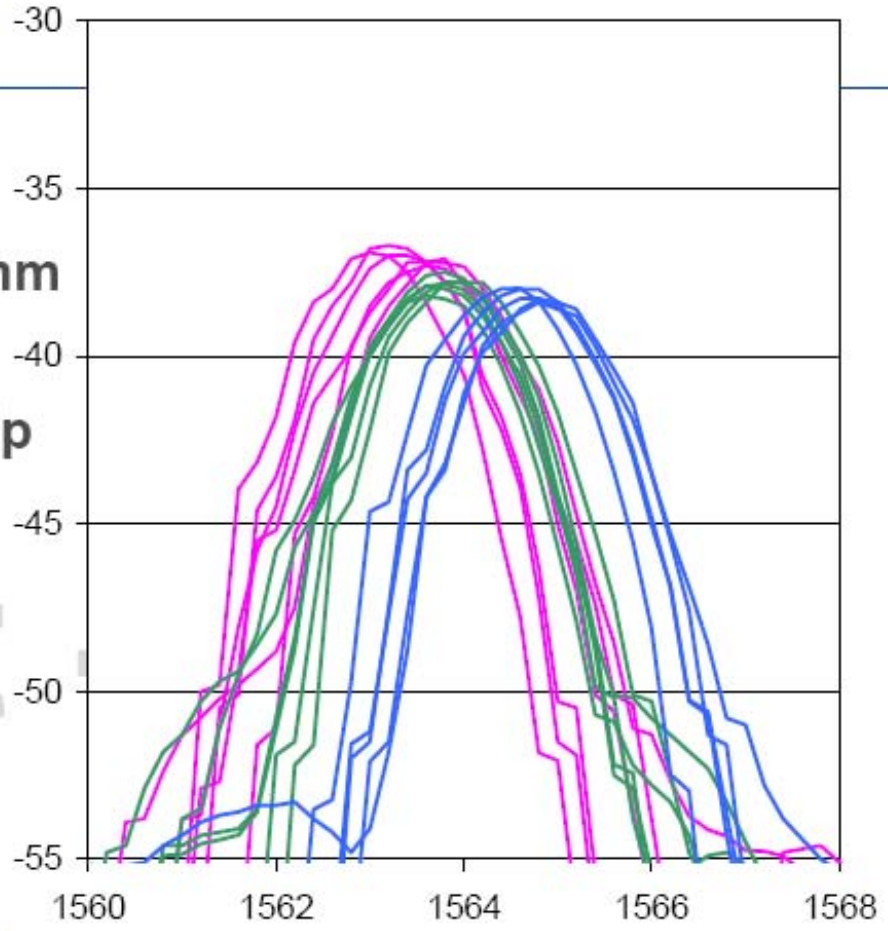
18 identical AWGs

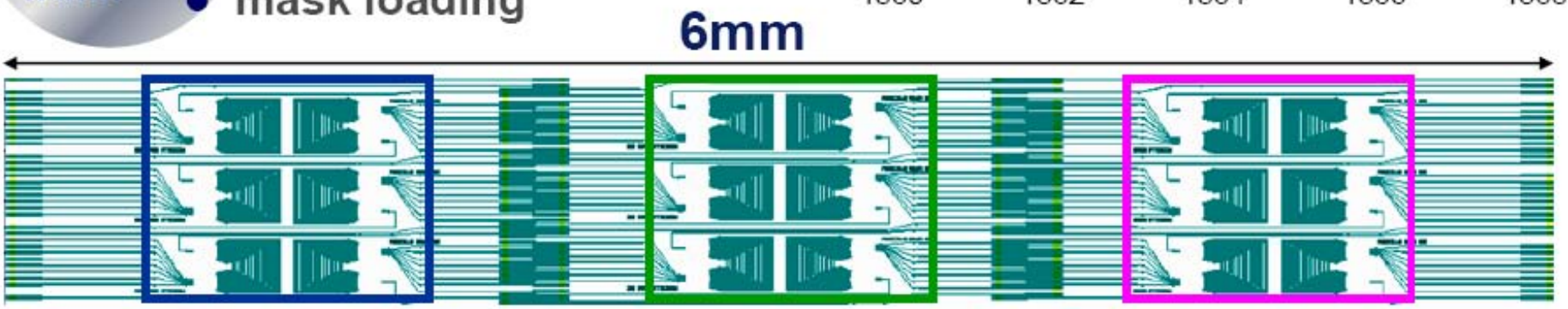
- shift in channel peak ~ 2.5nm
- strong correlation with location of the AWG on chip

Possible causes

- center-to-edge on wafer
- lithography scanning
- mask fabrication
- mask loading



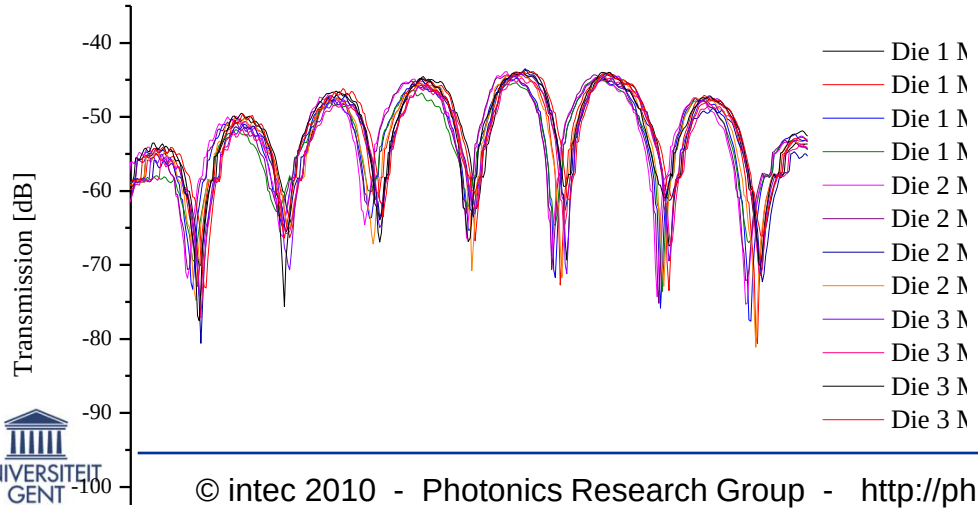


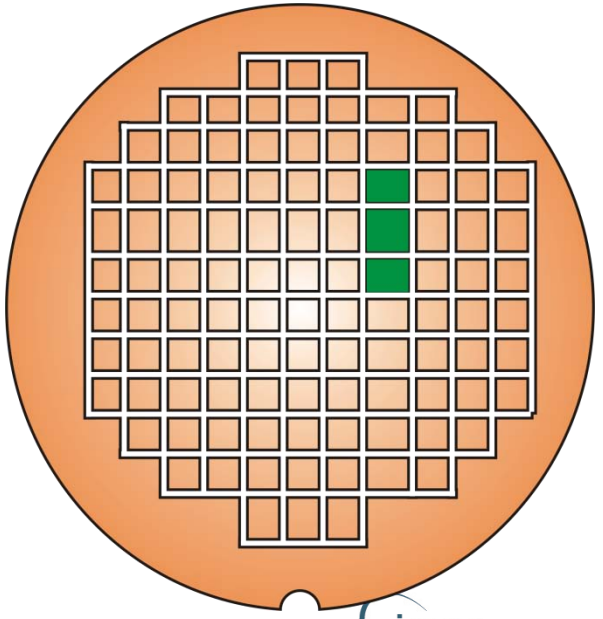


Die to die uniformity

- **Long range (few 10's of mm) – device width and height**
- **Non-uniformity source – Litho, Etch, Wafer**

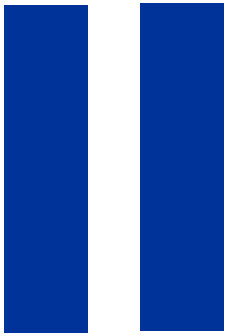
Distance between the devices (Die-to-Die)	Average resonance wavelength shift obtained (3 chips/12 devices)		Smallest resonance Wavelength shift obtained	
	Ring resonator	MZI	Ring resonator	MZI
10,000mm	**1.3nm**	**1.08nm**	0.1nm	~0nm
20,000mm	**1.8nm**	**1.73nm**	1.5nm	1nm



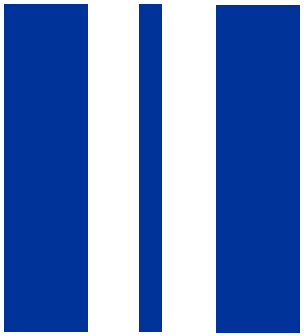


Dose to target

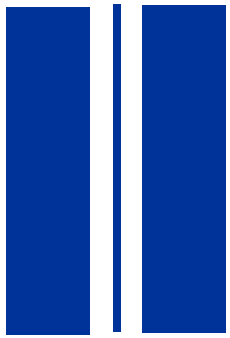
- **Each feature has a different dose-to-target**



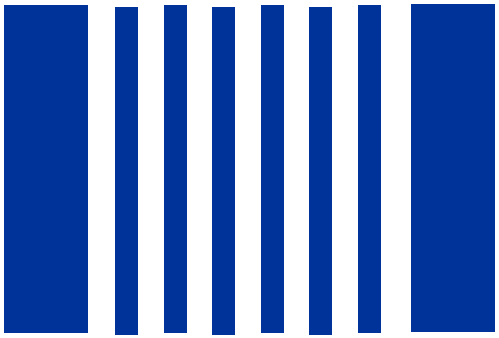
iso line



line pair
(coupled WGs)



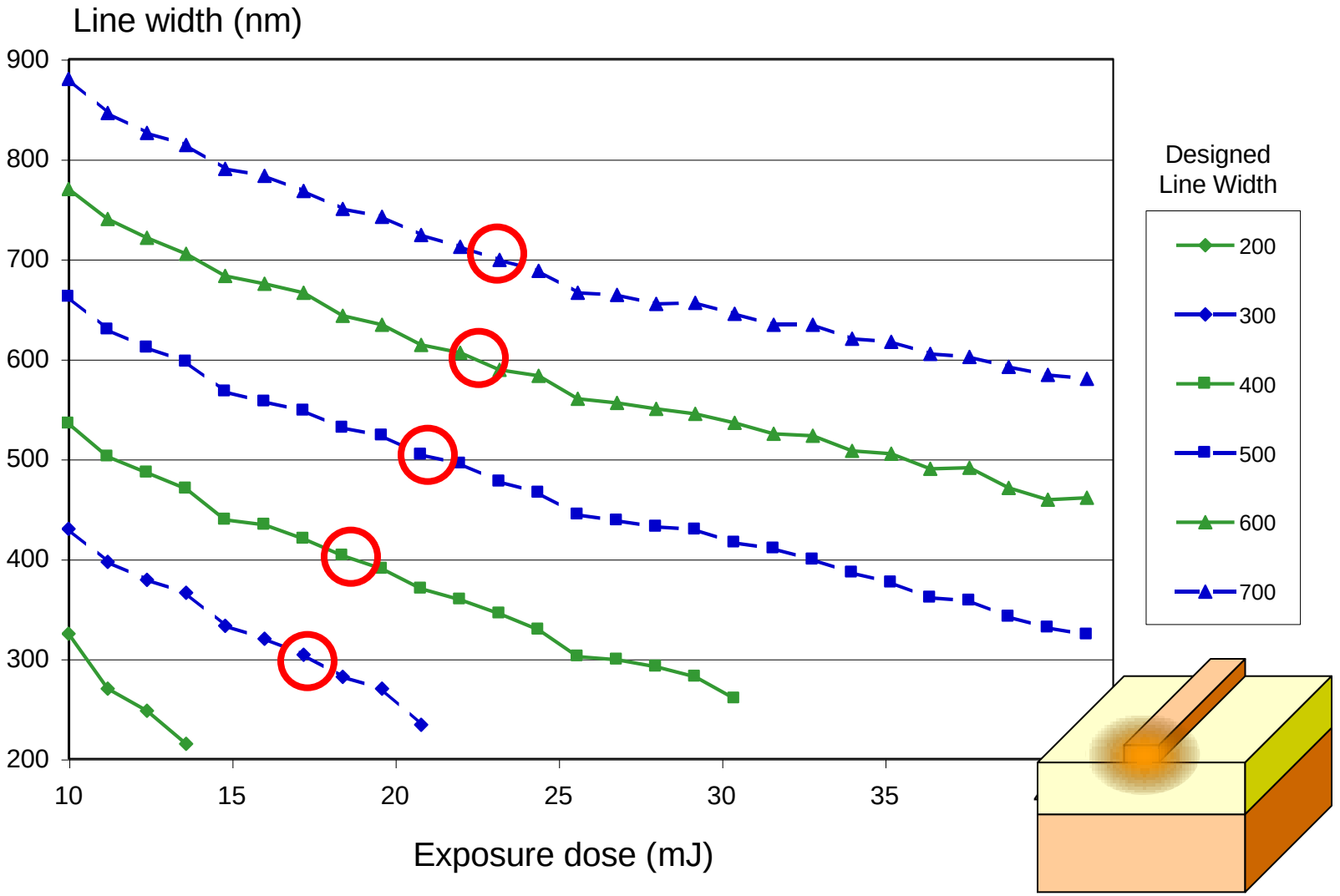
dense line pair
(slot waveguide)



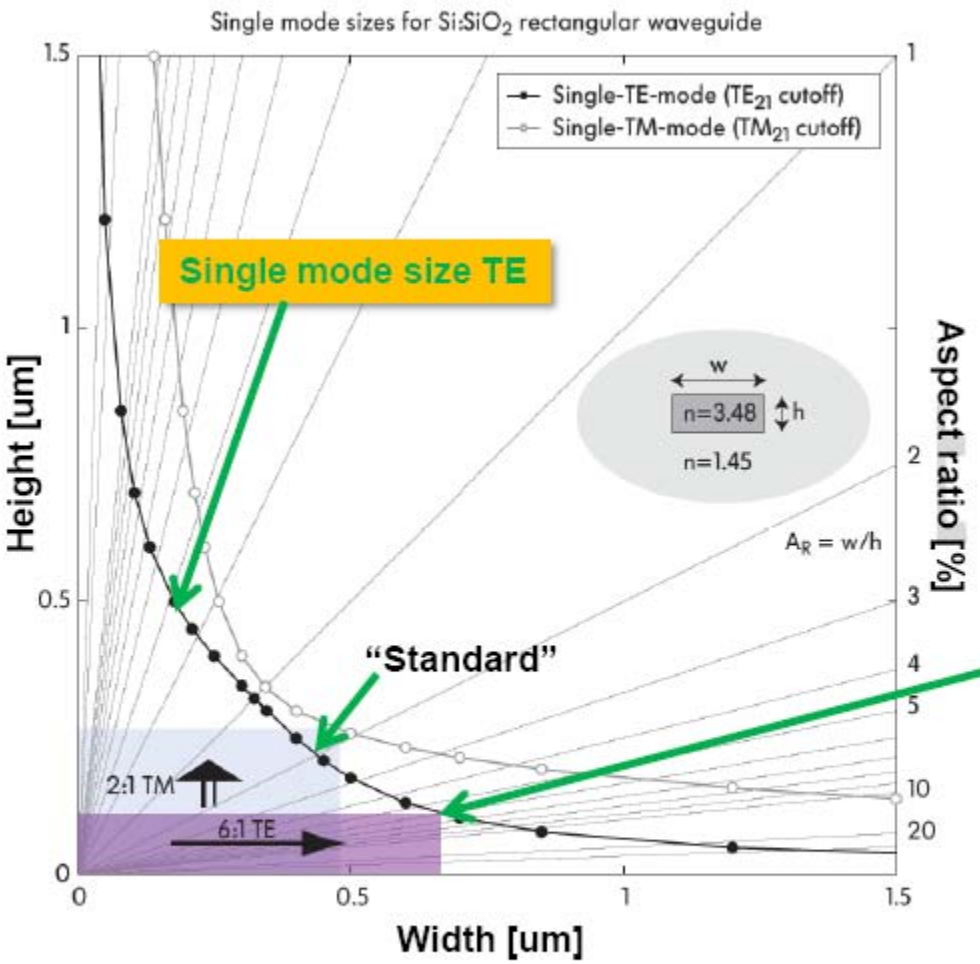
dense lines

dense holes

Line width with exposure dose



Waveguide dimensions



Popovic, PhD Thesis, MIT (2008) (http://dspace.mit.edu)

Question:

- Given certain optimization criteria
- What is optimal aspect ratio for waveguide ?

Popovic e.a. :

- Optimisation for:
  - Low loss,
  - Low sensitivity to dimensional variations
  - High thermal optic effect
- Choose AR = 6:1 !!!

Alternative optimisation criteria:

- High non-linear effects

  Vaillitis, Leuthold, e.a. OE 17 pp. 17357 (2009)

- Optimized sensing (overlap with outside world)

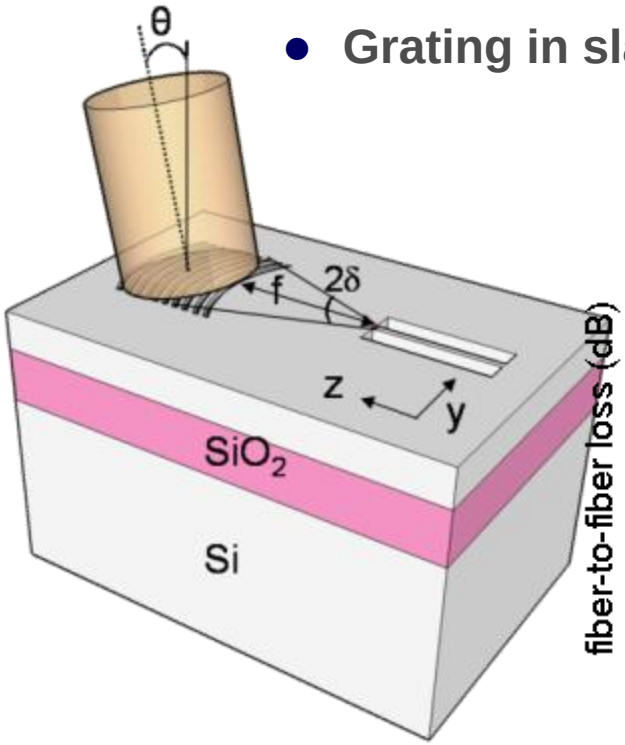
  Debackere, PhD thesis UGent (2010)

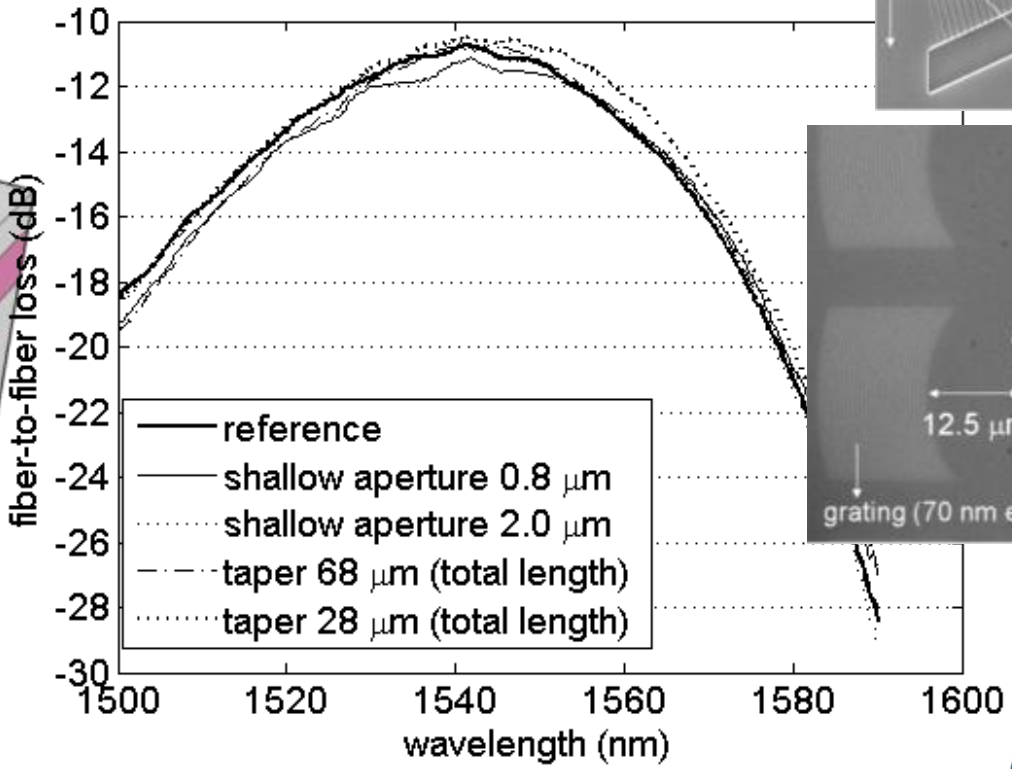
- Dispersion

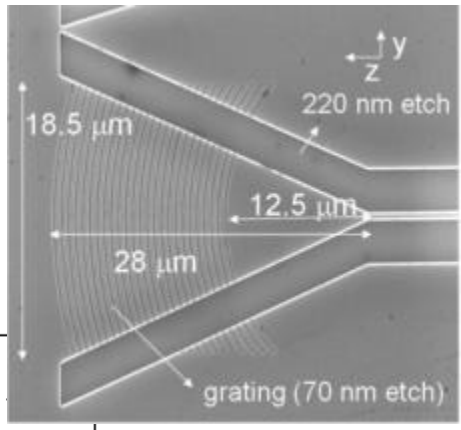
Focusing grating couplers

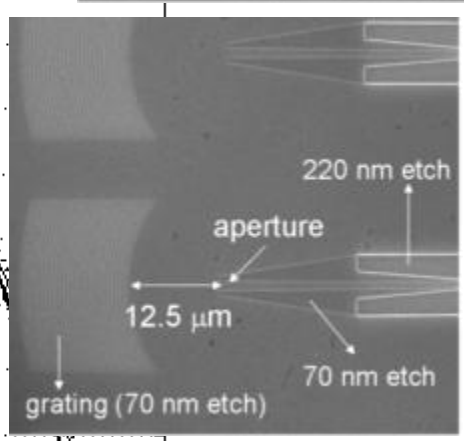
Curved gratings: focus light in submicron waveguides

- No adiabatic transition needed
- Grating in linear taper
- Grating in slab, focus on low-contrast aperture









F. Van Laere, PTL 19, p. 1919 (2006)

High-efficiency Fiber I/O

Grating coupler with locally thicker Si

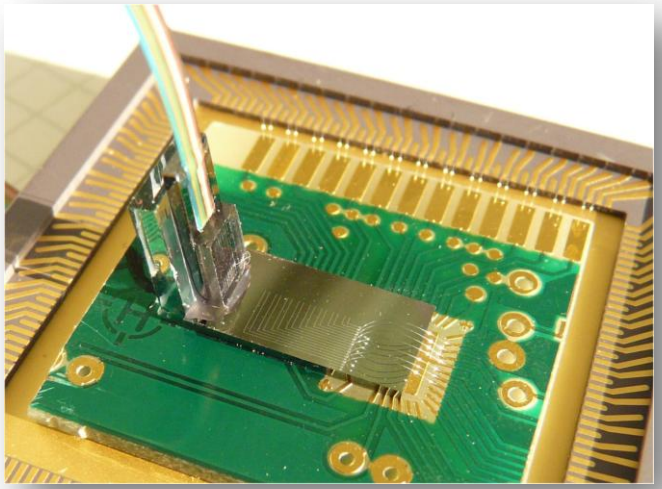
More complex process required

Low loss

Limited bandwidth (40nm 1dB)

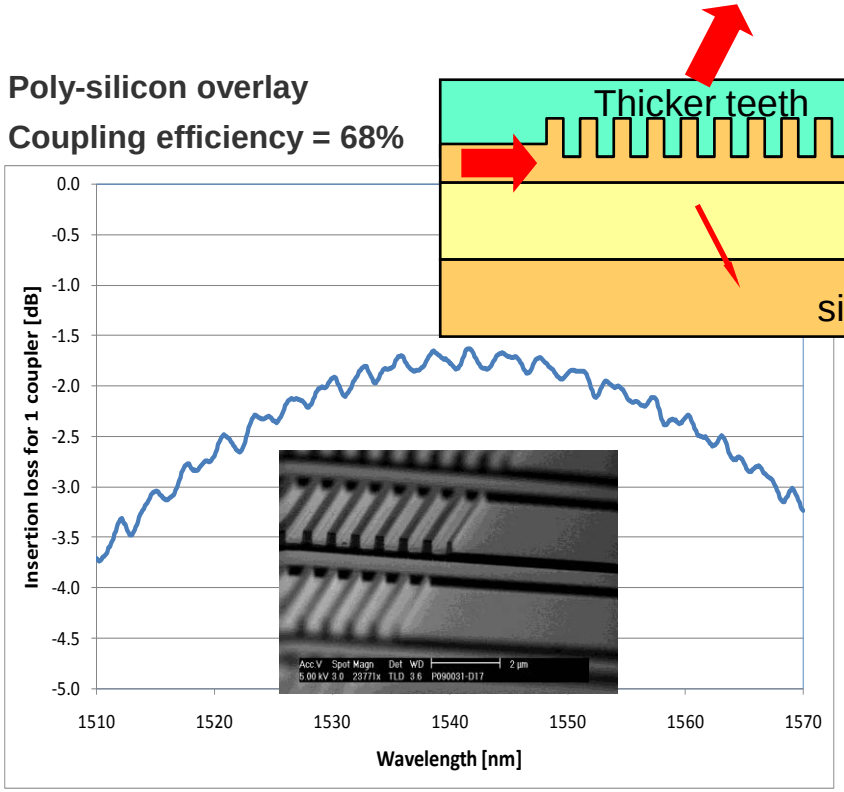
Novel packaging required

Wafer scale testing!



Poly-silicon overlay

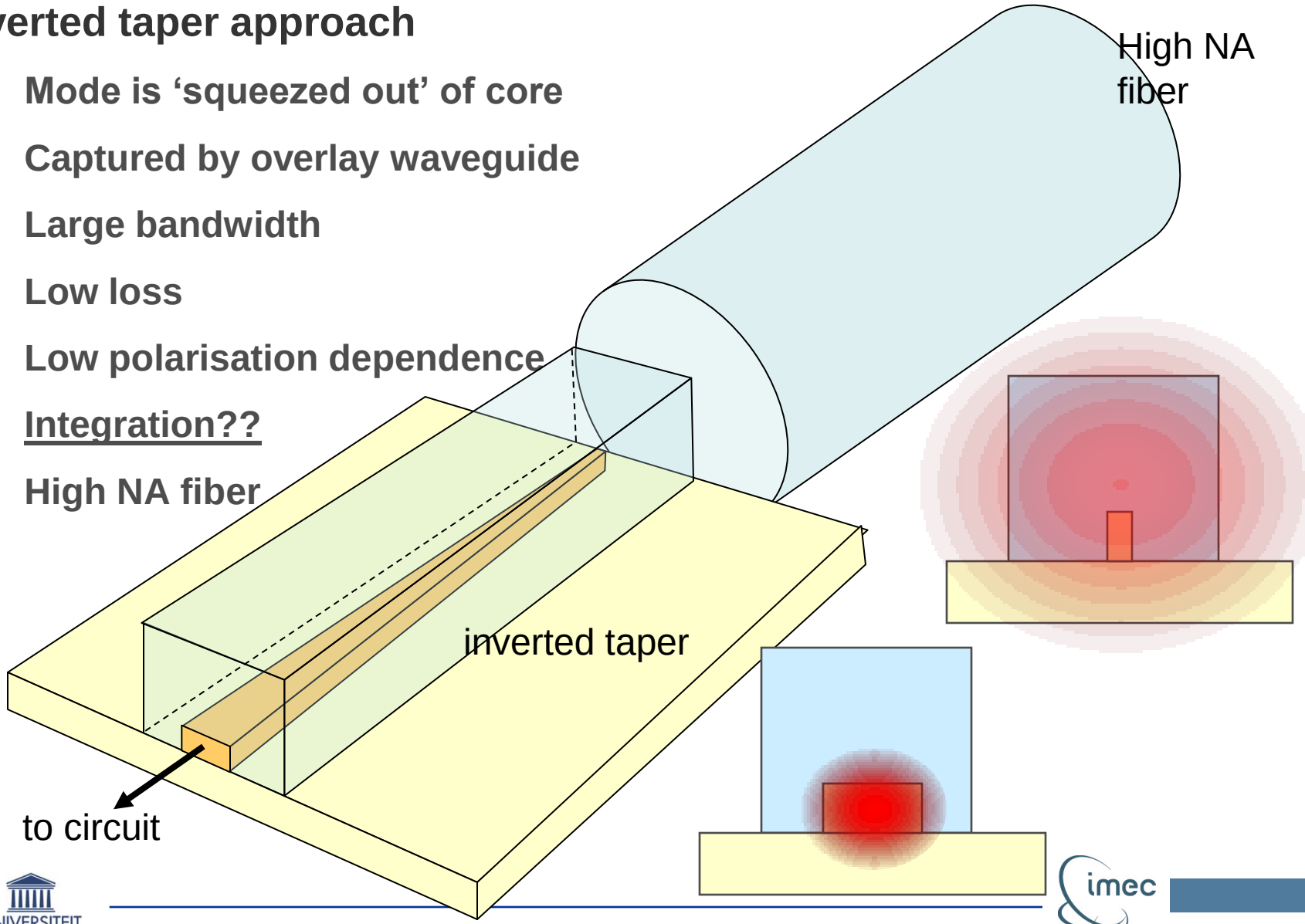
Coupling efficiency = 68%



High efficiency fiber I/O

Inverted taper approach

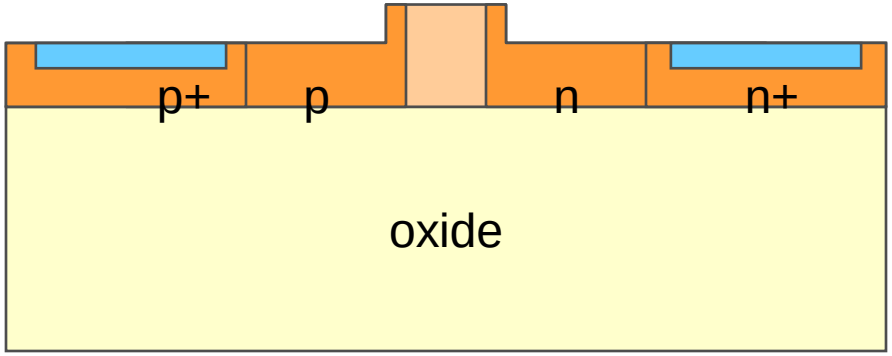
- Mode is ‘squeezed out’ of core
- Captured by overlay waveguide
- Large bandwidth
- Low loss
- Low polarisation dependence
- Integration??
- High NA fiber

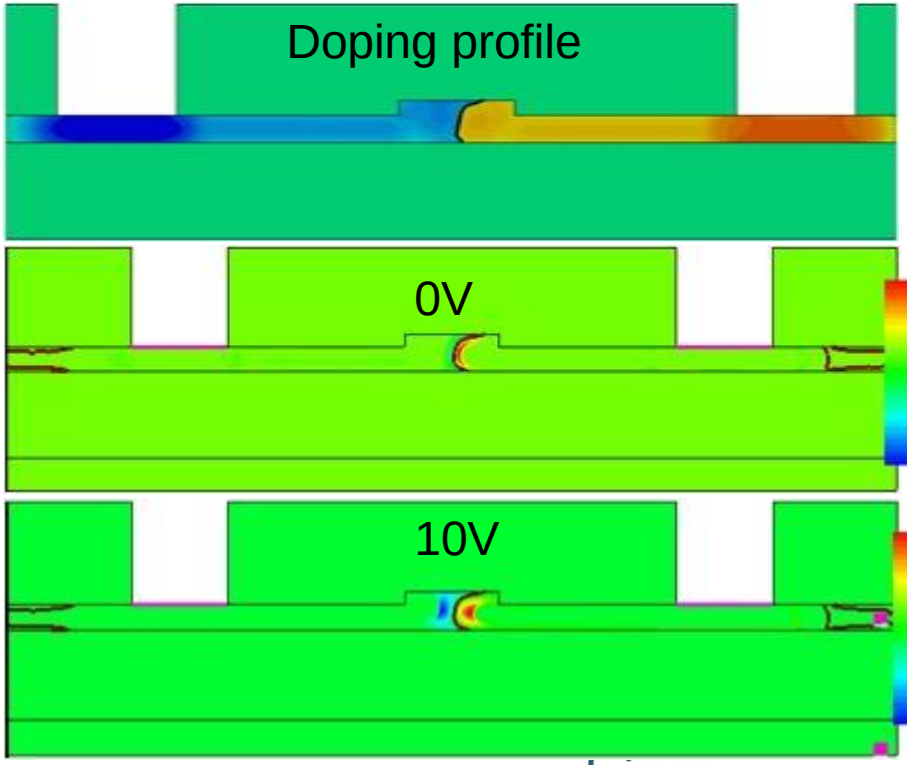


Carrier dispersion modulators

Create lateral p-n junction in the waveguide

- carrier injection changes refractive index
- lateral or vertical
- doping also causes absorption



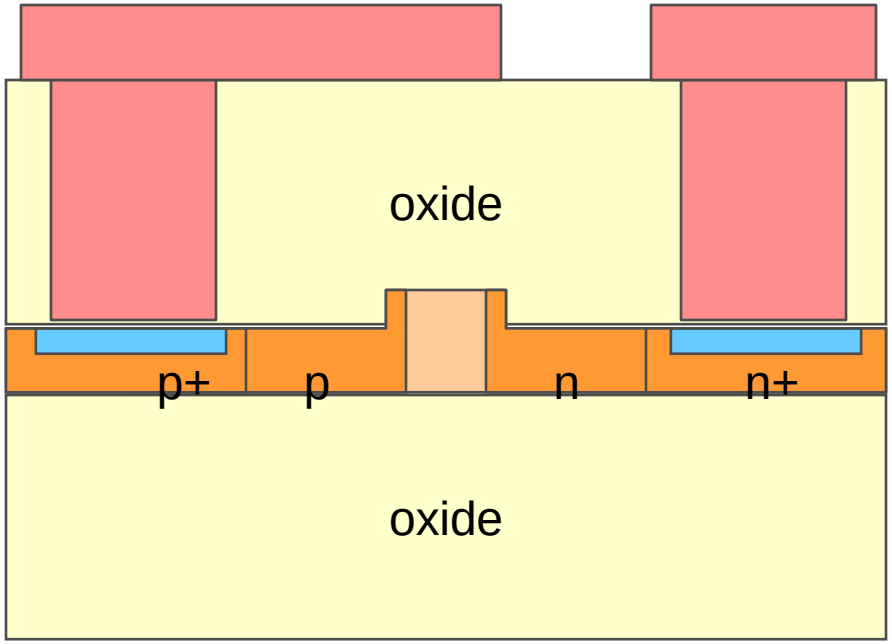


Contacting

- Need sufficiently thick top oxide (PMD)
- PMD thickness in 0.13-0.18um process: ~500nm

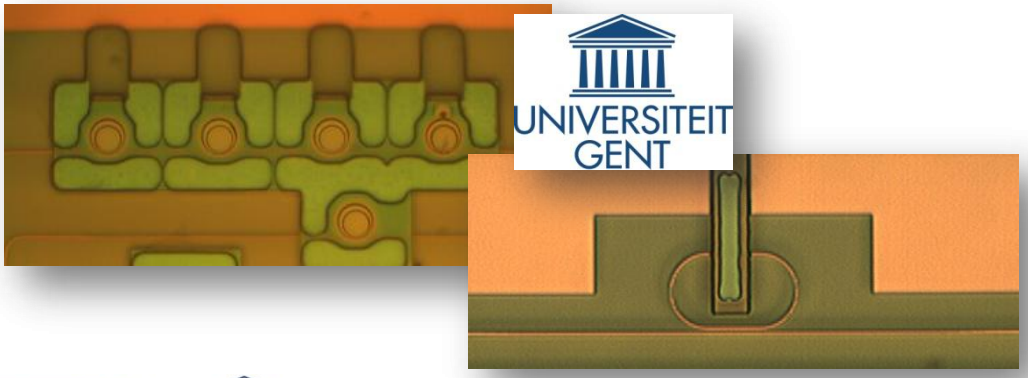
→ custom contact module with very different contact aspect ratio

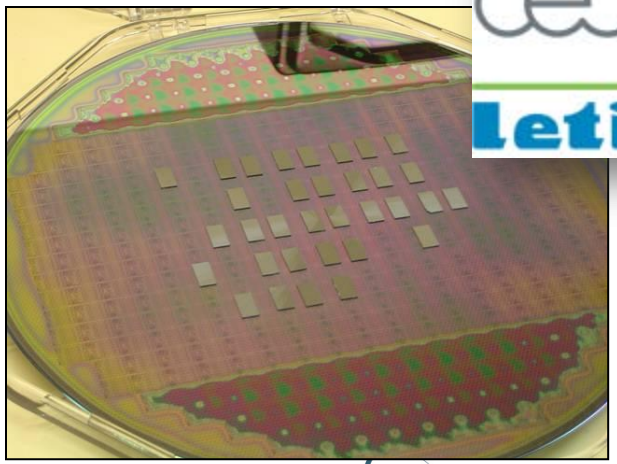
- Inverted taper fiber I/O with thick cladding: integration challenge



Active devices

- Detectors & sources
  - Ge
    - Detectors
    - maybe sources (exploratory work)
  - III-V
    - Sources, detectors, modulators, switches, λ convertors, flip-flops, …
- III-V on Si integration on wafer scale?
  - Yes
  - Take care of contamination, contacting, integration
  - Today on chip scale and being scaled up

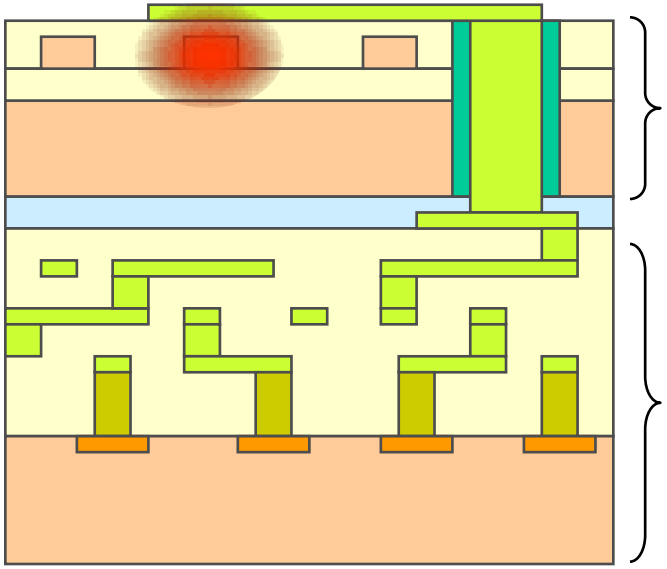


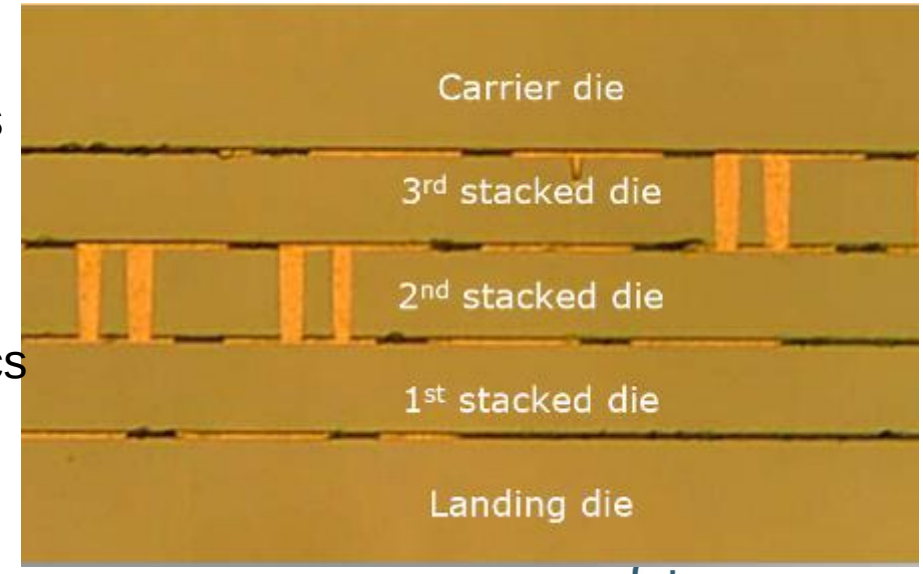


3D chip stacking

Technology in advanced stage

- Commercial 3D processes available
- imec: thin chip stacking
- ‘Cu nail’ TSV





Public offering

All of this in a process that:

- **can be maintained**
- **can be monitored**
- **has sufficiently low cost for a given volume**
- **allows MPW implementation**
- **we can make a design kit for**

WAFER TESTING

Wafer testing

Test structures for process monitoring/qualification

- **What to measure?**
- **How to measure?**

Wafer testing: testsuite

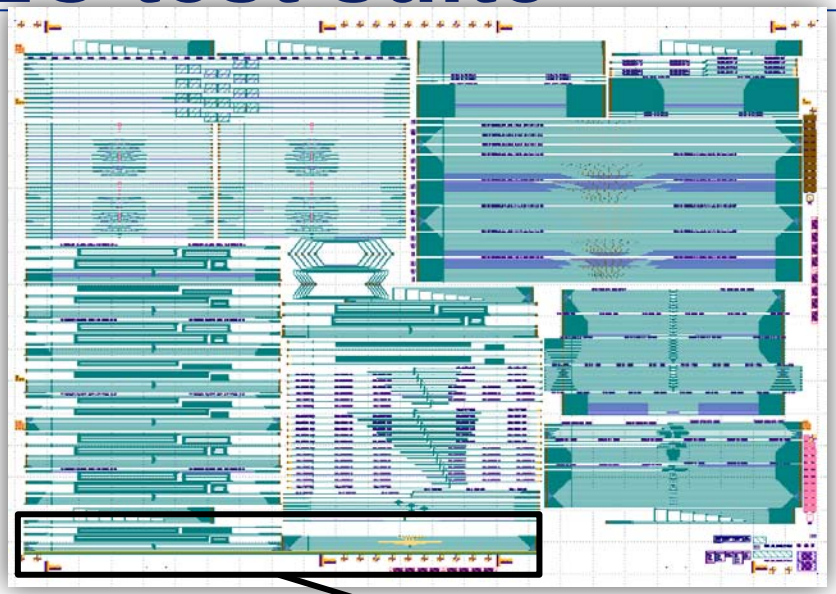
Structure metrology

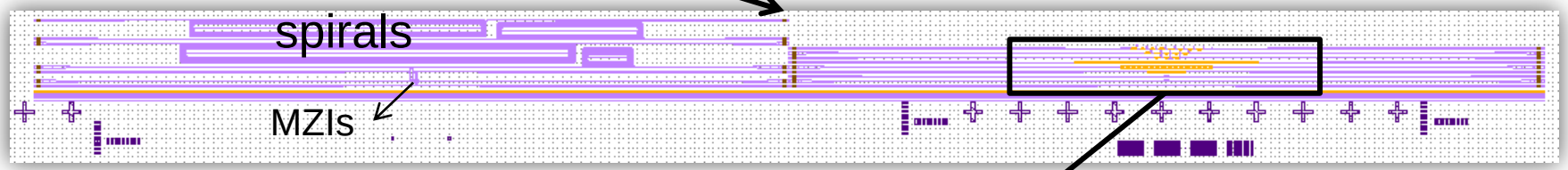
- standard waveguide width
- standard coupler width/gap
- …

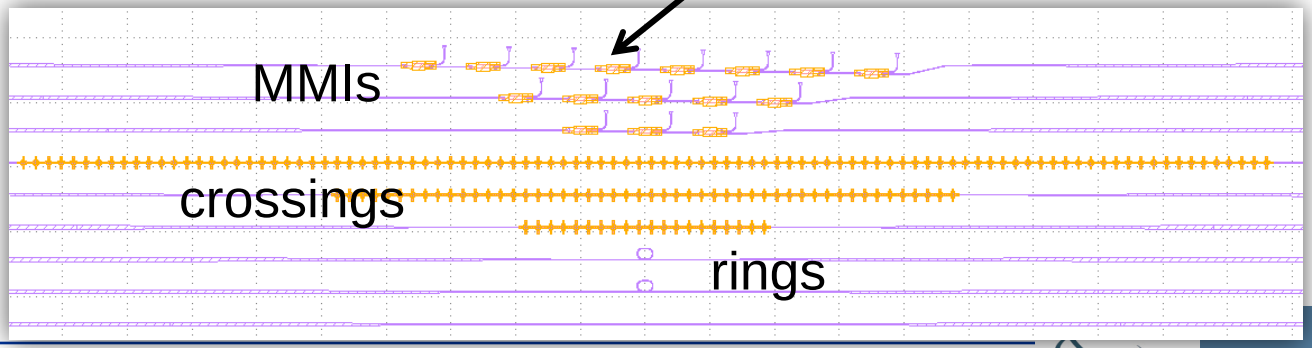
Optical test structures

- waveguide losses
- fiber I/O efficiency
- standard filter characteristic (e.g. ring resonator)
- standard p(i)n junction performance
- …..

IMEC test suite

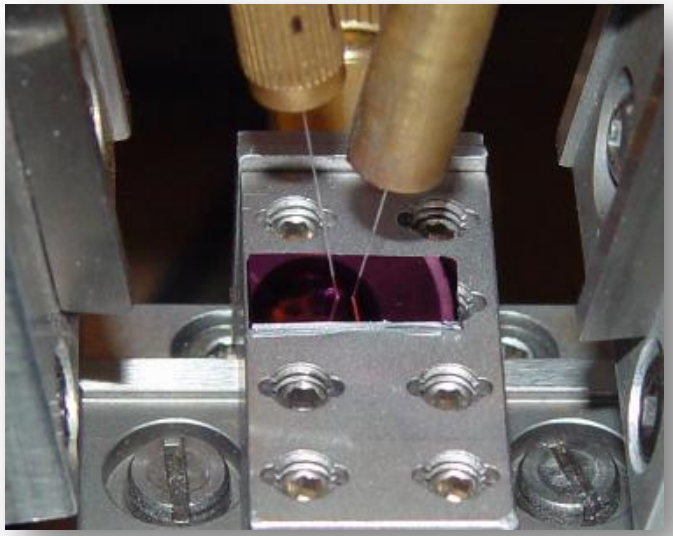






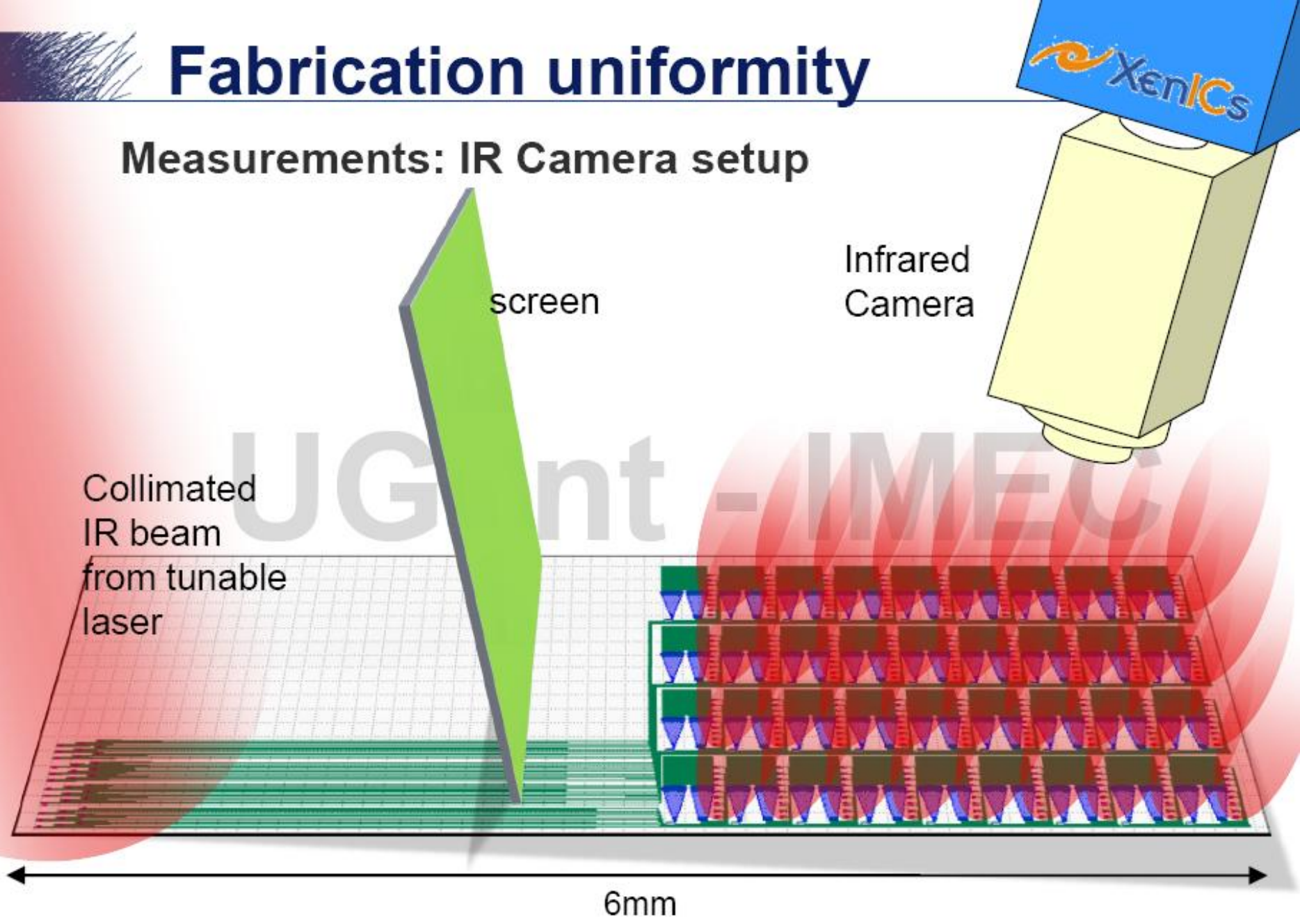
How to measure

- **Probe station**
- **Vertical fiber I/O**
- **Cost-effective or robust probes:**
  - **Standard single mode fibers (flexible use)**
  - **Fiber arrays (robust, multi I/O address)**



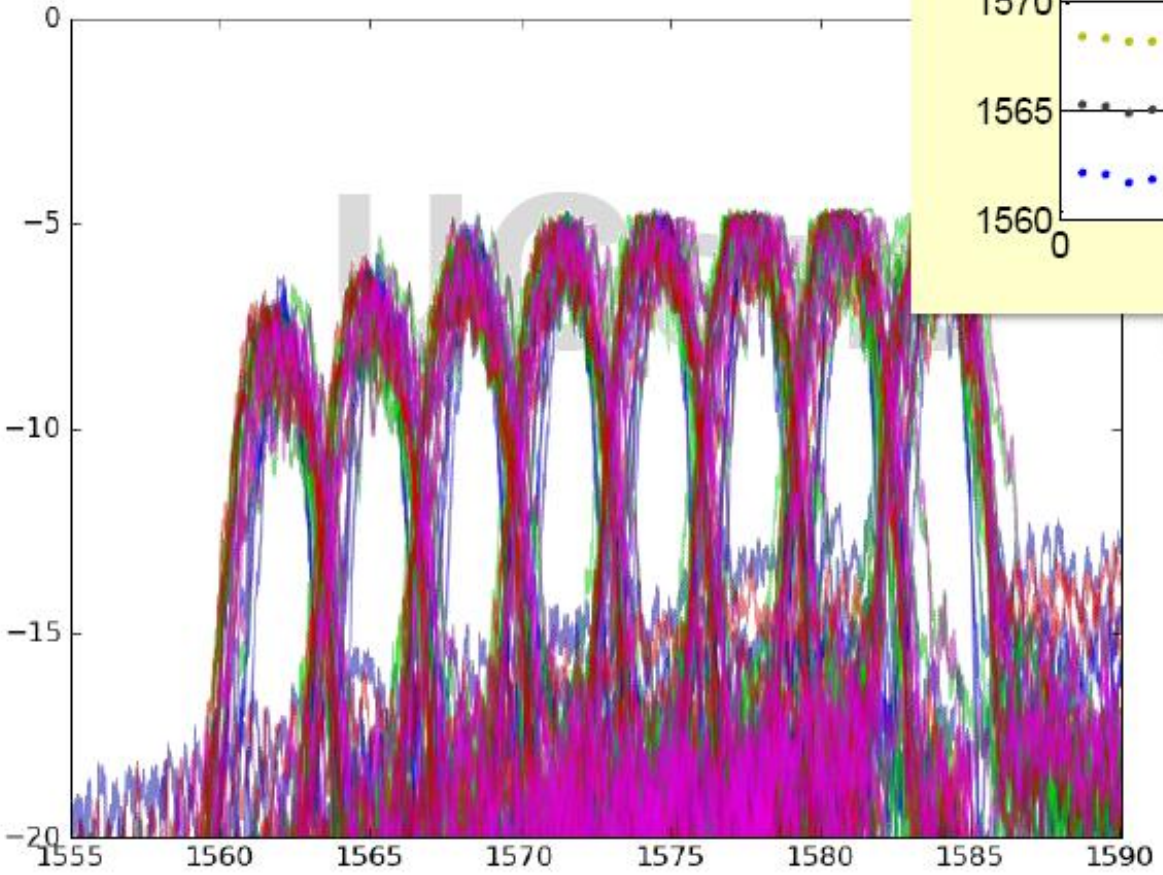
Fabrication uniformity

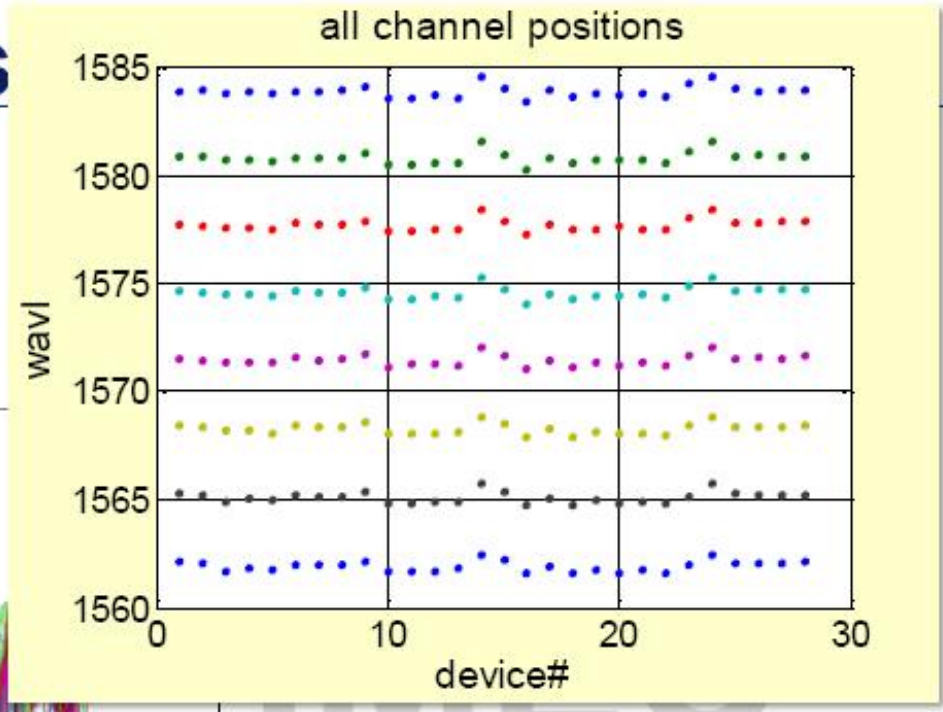
Measurements: IR Camera setup



Measurements

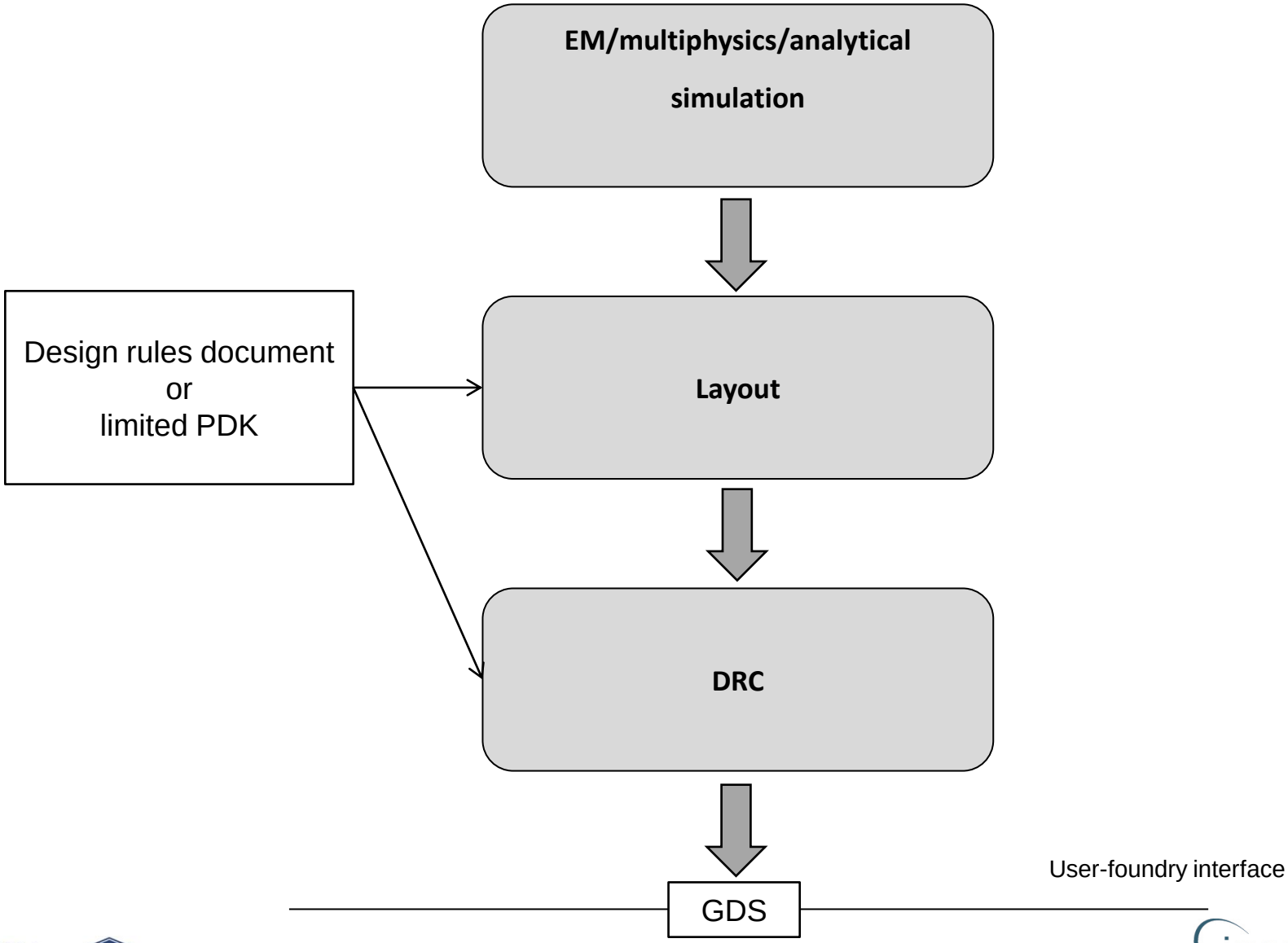
All rows



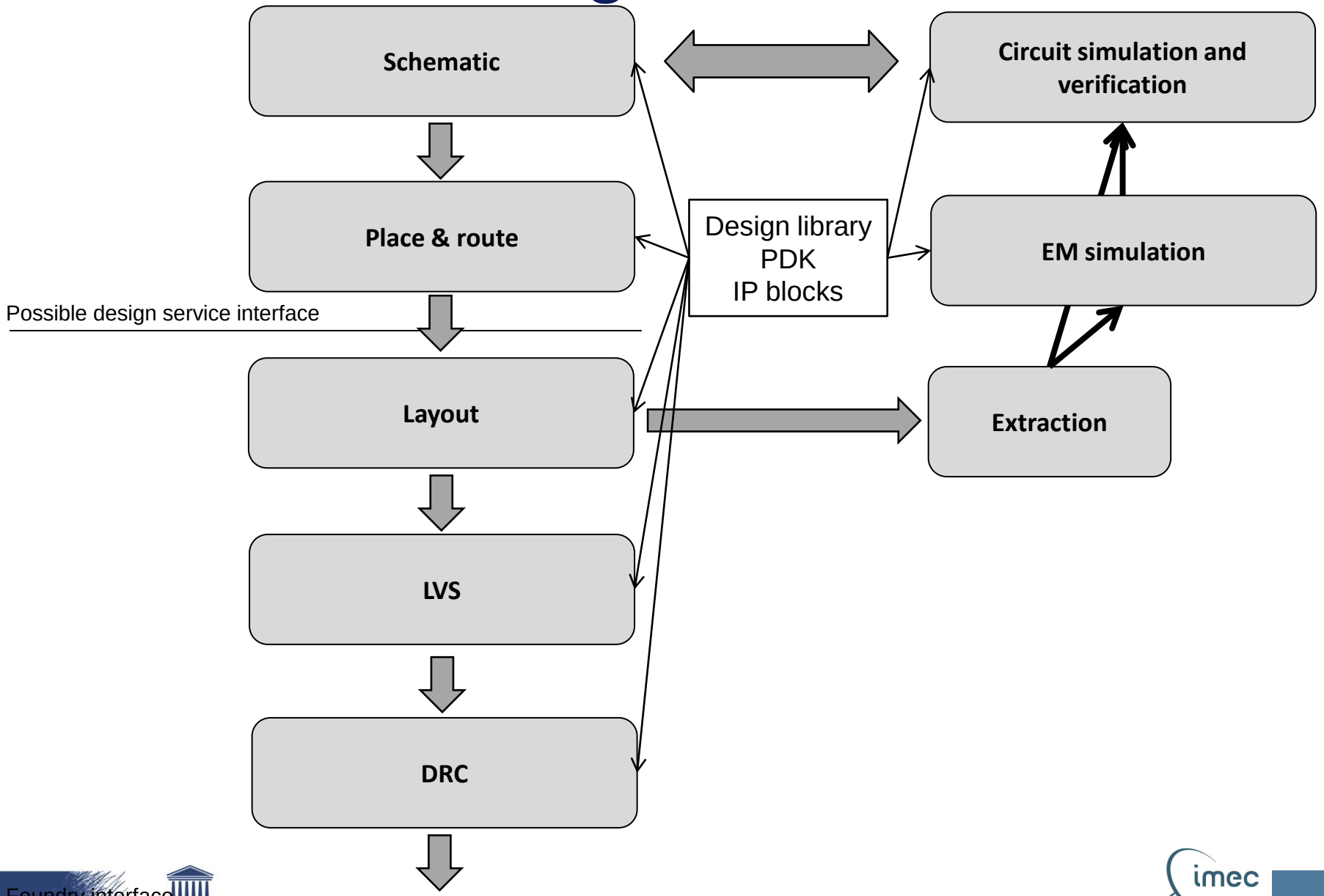


DESIGN

Design flow


EM/multiphysics/analytical simulation
Design rules document or limited PDK
Layout
DRC
GDS
User-foundry interface

Future design flow



Design automation

EM Simulation

Photon Design

RSOFT Design Group

PhoeniX Software for micro- and nano technologies

Optiwave

Circuit simulation

Photon Design

Optiwave

Aspic design

Layout

DESIGN WORKSHOP TECHNOLOGIES

PhoeniX Software for micro- and nano technologies

Tanner RESEARCH

cadence

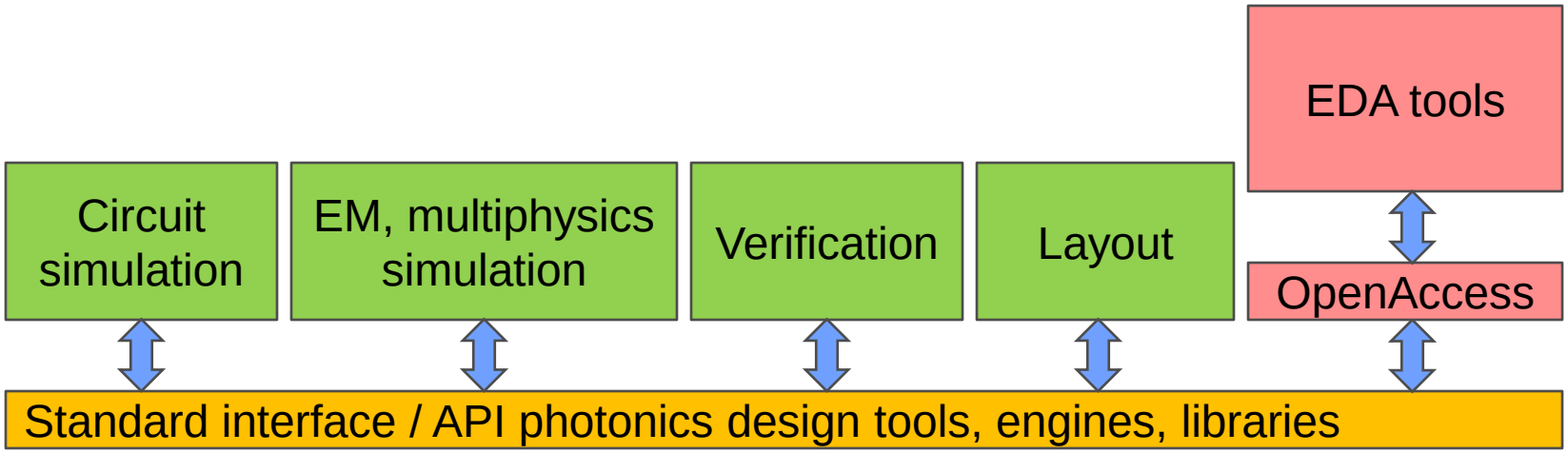
Verfication

Mentor Graphics

DESIGN WORKSHOP TECHNOLOGIES

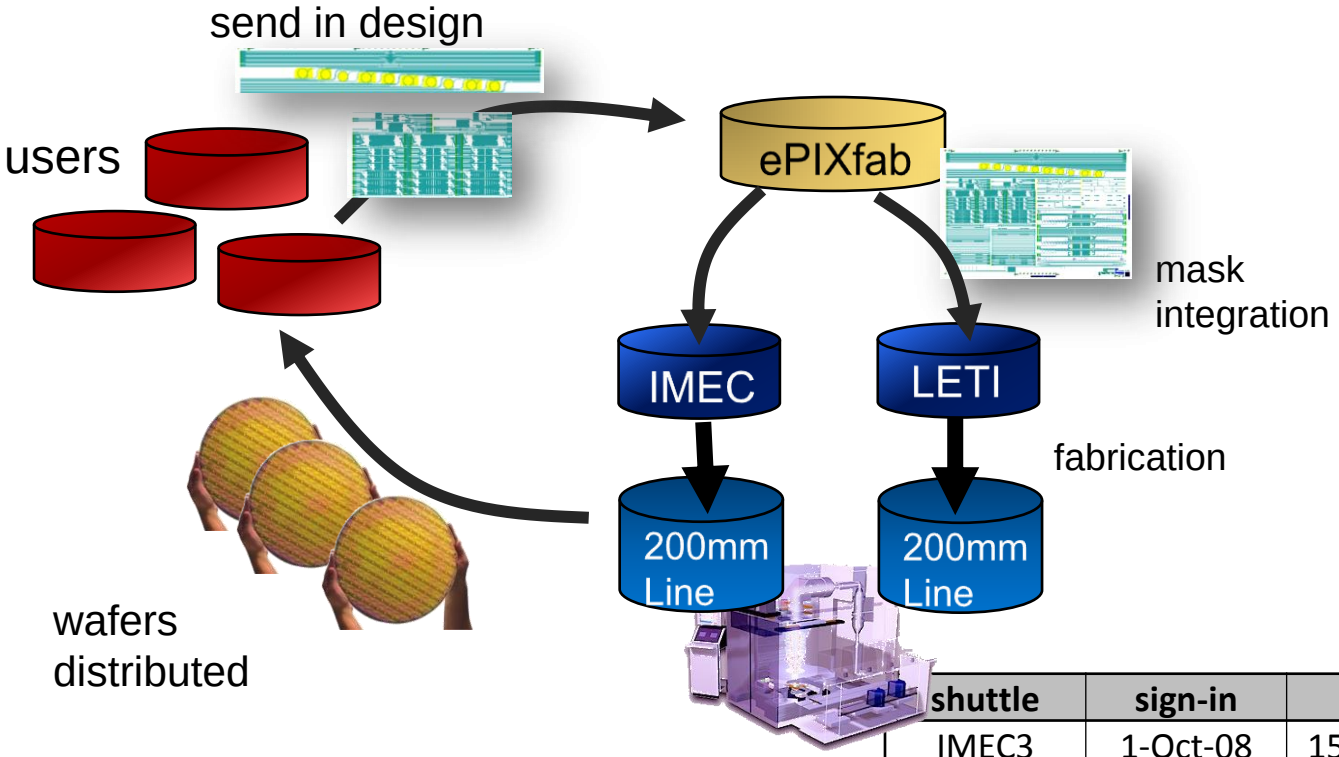
Design automation

- Make photonic design tools talk to each other
- Make EDA tools address photonic engines/libraries
- Enable PDKs with device simulation models, …



PROTOTYPING

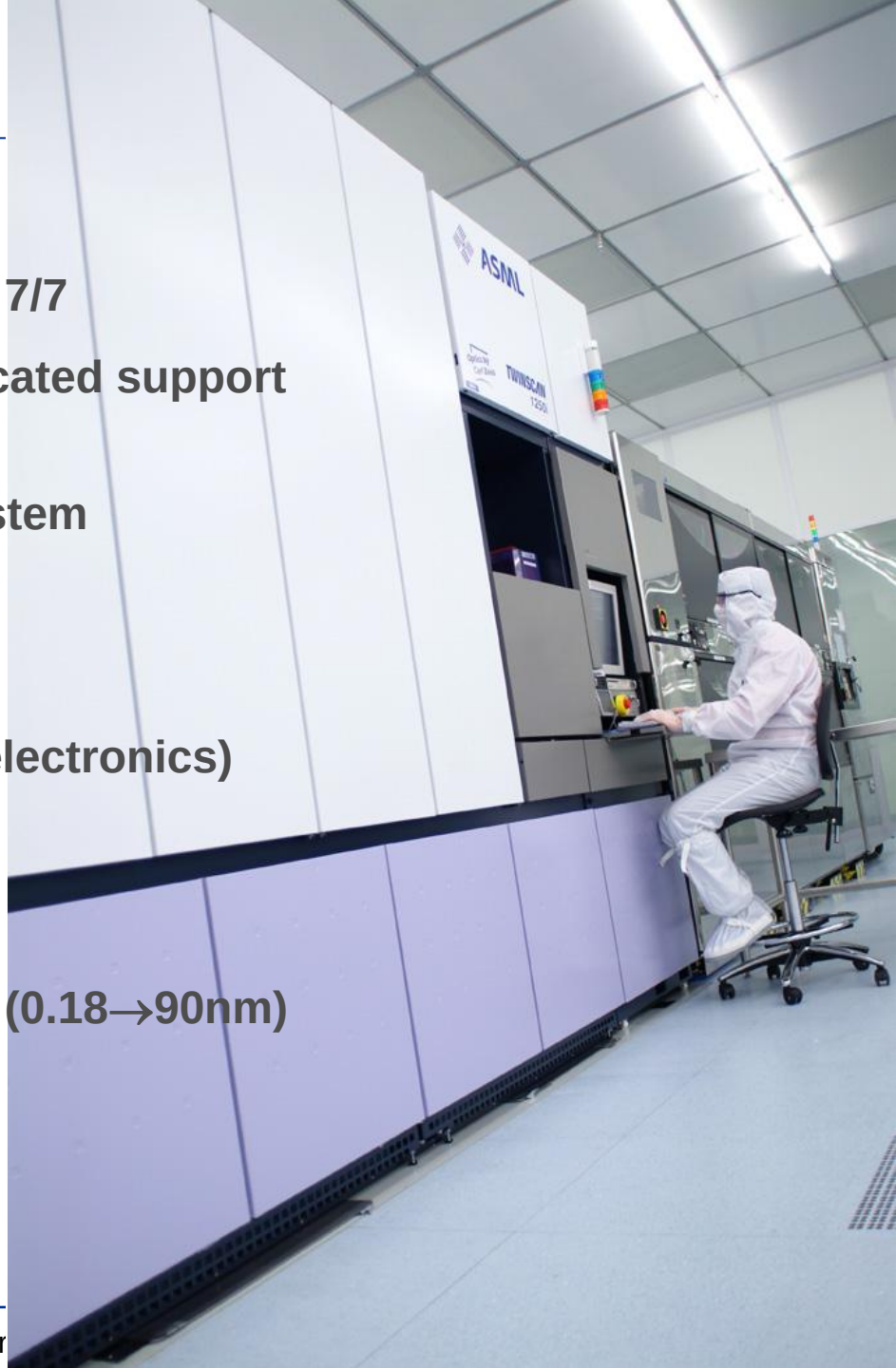
ePIXfab MPW



shuttle	sign-in	mask	processed	technology
IMEC3	1-Oct-08	15-Nov-08	23-Feb-09	IMEC
LETI3	15-Jan-09	1-Mar-09	9-Jun-09	LETI
IMEC4	1-May-09	15-Jun-09	23-Sep-09	IMEC
IMEC5	1-Oct-09	15-Nov-09	23-Feb-10	IMEC
LETI4	Jan-10	Feb-10	May-10	LETI
IMEC6	Apr-10	May-10	Aug-10	IMEC
LETI5	June-10	July-10	Oct-10	LETI
IMEC7	Oct-10	Nov-10	Feb-11	IMEC
LETI6	Jan-11	Feb-11	May-11	LETI
IMEC8	Apr-11	May-11	Aug-11	IMEC

Technology

- 200mm pilot lines
  - Continuous operation 24/24, 7/7
  - Trained operator force, dedicated support team, development team
  - Manufacturing execution system
- Well controlled environment
  - Strict contamination control
  - Statistical process control (electronics)
  - Procedures
- High-end tools
  - Deep submicron technology (0.18→90nm)
  - Wafer scale (200mm)
  - 193nm deep UV lithography



Public offering of fab process

Main questions:

- what is useful to the fabless researcher?
- how much are they willing to pay for it?
- cost control:
  - process running cost
  - process maintenance cost
  - manpower
- supply chain control
- risk control & mitigation

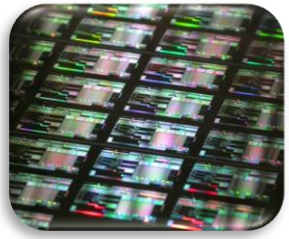
A process that makes fantastic devices is not necessarily a process that can be sustainably offered!

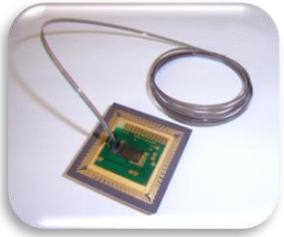
Silicon Photonics Forum

Building the food chain from research to the market

Friday 30 April 2010
imec auditorium, Leuven, Belgium
10h30 – 17h


Design


Prototyping


Packaging


Manufacturing


Training

- Learn about the fabless supply chain
- Discuss the future of fabless silicon photonics
- Silicon photonics tutorial 8h30-10h

Keynote: Cary Gunn, experiences from Genalyte and Luxtera

Speakers include PhoeniX, AMO, OptoCAP, DAS photonics, KTH, XiO,TU Berlin, NTU Athens, PoliMi, imec, …

Registration & venue: www.epixfab.eu