

# Self-Precharge in Single-Leg Flying Capacitor Converters

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**Abstract**—Flying Capacitor (FC) multilevel pulse width modulated (PWM) converters are an attractive choice due to the natural voltage balance property. During start-up of the converter, care has to be taken that the power switches are not exposed to voltage overstress due to uncharged capacitors. A flying capacitor self-precharge technique is proposed which, by making use of natural balancing and a DC-bus rate control, makes the capacitors balance with a zero average load current. The DC-bus rate control depends on the capacitor voltage balance dynamics. The regular PWM natural balancing technique gives good results for even-level single-leg converter self-precharge, for odd-level converters a special switching pattern is necessary.

## I. INTRODUCTION

Multilevel converters were developed as a result of a growing need for higher power converters, [1], [2]. In order to achieve this higher power rating, the voltage and current capabilities of the devices used in the converter need to be increased. Current insulated gate bipolar transistor (IGBT) technology extends up to 6.5 kV 900 A per switching device. Converters that make use of a series connection of switches, allow for the use of switches with reduced voltage ratings. These lower voltage switches have lower switching losses and can switch at a higher frequency. Higher switching frequencies and a smaller voltage step capability result in higher quality switching waveforms.

Flying capacitor multilevel converters are an attractive choice due to the natural voltage balance property. The natural balancing is achieved by applying a phase shifted carrier PWM (PSCPWM) method. The balancing of the capacitors is driven by load current high order harmonics, [3]-[6], namely, by the capacitor "voltage unbalance" excessive energy dissipation in the converter load by switching harmonics in the load current. Though it is accepted to consider a simplified series LR-load model, practically high frequency loss mechanisms like skin-effect and PWM eddy current core losses are expected to make voltage balance rate faster.

FC literature survey shows that so far the engineering community is convinced that flying capacitors precharge is a complex task that may be considered as a FC converter serious disadvantage. Statements as "Additional circuits are also required to initialize the capacitor charge", [7] and "Precharging all the capacitors to required voltage level at start-up is complex", [8], make one believe it can be a serious drawback for FC converters.

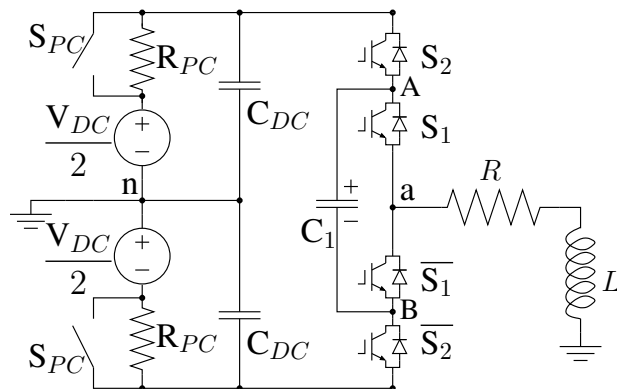


Fig. 1. Three-level flying capacitor multilevel converter circuit topology.

It is this paper's goal to show that the common spread opinion about FC converter precharge complexity to a certain extent is a myth and, given DC power supply voltage build-up rate control at start-up, flying capacitors may be precharged to their required balanced voltage levels at virtually no cost. This can be done with no change to the converter's topology and by using as much as possible the normal control of the converter and its switches.

## II. SELF-PRECHARGE FOR THREE-LEVEL FC CONVERTER

The topology of a three-level single leg FC converter is depicted in Fig. 1. In all FC converter topologies, each pair of switches (as  $S_1$ ,  $\bar{S}_1$  and  $S_2$ ,  $\bar{S}_2$ ) are switched complementary. The pulse width modulation (PWM) strategy used for this topology incorporating the natural balancing mechanism is depicted in Fig. 2. When the normalized voltage command  $D$  is above carrier  $c_1$  ( $c_2$ ), switch  $S_1$  ( $S_2$ ) is turned on; when below carrier  $c_1$  ( $c_2$ ), switch  $\bar{S}_1$  ( $\bar{S}_2$ ) is turned on.

With the start-up of the converter, capacitor  $C_1$  is expected to be discharged, so the voltage over the capacitor equals zero. The capacitor can be regarded as a short circuit. Points A and B in Fig. 1 are at the same voltage and at that point there is in fact a two-level converter, with only switches  $S_2$ ,  $\bar{S}_2$ . When suddenly a voltage  $V_{DC}$  is put on the DC bus, voltage overstress can occur on these switches.

To avoid overstress of the switches, it is required that

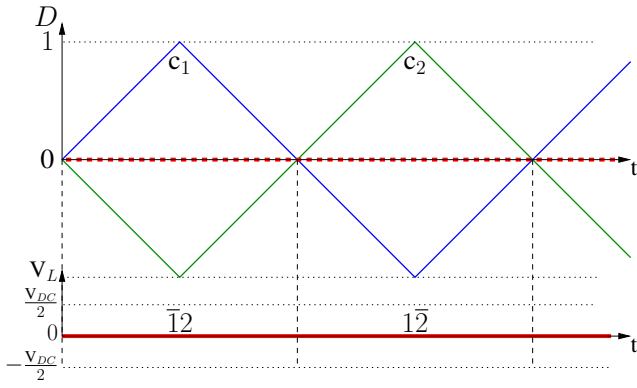


Fig. 2. Natural balancing PWM strategy for three-level FC converter with  $D=0$ .

capacitor  $C_1$  has a voltage which is consistent with  $V_{dc}$ . This can be done by increasing the voltage on the DC-bus slowly. A simple approach to achieve this is by placing a resistor ( $R_{PC}$ , precharge resistor) between the power supply and the DC-bus capacitors  $C_{DC}$ . This gives following time constant for the DC-bus voltage rise when no extra load is presumed:

$$T_{PC} = R_{PC}C_{DC}. \quad (1)$$

After precharging, switches  $S_{PC}$  are closed, shorting resistances  $R_{PC}$ . This way extra losses during normal operation are avoided. This circuit can already be found in normal converters to avoid large charge currents while turning on the DC power supply.

During the precharging, the load current must be under control and as close to zero as possible. To achieve this, a normalized voltage command of  $D=0$  is chosen. As depicted in Fig. 2,  $D = 0$  for a three-level converter results in a zero output voltage on average on a switching period for an arbitrary capacitor voltage and pure zero for a perfectly balanced capacitor. When the capacitor has zero voltage, the output voltage  $v_{an}$  switches between  $V_{C_{DC}}$ , the voltage over the DC-bus capacitors, and  $-V_{C_{DC}}$  with a duty ratio of  $1/2$ . The switching of the output voltage  $v_{an}$  results in currents which will balance the capacitors. Charging of capacitor  $C_1$  with a voltage step on the DC-bus is depicted in Fig. 3. Parameters used in this simulation are:  $R=1.5\Omega$ ,  $L=1\text{mH}$ ,  $C_1=500\mu\text{F}$ ,  $T_{pwm}=410\mu\text{s}$ .

For a three-level FC converter with zero voltage command ( $D=0$ ), voltage balance exponential dynamics time constant is, [9],

$$T = \frac{48L^2C}{RT_{PWM}^2}. \quad (2)$$

Formula (2) and other time constant estimations in this paper assume inductance dominated load on switching frequency:

$$T_{pwm} < T_L = \frac{L}{R}, \quad (3)$$

meaning low ripple current. Another requirement is a relatively low capacitor ripple voltage that allows effective averaging on a switching period to calculate average voltage balance dynamics. If (3) does not hold, then the actual voltage balance

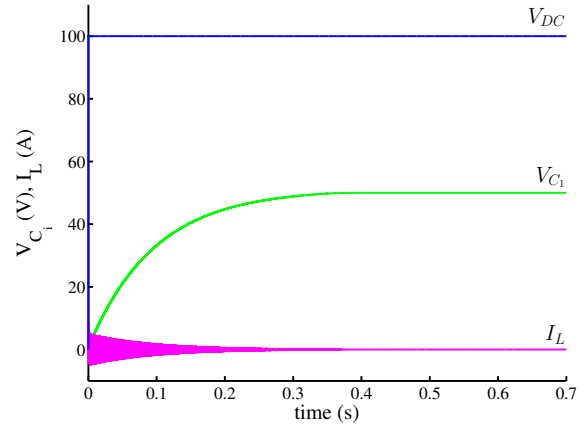


Fig. 3. Self-precharge of capacitor  $C_1$  of a three-level FC converter with voltage step on DC-bus,  $T=0.096\text{s}$ .

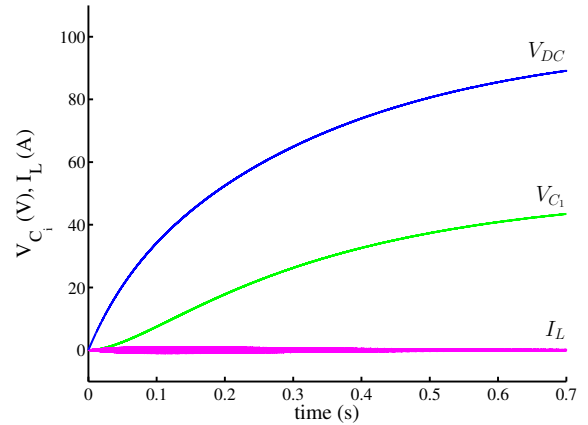


Fig. 4. Self-precharge of capacitor  $C_1$  of a three-level FC converter with making use of  $R_{PC}$ .

time constant is larger than that predicted by formula (2). On the other hand, unaccounted additional high frequency load loss mechanisms, like skin-effect, PWM eddy current and hysteresis core loss, make voltage balance dynamics faster.

The time constant of equation (2) can now be used to calculate a time constant for the voltage on the DC-bus capacitors. By taking a time constant for the DC-bus voltage (1) which is sufficiently larger, e.g. two times the balancing time constant, the voltage over capacitor  $C_1$  can follow the DC-bus voltage, as is depicted in Fig. 4. This way the voltage over every switch is never higher than the voltage in normal use. There can also be noticed that the current ripple stays smaller because the DC-bus and the flying capacitor voltage gradually rise.

The capacitor voltage balancing time constant depends on the load parameters. If the load of the converter is not primarily known, a special precharge load can be connected only for the self-precharge balancing, or a balance booster can be used for the self-precharge and during normal operation of the

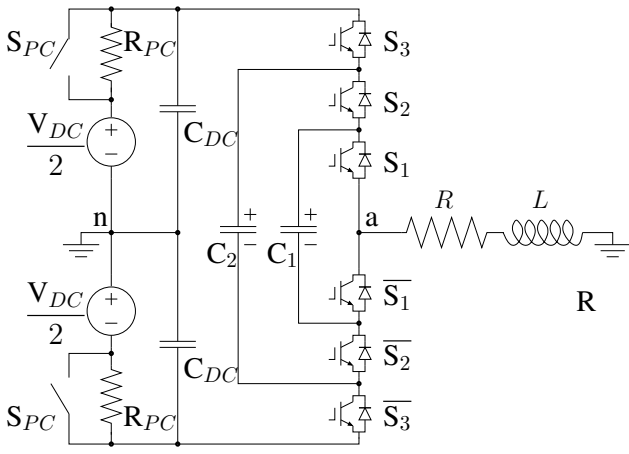


Fig. 5. Four-level flying capacitor multilevel converter circuit topology.

converter, [6].

### III. SELF-PRECHARGE FOR FOUR-LEVEL FC CONVERTER

The topology of a four-level single leg FC converter is depicted in Fig. 5. To create four levels on the output, now two flying capacitors and three pair of switches are needed. To control these three pair of switches while incorporating the natural balancing mechanism, three carrier waves are necessary to define the switching states pattern for a given normalized voltage command  $D$ . The three carrier waves can be ordered using two different modulation strategies. The first strategy can be referred to as the lead strategy because the carrier wave  $c_1$  leads  $c_2$  and  $c_2$  leads  $c_3$ , as depicted in Fig. 6(a). For the alternative, the lag modulation strategy, the carrier wave  $c_3$  leads  $c_2$  and  $c_2$  leads  $c_1$ , as depicted in Fig. 6(b). As may be observed, the lag modulation strategy generates inverse switching states sequence with respect to the lead modulation strategy.

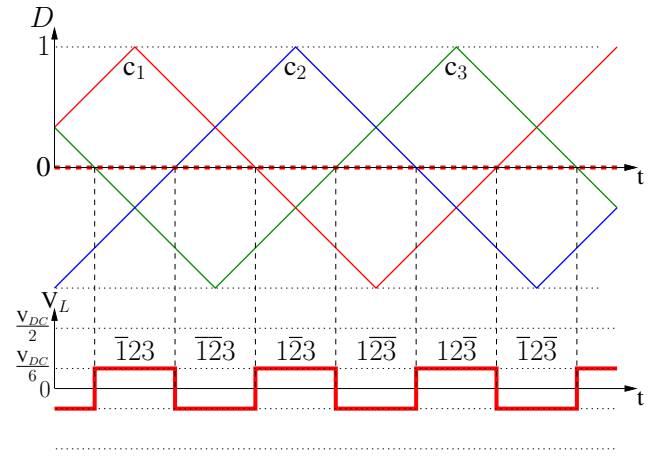
As follows from the modulation strategies, it is impossible to get a constant zero load voltage  $V_L$  for  $D=0$  and balanced capacitors. Instead, a switching voltage between  $\frac{V_{dc}}{3}$  and  $-\frac{V_{dc}}{3}$ , with zero mean voltage, is applied over the load. This zero mean voltage results in a zero mean load current.

#### A. Ideal switches without anti-parallel clamping diodes

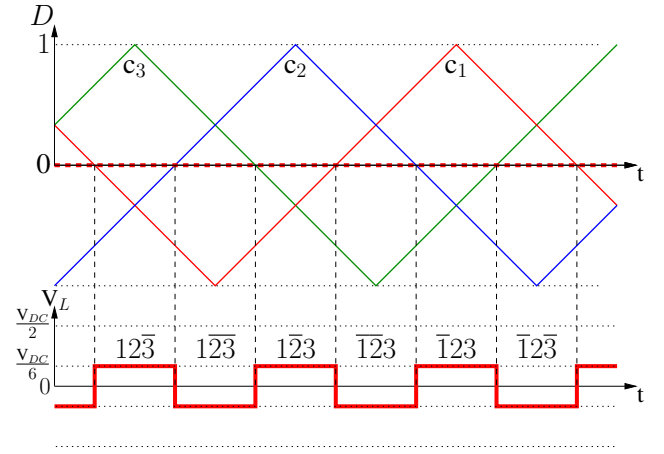
In the theoretical work regarding step response time constants and oscillation frequencies, ideal switches and the lack of anti-parallel clamping diodes are assumed, [10]. Otherwise the clamping diodes would introduce non-linearities which are hard to take into account.

For a four-level FC converter, under the assumption (3), the flying capacitor voltages show an oscillating step response for a step in the DC-bus voltage. For a zero normalized voltage command  $D = 0$ , the voltage balance angular frequency and damping time constant amount to, [10]:

$$\omega = \frac{T_{pwm}}{12L\sqrt{C_1C_2}}, \quad (4)$$



(a) Lead PWM strategy.



(b) Lag PWM strategy.

Fig. 6. Natural balancing PWM strategy for four-level FC converter, lead and lag strategies.

$$T = \frac{648L^2C_1C_2}{5RT_{pwm}^2(C_1 + C_2)}. \quad (5)$$

The capacitor voltages step response on a DC-bus voltage step for a four-level FC converter with ideal switches, using the same parameters as for the three-level converter with equal capacitor values ( $C_1 = C_2$ ) and using the lead modulation strategy, is depicted in Fig. 7(a). The one for the lag modulation strategy is depicted in Fig. 7(b). For the lead modulation strategy, the oscillating voltage component of the first capacitor leads that of the second capacitor. For the lag strategy, the oscillating voltage component of the first capacitor lags that of the second capacitor.

#### B. Real switches with anti-parallel clamping diodes

Real FC converters use switches with anti-parallel clamping diodes, like IGBT's with an anti-parallel clamping diode in the same package. This has some consequences when these switches are used for the self-precharging of the capacitors:

- The capacitors can not have a negative voltage. (due to the clamping diodes, but also because mostly electrolytic capacitors are used)

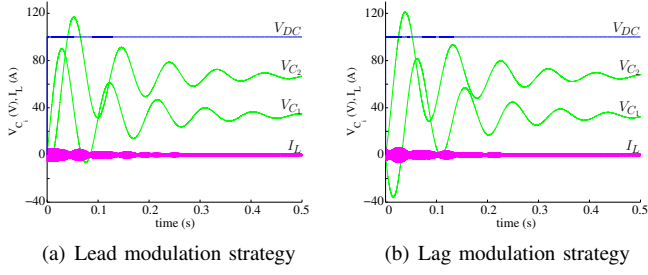


Fig. 7. Self-precharge of the flying capacitors of a four-level FC converter with voltage step on DC-bus and ideal switches without anti-parallel clamping diodes.

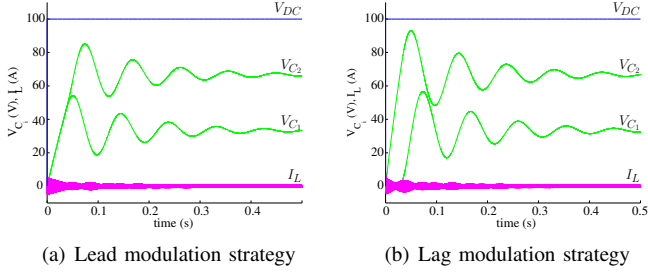


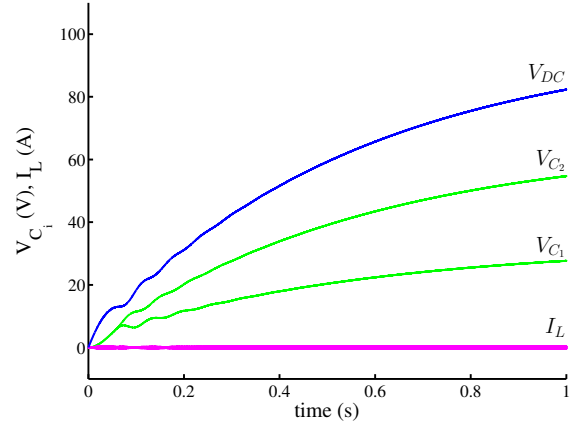
Fig. 8. Self-precharge of the flying capacitors of a four-level FC converter with voltage step on DC-bus and anti-parallel clamping diodes.

- There exists an order in capacitor voltages:  
 $V_{C_1} \leq V_{C_2} \leq V_{C_3}$ .

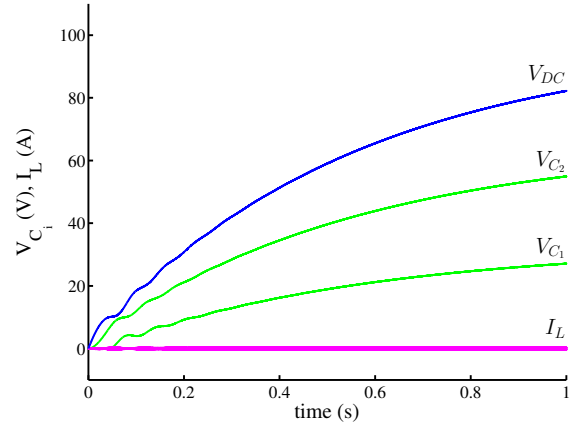
Both properties have an influence on the step response as non-linearities are introduced. The capacitor voltage step response for the lead modulation strategy is depicted in Fig.8(a), the one for the lag modulation strategy in Fig. 8(b). For the lead modulation strategy, the oscillating voltage component of the first capacitor leads that of the second capacitor, but the clamping diode clamps the voltage of the second capacitor to that of the first capacitor. Both capacitors are then connected in parallel. Both capacitors are now charged at the same time until the first capacitor reaches its nominal voltage. The total balancing is now slightly faster and with a smaller amplitude of the oscillations, making it acceptable to use the ideal equations.

The time constant  $T$ , from equation (5), can be used to find a DC-bus voltage rise time constant. Similar to the three-level case, precharge resistors  $R_{PC}$  can be used. The resistors  $R_{PC}$  can be calculated so the DC-bus voltage rise time constant is around double the balancing time constant (5). The balancing time constant for the given parameters is 0.129. For DC-bus capacitors of  $470\mu\text{F}$  and a DC-bus time constant double of the balancing time constant,  $R_{PC}$  is  $551\Omega$ .

The capacitor voltage responses, using the calculated  $R_{PC}$ , for the lead and the lag modulation strategies are depicted in Fig. 9). The influence of the modulation strategy on the capacitor voltage response is not very significant because the change of the DC-bus voltage is small enough.



(a) Lead modulation strategy



(b) Lag modulation strategy

Fig. 9. Self-precharge of the flying capacitors of a four-level FC converter with making use of  $R_{PC}$ .

#### IV. SELF-PRECHARGE FOR FIVE-LEVEL FC CONVERTER

The topology of a five-level single leg FC converter is depicted in Fig. 10. To create five levels on the output, now three flying capacitors and four pairs of switches are needed.

This time four carrier signals are needed to define the switching states pattern, as depicted in Fig. 11. Here only the lead modulation strategy is depicted, but also for the five-level case a lag modulation strategy can be considered. For the lag modulation strategy, the order of the carrier signals is reverted, resulting in a switching states sequence which is the inverse of the one of the lead modulation strategy. As follows from the switching states pattern, there will be a pure zero output voltage for  $D = 0$  and perfectly balanced capacitors.

Simulations for a DC-bus voltage step response, for ideal switches without anti-parallel clamping diodes, are depicted in Fig. 12. For these simulations the same parameters as previously were used with equal capacitor values ( $C_1 = C_2 = C_3$ ). The voltages of capacitors  $C_1$  and  $C_3$  are opposite to each other and the voltage of capacitor  $C_2$  oscillates to its nominal voltage.

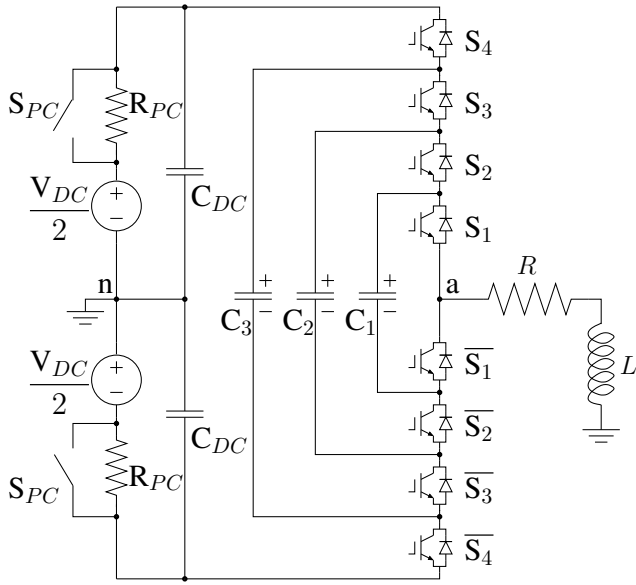


Fig. 10. Five-level flying capacitor multilevel converter circuit topology.

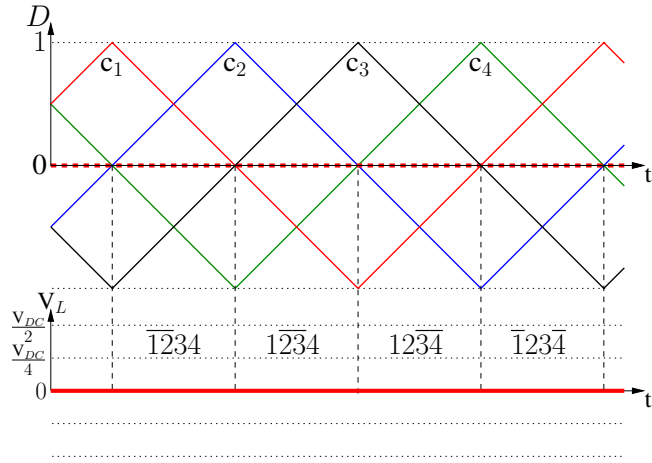


Fig. 11. Natural balancing PWM strategy for five-level FC converter, lead modulation strategy

The flying capacitor's voltage dynamics are dependent on two time constants. One aperiodic time constant controlling the common mode voltage of capacitors  $C_1$  and  $C_3$ , [11], (for  $0 \leq D < 0.5$ ):

$$T_A(D) = \frac{48L^2(C_1 + C_3)}{RT_{pwm}^2 D^2 (3 - 4D)}. \quad (6)$$

For  $D \rightarrow 0$ , this time constant  $T_A$  tends to infinity, which corresponds to the results from the simulation. The second time constant controls the balancing of the excessive unbalance energy between capacitors  $C_2$  and both  $C_1$  and  $C_3$ , [11], (for  $0 \leq D < 0.5$ ):

$$T_P(D) = \frac{384L^2(C_1 + C_3)}{RT_{pwm}^2 [16D^3 - 3(F + 6)D^2 + 2(F + 2)]}, \quad (7)$$

with  $C_{123}$  the equivalent capacitance of the three series

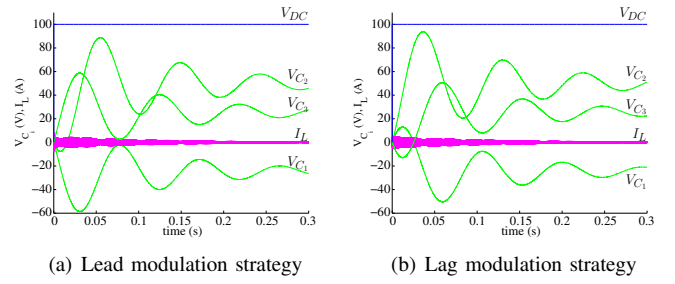


Fig. 12. Self-precharge of the flying capacitors of a five-level FC converter with voltage step on DC-bus and ideal switches without anti-parallel clamping diodes.

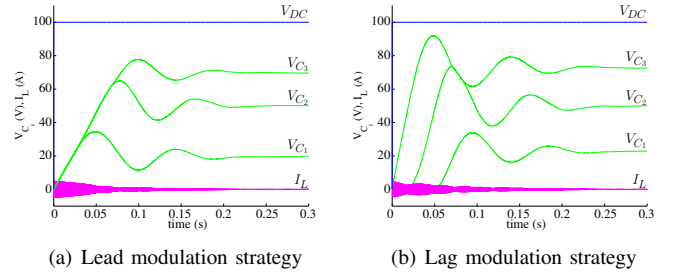


Fig. 13. Self-precharge of the flying capacitors of a five-level FC converter with voltage step on DC-bus and anti-parallel clamping diodes.

connected capacitors:

$$F = F(C_1, C_2, C_3) = \frac{C_1 + C_3}{C_2} + \frac{C_1}{C_3} + \frac{C_3}{C_1}. \quad (8)$$

The same simulations for real switches with anti-parallel diodes are depicted in Fig. 13. The non-linearities, introduced by the clamping diodes, allow self-precharge in this case. A simulation with first order DC-bus voltage rise is depicted in Fig. 14. It can be concluded that the non-linearities only allow self-precharge for fast DC-bus build-up rates. This makes this self-precharge method unusable in this case as fast DC-bus build-up rates lead to voltage overstress on the switches.

## V. SELF-PRECHARGE FOR HIGHER LEVEL FC CONVERTERS

The suggested approach for the self-precharge (using regular PWM with  $D = 0$ ) works for FC converters with even levels as they have only oscillating decaying voltage balance components with a time constant that is small enough to ensure a good balancing. An example of the self-precharge of a six-level FC converter is depicted in Fig. 15.

For an odd number of levels (5-, 7-, ... level) there is an aperiodic voltage balance dynamics term with a time constant which tends to infinity for  $D \rightarrow 0$  and creates potential self-precharge problems. A general solution for this is a special self-precharge switching pattern, preserving the zero mean load current, but altering the capacitor voltage balancing time constants. This is a topic for future research. Fig. 16 shows the example for a seven-level converter.

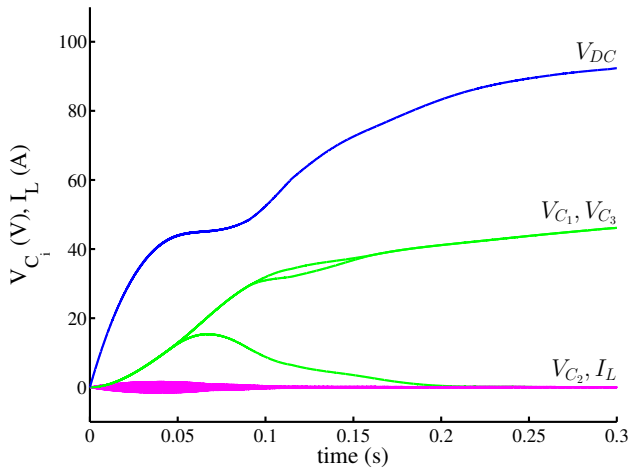


Fig. 14. Self-precharge failure for slow DC bus ramp-up rate for a five-level FC converter with lead modulation strategy.

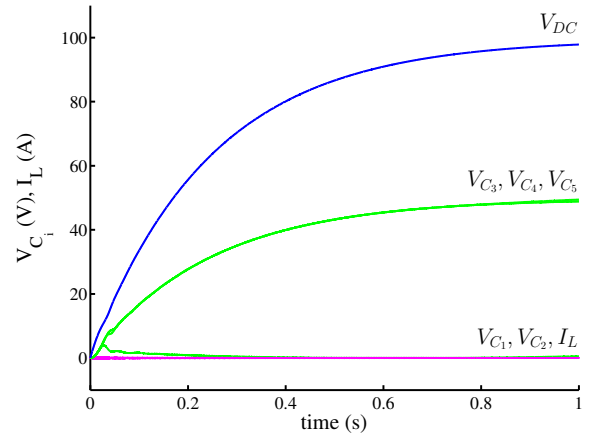


Fig. 16. Self-precharge failure of the flying capacitors with making use of RPC for a seven-level FC converter with lead modulation strategy.

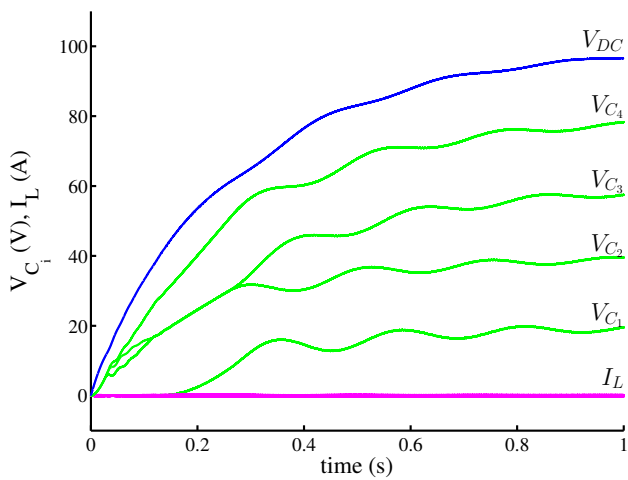


Fig. 15. Self-precharge of the flying capacitors with making use of RPC for a six-level FC converter with lead modulation strategy.

## VI. CONCLUSION

A self-precharge method was proposed for FC converters which uses the natural balancing property of the PSCPWM strategy with a normalized voltage command of  $D = 0$  and a controlled DC bus voltage ramp-up rate. This method is an easy to implement and to control self-precharge method. It does not need special adaptations to the system.

For even level FC converters this method works, resulting in a self-precharge of the flying capacitors without voltage over-stress on the switches. The balancing time constant depends on the load connected to the converter.

For odd level FC converters, this method does not seem to be sufficient to guarantee an accurate balancing of the flying capacitor voltages, except for a three-level where is balancing is trivial. This is due to the aperiodic time constant in the voltage balancing which becomes infinite when  $D$  tends to zero. This can be solved by using a different switching pattern and not just keeping  $D = 0$ . This will be investigated in further

research.

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