Novel Methodology to Integrate Ultra-thin Chips on Flexible Foils

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Abstract

The placement and integration of ultra-thin chips (UTCs) on low-cost polymer foils is a key challenge in the realization of large-area flexible electronic products. Such products, are for cost reasons, preferably fabricated on low cost polyester foils like PET/PEN. A disadvantage of these materials is that they have a low thermal stability. As a consequence of this, the majority of existing chip integration technologies cannot be used. A novel approach for placement and interconnection of UTCs is presented in this paper. This approach, which involves face-up bonding of UTC and its subsequent interconnection, is compatible with low-cost polymer foils.

The key process steps involved in UTC integration using the proposed methodology are discussed in detail. The fabrication of a technology demonstrator to validate the proposed concept is also detailed.

Introduction

Printed electronics, which refers to the application of printing technologies in electronics fabrication, has opened up new application and fabrication possibilities for large-area electronics. Examples of such products are lighting and signage devices, displays, wearable electronic products etc. [1] The additive nature of printing processes, their maturity, high throughput and compatibility with both roll-to-roll (R2R) and sheet-to-sheet (S2S) fabrication are some of the factors that make printed electronics suitable for low-cost large-area electronics. However, printed electronics by itself cannot cater to all the requirements of a large-area electronic system. For instance, the high performance offered by silicon technology cannot be matched by printed electronics; nor would it be preferred or realistic to completely replace silicon technology by printing. Hence, an hybrid approach is often needed, combining the advantages of printed electronics with the high performance of silicon technology to realize large-area flexible electronic products. Moreover, to ensure the flexibility of the resulting large-area electronic product, the silicon chips are preferably integrated in a thinned down form.[2]

The substrate material for R2R manufacturing of low-cost large-area flexible electronic products will not be polyimide as commonly used in more traditional flexible electronics. Usage of polyesters such as PET or PEN are preferred because it allows a reduction of substrate costs by a factor of 5-10 [3]. The usage of such low-cost foils, however, places a constraint on processing temperature, due to their relatively low thermal stability. The glass transition temperature (T_g) for PEN is ~130°C while that for PET it is about 85°C.

The low thermal stability of these foils places restrictions on the chip interconnection process. Widely used interconnection technologies involving soldering cannot be applied on polyester foils as the process temperatures exceed 200°C. Flip-chip thermo-compression bonding using anisotropic conductive adhesives (ACAs) is currently the most widely used methodology to bond and interconnect Si chips on polyester foils. [4, 5] A disadvantage of this technology is that each placed chip needs to be pressed against the foil circuitry for a period of up to 10 seconds to thermally cure the ACA. This thermo-compression bonding process step affects the manufacturing throughput. Additionally, it is a known issue that the very fragile UTCs can be damaged due to the pressing of the chip against the foil circuitry. To overcome these disadvantages, a novel interconnection methodology involving face-up UTC placement and interconnection is proposed in the current paper.

Face-up UTC Integration

The schematic of the novel UTC integration on foil is shown in Figure 1. The following individual steps can be distinguished:

1. Face-up placement of the UTC using die attach adhesive on the foil with pre-printed circuitry, and subsequent curing of the adhesive.
2. Coating of a glob-top material on the UTC and its subsequent curing. The glob-top is a conformal coating to encapsulate the chip, thereby protecting it and providing structural support.
3. Optical recognition of bond-pad locations underneath the glob-top, and laser drilling of vias through the glob-top and stopping at the UTC bonding pads. The vias offer a pathway for electrically interconnecting the UTC to the external circuitry on foil.
4. Optical recognition of locations of the vias and the foil circuitry, and subsequent fabrication of fan-out wiring, which interconnects the chip to the pre-printed circuitry on the foil.

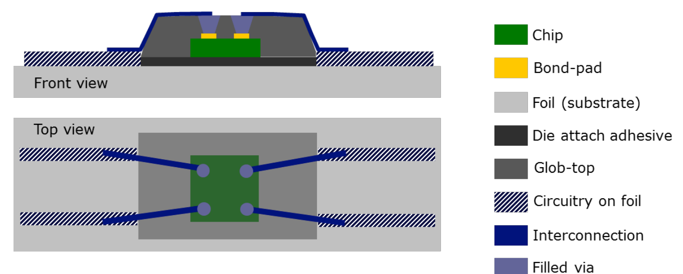

Figure 1. Schematic of face-up UTC integration concept

The main advantages in placing the UTC on foil using the proposed methodology are as follows:

1. *Easy integration of a fine pitch chip with a lower resolution pre-printed foil circuitry:* a fan-out is created that connects the fine pitch chip to the coarse

pitch pre-printed foil circuitry. This removes the need to deploy high resolution printing technologies for the foil circuitry. Figure 2 shows an example of a pre-printed coarse foil circuitry to integrate a fine pitch chip.

2. *Less chances of UTC fracture:* contrary to flip-chip bonding using ACAs, the proposed methodology does not require thermo-compression bonding. As a result, the UTC is subjected to much lower forces during bonding, resulting in a lower chance on chip fracture.
3. *Via metallization and interconnection possibilities:* due to the less stringent process capability requirements (especially resolution) and due to the fanning-out of circuitry, it is possible to use a wide range of via metallization and interconnection technologies. In addition to that, the interconnections can be made in an adaptive manner, compensating for misalignments in UTC placement. This can be done by optical recognition of bond-pad locations with respect to the foil circuitry, and creating the interconnections adaptively.

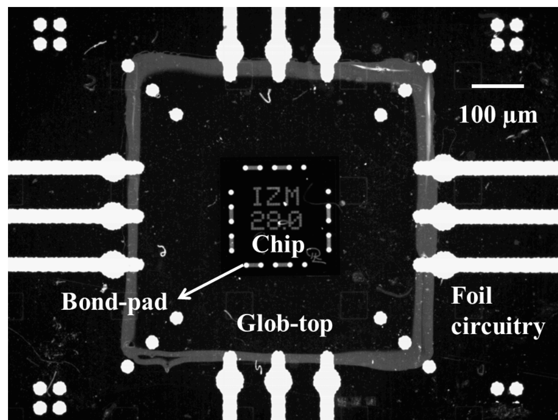

Figure 2. Coarse-pitch design of foil circuitry, enabled by face-up UTC integration. The UTC shown here is an IZM28 daisy chain test chip; the foil circuitry was screen printed

Technology Demonstrator Design

To demonstrate the proposed face-up UTC integration concept, a demonstrator design, shown in Figure 3, was prepared. An IZM28 daisy chain test chip *(from Fraunhofer IZM, Germany)* with Ni/Au metallization on bond-pads was selected for the demonstrator fabrication. The bond-pads are 100 µm in diameter, with the inter bond-pad pitch being 300 µm. These test chips were thinned at the wafer level down to 20 µm using the dicing before grinding (DBG) process *(Disco Hi-tech Europe GmbH, Germany)*. [6] The foil circuitry for the demonstrator was designed taking subsequent electrical and flexural testing into consideration. The proposed layout of the foil circuitry enables via-to-via contact resistance measurement by 4-point resistance method while simultaneously being tested for flexural reliability.

The demonstrator design also included light-emitting diodes (LEDs) as shown in Figure 3 to demonstrate functionality of the circuitry.

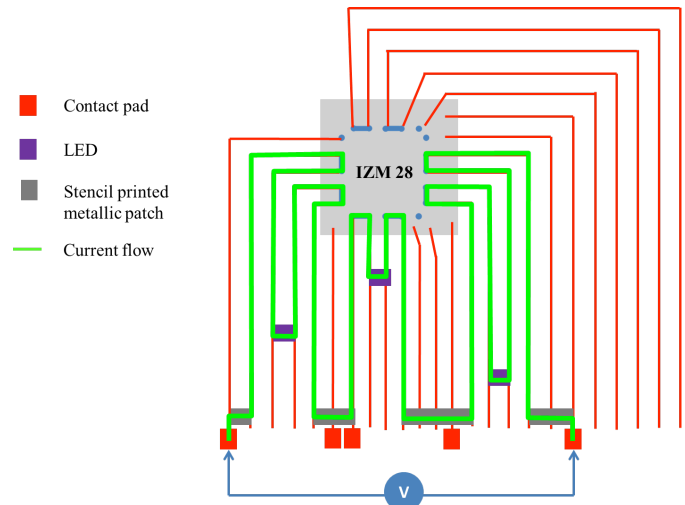

Figure 3. Schematic of the demonstrator design; the path of current flow through the test chip is highlighted

Process Selection for Demonstrator Fabrication

The different processes that were used to demonstrate feasibility of the novel chip interconnection technology are summarized in Table 1.

Table 1: Technologies used in demonstrator fabrication

Process step	Technology
Foil circuitry printing	Screen printing
Die attach adhesive deposition	Stencil printing
Chip placement	Semi-automatic pick-and-place machine
Glob-top deposition	Stencil printing
Via drilling through glob-top	Laser drilling using KrF-excimer 248 nm laser source
Metallization and interconnection	Laser scribing of conductive patch

In Step 4 of the process *(see previous section)* there are different possibilities for making the adaptive circuitry. Based on earlier investigations [1], the laser scribing of conductive patch was selected as the method to create via metallization and interconnection. The investigations showed that this method offers key advantages over other candidate technologies for via metallization and interconnection, viz. inkjet printing, laser inducted forward transfer (LIFT) and electroplating.

The process is shown schematically in Figure 4. The first step is the screen printing of a continuous conductive patch over the chip area, covering the glob-top completely. Screen printing, a mature process well-established in R2R and S2S manufacturing, yields a thick conductive layer (~10 µm) with one stroke of the squeegee. During the printing process, the conductive material is pushed into the vias by the action of the squeegee, thereby forming the metallization. As shown in Figure 4, the printed conductive patch extends slightly beyond the area covered by the glob-top, so that it contacts the pre-printed foil circuitry. The conductive patch is then cured to yield an electrically conductive layer. The next step is to

scribe the patch using an appropriate laser source to separate the vias and their corresponding interconnect paths. The laser source should scribe the screen printed patch without damaging the glob-top, chip or foil underneath.

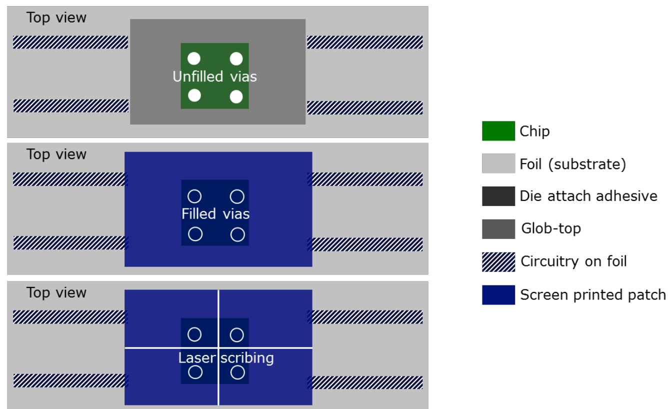

Figure 4. Schematic of main steps involved in laser scribing of conductive screen printed patch in the context of face-up chip integration

Demonstrator fabrication and testing

In addition to the fabrication of the demonstrator with LEDs, four samples were prepared without LEDs to test the electrical properties and flexural reliability. Table 2 lists the materials used for the fabrication of the demonstrator as well as the test samples.

Table 2. List of equipment and materials

Equipment/Material	Model/Type	Supplier
Substrate	PEN 125 µm thick foil	DuPont
Die attach adhesive	WFP-14686-141E	Henkel
Chip bonder	T-3200	Dr. Tresky AG
Glob-top material	Loctite 3730	Henkel
Screen printer	Horizon 03i	DEK International
Laser source for via drilling and scribing	KrF-excimer (248 nm)	ATL Lasertechnik GmbH
Silver paste for screen printing	DuPont 5025	DuPont

All the samples were prepared in the following sequence:

1. Screen printing of foil circuitry and subsequent thermal curing.
2. Stencil printing of the die attach adhesive using a 15 µm metallic stencil by manual doctor blading.
3. Bonding the UTC on the foil and UV curing of the die attach adhesive.
4. Stencil printing of the glob-top material on the UTC using a 20 µm metallic stencil by manual doctor blading, and subsequent UV curing of the glob-top.
5. Via drilling through the glob-top using the KrF-excimer laser. The detailed drilling parameters are discussed in an earlier paper.[1]
6. Screen printing of the conductive patch on the glob-top layer, overlapping the foil circuitry.
7. Laser scribing of the conductive patch using the KrF-excimer laser. The locations of the bond-pads and foil circuitry were recognized using a camera system mounted on the laser setup, and creating scribing paths for the laser manually. The optimized scribing parameters to scribe the conductive patch, with minimal damage to the glob-top layer underneath, were available from an earlier study. [1]
8. The demonstrator preparation involved an additional step: bonding of packaged LEDs on the foil circuitry. Isotropic conductive adhesive (ICA) dots were screen printed on locations governed by the circuit design, and packaged LEDs were bonded using the same pick-and-place device that was used for UTC bonding. Finally, the ICA was thermally cured.

The schematic of flexural testing methodology is shown in Figure 5. The test sample containing the integrated UTC is flexed around two cylinders of selected radii sequentially. One cycle comprises flexing the sample around each of the two cylinders. The flexural test setup can be programmed to measure the resistance after a desired number of cycles, after which it continues with the testing and repeats this procedure until the set number of cycles is reached. The samples flex tested using the settings listed in Table 3.

Table 3. Flexural testing scheme

Cylinder radius (mm)	No. of cycles	No. of samples
10	2000	3
5	2000	1

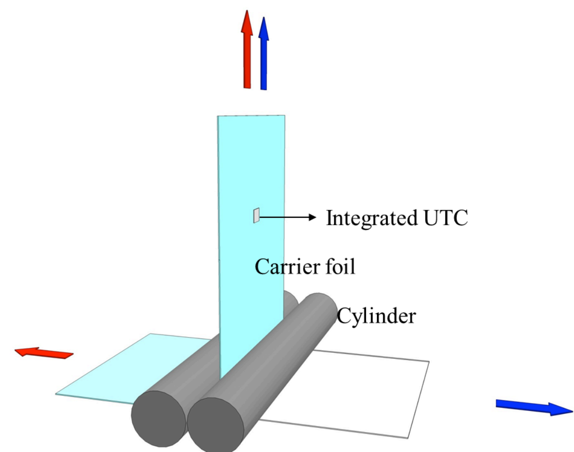

Figure 5. Schematic of flexural testing

Results and Discussion

The glob-top layer thickness on top of the chip was ~17 µm, which was also the depth of the vias. The bond-pads were not damaged during via drilling, as is evident from Figure 6.

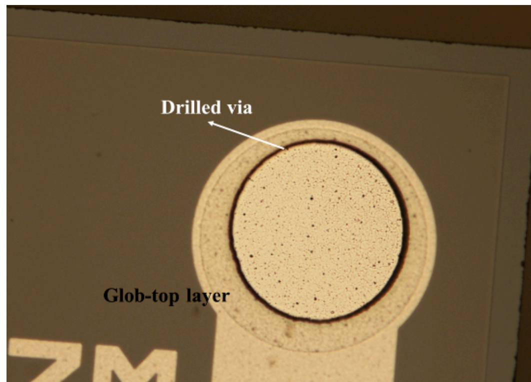

Figure 6. Via drilling through glob-top and stopping on bond-pad

Screen printing of conductive patch resulted in proper via filling, confirmed by electrical measurements and cross-section analyses. Figure 7 shows an overview image of filled vias *(top)*, as well as an image of the cross-section of a filled via *(bottom)*.

Laser scribing of the screen printed conductive patch resulted in isolation of vias and creation of interconnections as per the design. Figure 8 shows the cross-section of a laser scribed line on the conductive patch. It is evident from this micrograph that the conductive patch is properly scribed, thereby providing electrical isolation, without any damage to the glob-top layer underneath.

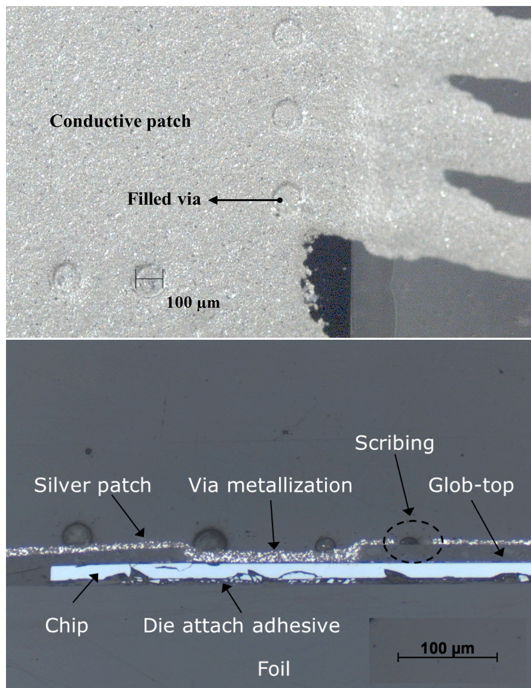

Figure 7. *(top):* overview image of a part of screen printed conductive patch and resulting via filling; *(bottom):* cross-section image of a filled via

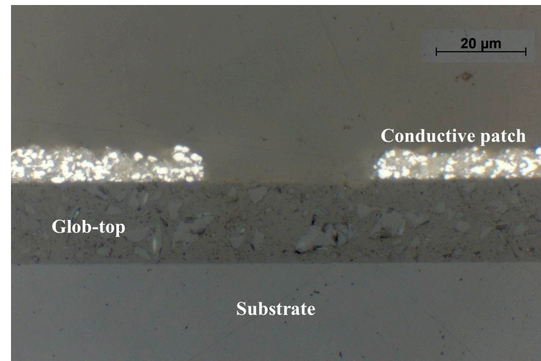

Figure 8. Laser scribed conductive patch; the glob-top layer underneath is undamaged

All the samples subjected to flexural testing survived the fixed number of cycles. The via-to-via resistance values measured in-situ are plotted in Figure 9. The change resistance values was marginal. In several cases, the via-to-via resistance actually decreased; it is hypothesized that this could be due the compaction of the conductive material within the vias as a result of multiple flexing cycles around the cylinders.

The demonstrator functioned as per the design: all the three LEDs lit up when voltage was applied across the foil circuitry. This proves the flow of current through the daisy chains of the UTC, thereby confirming the contact between via metallization and the bond-pads. Figure 10 shows images of the final demonstrator.

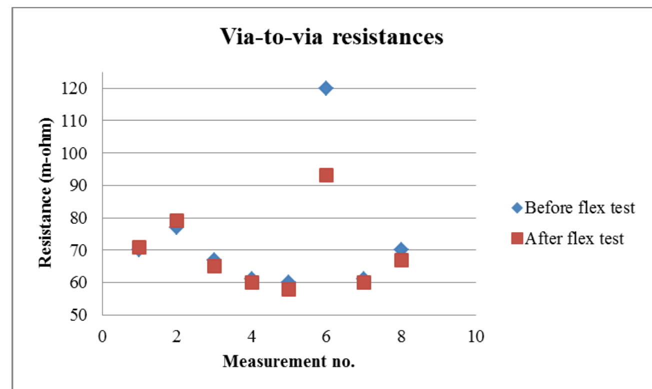

Figure 9. Via-to-via contact resistances before and after flex testing

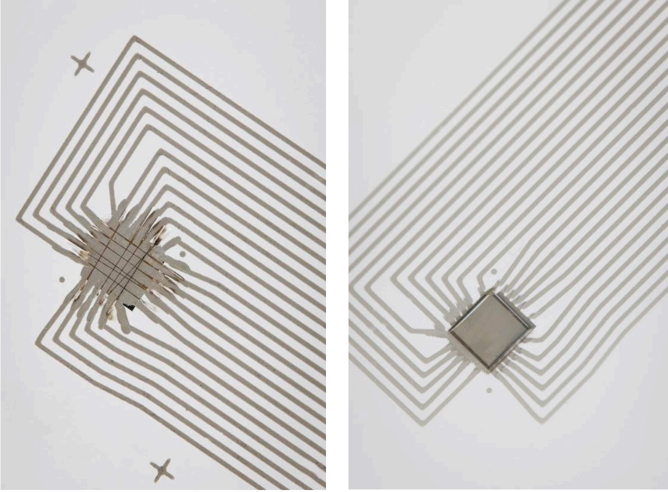

Figure 10. Technology demonstrator: *clockwise, from top:* overview image showing LEDs lit-up due to voltage application, back-side of carrier foil showing bonded UTC, and laser scribed interconnections

Conclusions

The following conclusions are drawn from theoretical and experimental investigations on face-up UTC integration with adaptive interconnection:

1. The proposed methodology is suitable for large-area electronics on low-cost polymer foils.
2. It offers several advantages over existing methodologies. The main advantages are: elimination of the need for high-resolution foil circuitry even for fine-pitched chips, significantly lower chances of UTC fracture during placement, and a multitude of possibilities in via metallization and interconnection.
3. Samples prepared based on the proposed methodology in combination with laser scribing of conductive patch to create via metallization and interconnections offer low via-to-via contact resistance. They also passed the flexural testing around cylinders of 10 mm and 5 mm radius, thereby demonstrating the application potential of the proposed methodology in flexible electronics applications.
4. A technology demonstrator was fabricated and shown to function as per the design.

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