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FACULTY OF ENGINEERING
Department of **Information Technology** INTEC

Small things make a big difference.

Melexis
Microelectronic Integrated Systems

Application of Circuit/Field Co-optimization Techniques to IEC 61967/62132 Test Boards

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Overview

- Introduction
- Circuit/field co-optimization with ADS-Momentum (Agilent EEsof EDA)
- Application of circuit/field co-optimization to DPI test board design
- Conclusions

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- **Introduction**
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Introduction

- **Design of PCBs for IC-level EMC tests: conducted emission and immunity testing (e.g. 150 Ohm method and DPI) and radiated emission and immunity testing (TEM-cell)**
- **Important issues:**
  - Transfer characteristics of RF coupling path (from SMA to IC-pin):
    - **maximal deviation < 3 dB**
    - **no resonances allowed**
  - Extension of frequency range: from 150 kHz to 2.5 GHz (instead of 1 GHz)
- **Optimization of test and application boards by prototyping and measuring is costly and time-consuming**
  => Circuit/field co-optimization is necessary

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- Application of circuit/field co-optimization to DPI test board design
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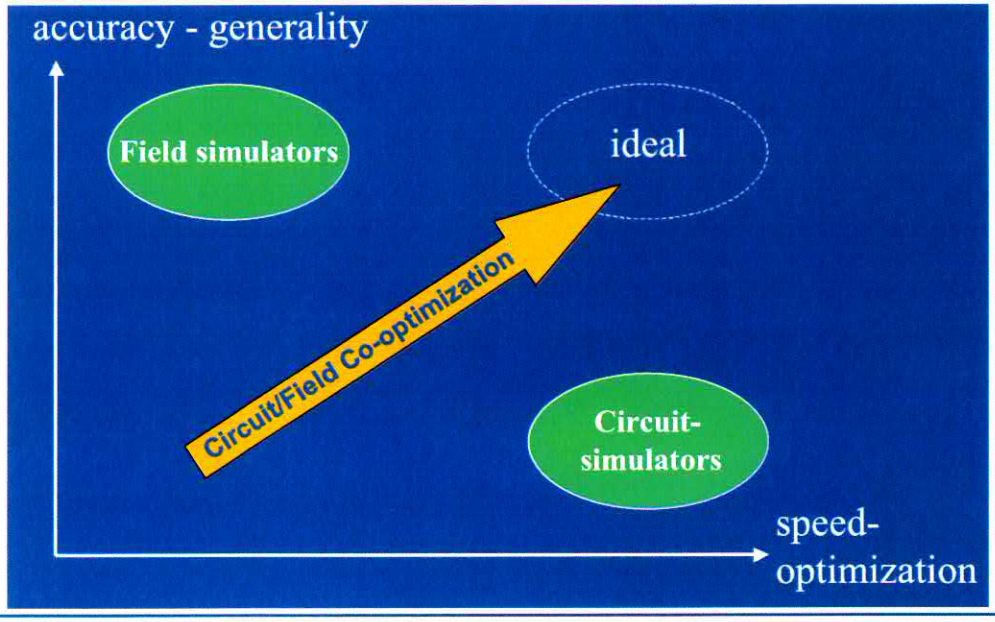
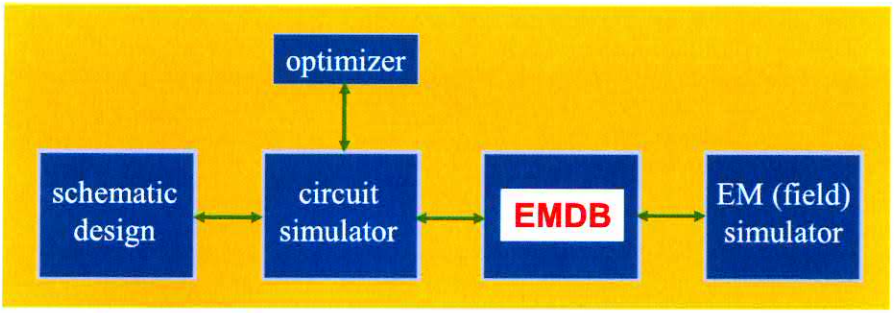
Circuit/Field Co-optimization

- Design techniques for high speed and RF design



Circuit/Field Co-optimization

- Design techniques for high speed and RF design



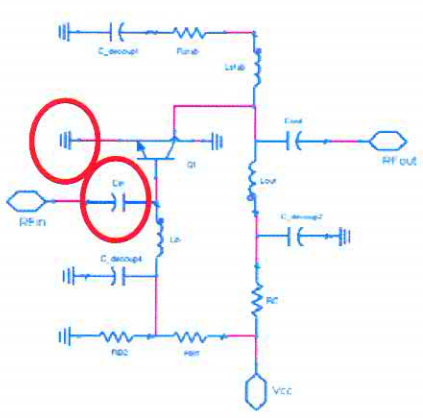
EMDB =
Electromagnetic
Model
Data**B**ase

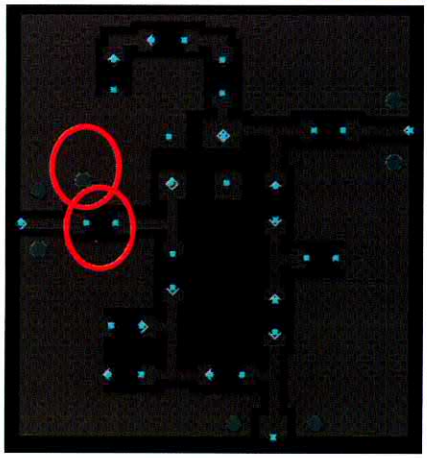
circuit simulator ⇨ transient, frequency domain, DC, AC, Harmonic Balance, Envelope Analysis, ...

EMDB ⇨
- the EMDB holds the data for a **GLC**
- **GLC**: **G**eneralized **L**ayout **C**omponent
- data: S-parameter data

Circuit/Field Co-optimization

- Example: LNA design





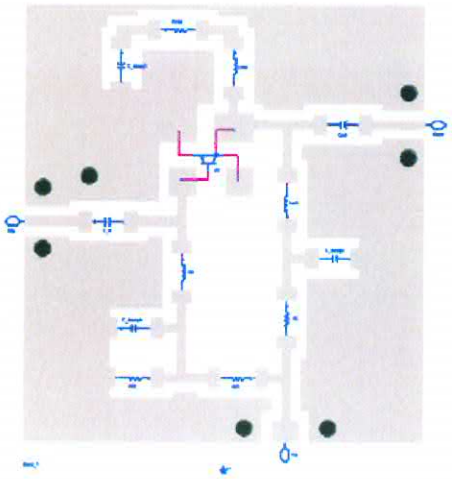
Low noise amplifier schematics

RF board footprint

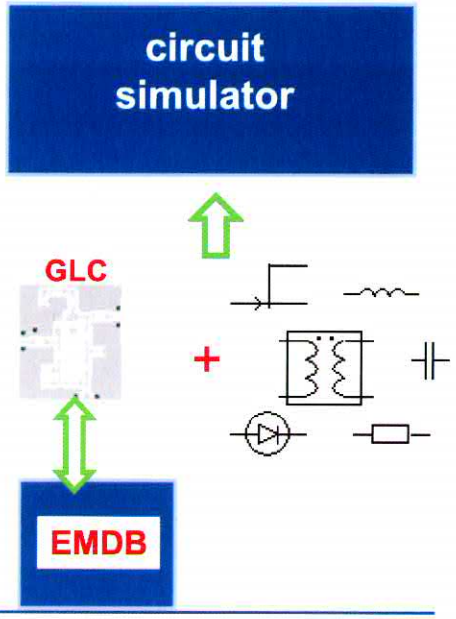
to be optimized

Circuit/Field Co-optimization

- Example: LNA design



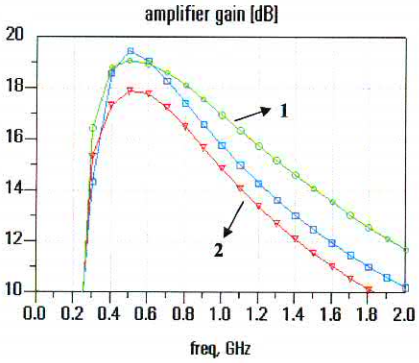
Schematic of the low noise amplifier including the GLC for the RF board footprint



Circuit/Field Co-optimization

- Example: LNA design

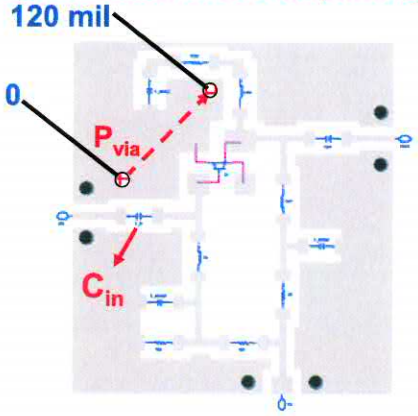
Amplifier gain as a function of frequency



result of original schematic without effect of RF board

result of original schematic including effect of RF board

Optimization of the amplifier gain

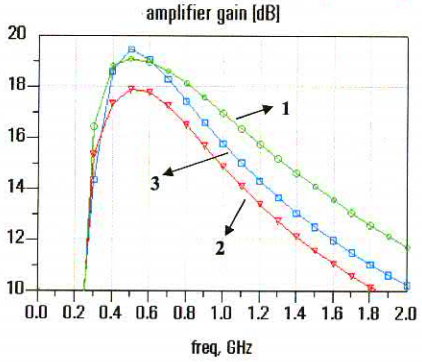


parameter p_1: input capacitance value C_{in}
parameter p_2: position of grounding via of emitter contact P_{via}
initial values: C_{in} = 12 pF, P_{via} = 20 mil

Circuit/Field Co-optimization

- Example: LNA design

Amplifier gain as a function of frequency



Optimization of the amplifier gain

- initial values: p_1 = C_{in} = 12 pF, p_2 = P_{via} = 20 mil (see curve 2)
- $0 < P_{via} < 120$ mil
- goal: optimize gain between 0.4 and 0.6 GHz

result of optimized gain including effect of RF board

$C_{in,opt}$ = 120 pF
$P_{via,opt}$ = 89.73 mil
extra gain of 2dB

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DPI Test Board Design

Problem statement:

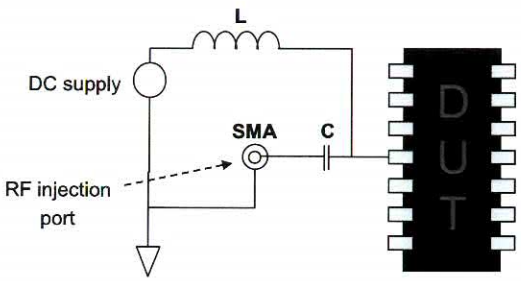
- **Determine transfer characteristics (S-parameters) of RF coupling path (from SMA to IC-pin):**
  - maximal deviation < 3 dB
  - no resonances allowed

How?

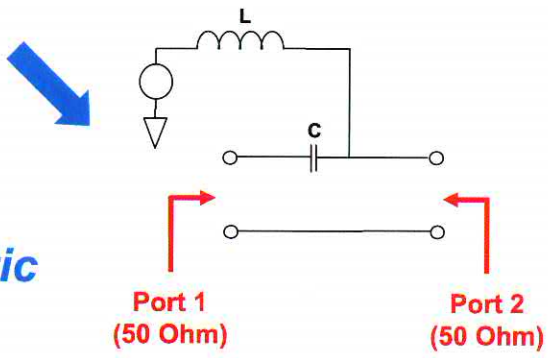
- **Replace IC-pin by 50 Ohm termination**
- **Calculate S-parameters**
- ***Incorporate all high-frequency effects!***

DPI Test Board Design

- Example: IC's VDD-pin → S-parameters



Principle of DPI test-setup



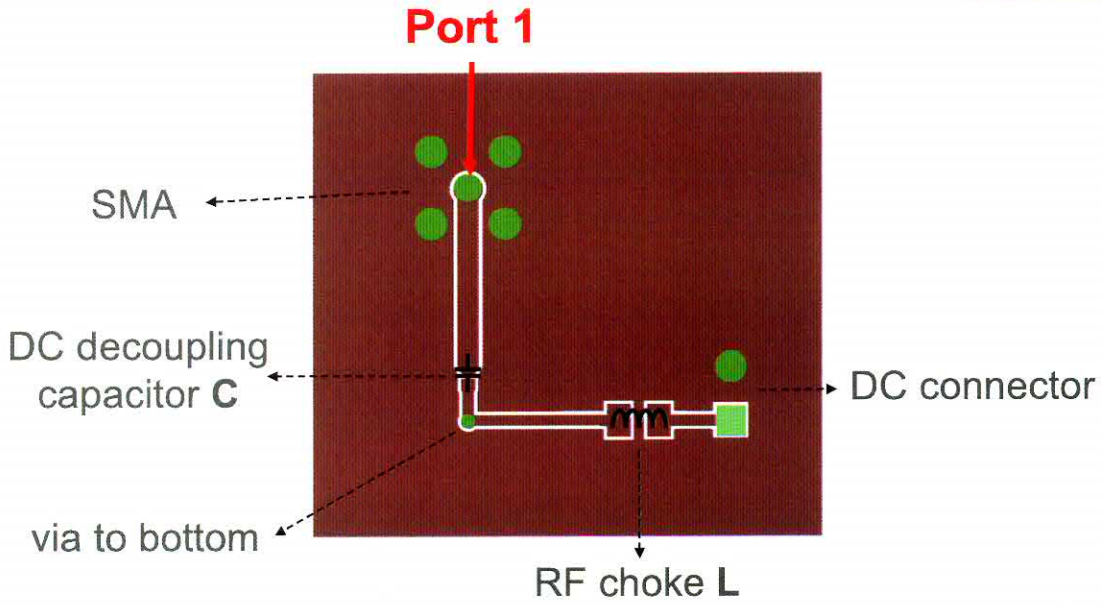
two-port network: transfer characteristic determined by S_{21}

DPI Test Board Design

- At high frequencies it is crucial to include the board characteristics!!
- Board:
  - **Double-sided FR4**
    - substrate thickness = 1.6 mm
    - relative permittivity = 4.35
  - **Grounded Co-Planar Waveguide**
  - **IC (DUT) placed at the bottom side**
  - **All other components placed at top side**
  - **SMA at port 1**
  - **Port 2 is placed at the position of the DUT's VDD-pin**

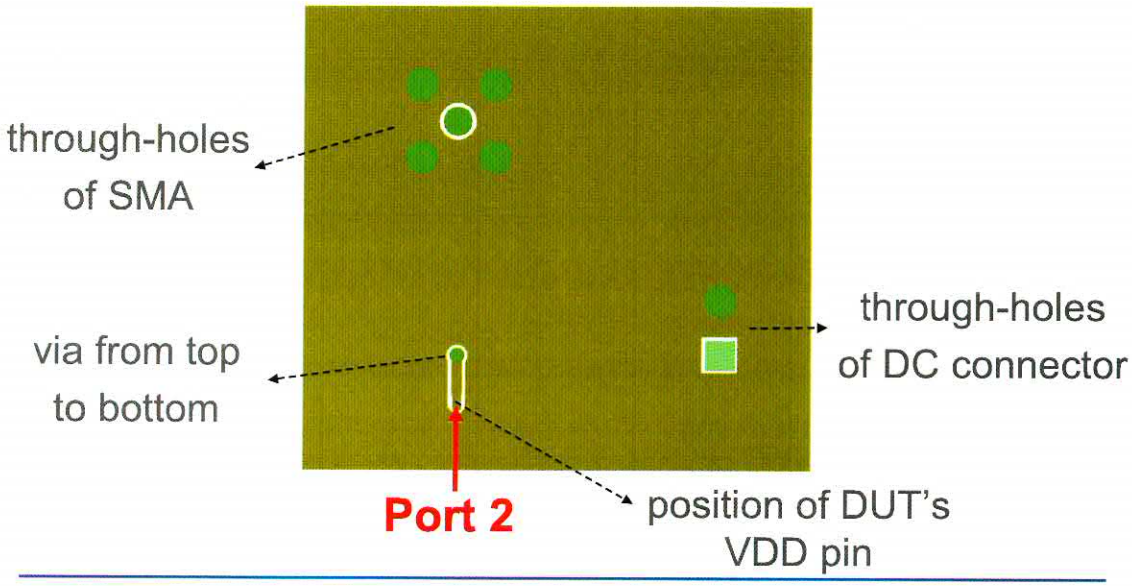
DPI Test Board Design

- Lay-out of the board: top side



DPI Test Board Design

- Lay-out of the board: bottom side



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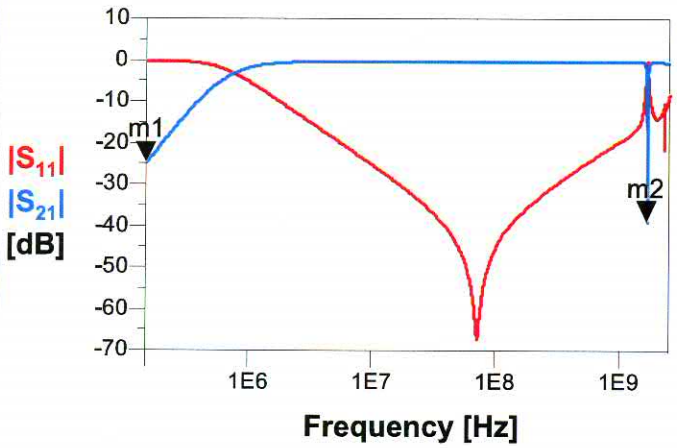
DPI Test Board Design

- Analysis of RF power injection path
  - **initial values of L and C:**
    - **C** = 6.8 nF (as proposed in IEC 62132-4)
    - **L** = 5uH coil



m1: -25 dB @ 150 kHz
m2: -39 dB @ 1.64 GHz

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DPI Test Board Design

- Analysis of RF power injection path

Observations

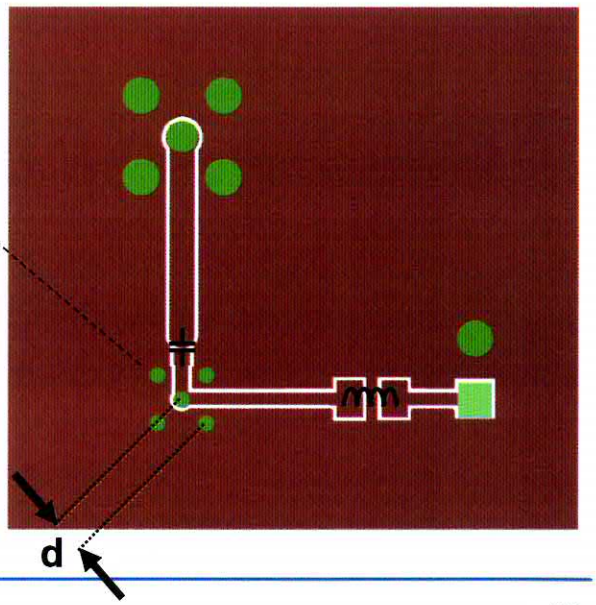
- **Values of the capacitor and inductor are too low**
  => these need to be optimized!!
- **A resonance occurs at 1.64 GHz. This is due to the signal via. As the board is rather thick, the return path is not well-defined. To minimize the flux in the RF-loop, ground vias should be placed near the signal via.**
  => the positions of the ground vias have to be optimized!!

DPI Test Board Design

- New lay-out including ground vias near signal via

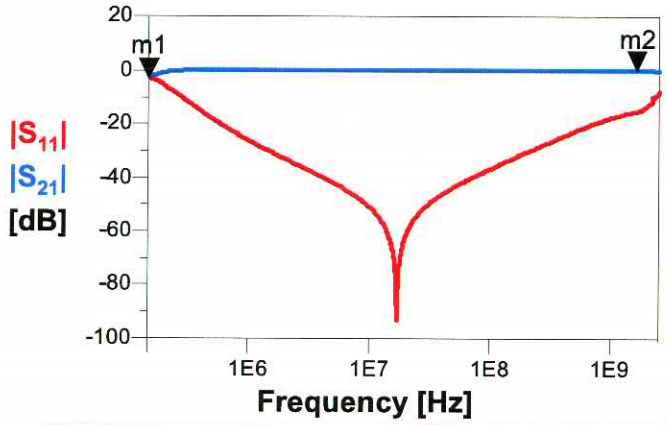
4 ground vias
placed near signal via
to improve flux cancellation

- radius of vias: 0.5 mm
- distance **d**: to be optimized



DPI Test Board Design

- Analysis of RF power injection path
  - **Optimization => minimal required values:**
    - **C** = 18.7 nF
    - **L** = 31.6 uH
    - **d** = 1.20 mm



m1: -2.97 dB @ 150 kHz
m2: -0.12 dB @ 1.64 GHz

Transfer characteristic meets requirements from 150 kHz up to 2.5 GHz!!

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Conclusions

- High-frequency phenomena corrupt (the interpretation of) IC-level EMC tests
- These phenomena, occurring at the board level, can only be accurately determined by EM (field) simulations of the board
- This becomes especially important at frequencies exceeding 1 GHz
- Circuit/field co-optimization leads to rapid, easy, and cheap design of test boards

- Extensions: more complex structures including cross-talk between RF-paths, 4-layer boards, ...

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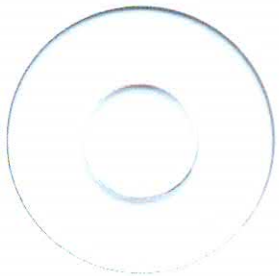

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