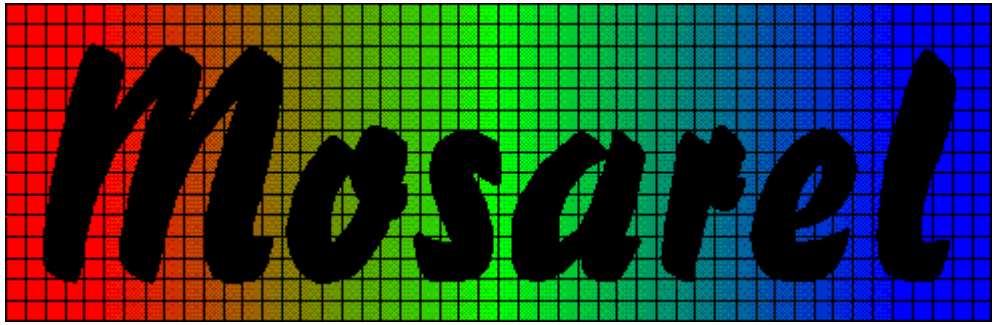

Monocrystalline Silicon Active matrix Reflective Light valve

http://come.to/mosarel

Herbert De Smet, Jean Van den Steen, Dieter Cuypers, Nadine Carchon and André Van Calster,

Imec vzw & Ghent University

Ghent, Belgium

imec

Cupid Microdisplays 2001

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Overview

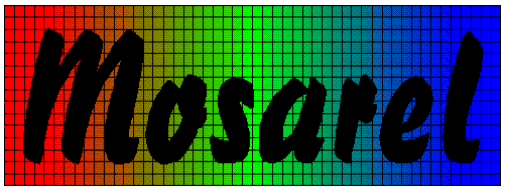
- Introduction
- Technological issues
- Project planning
- Problems test vehicle
- Problems demonstrator
- Successes
- Open issues
- Results
- The future
- Acknowledgements

Introduction

- Idea:
  - Show feasibility of ultra-high resolution Displays in LCOS technology
  - ASIC approach using existing foundry and LCD assembly house

Introduction

- Project data :
  - Esprit project EP25340
  - Start date: 1/9/1997
  - Initial duration: 24 months



- Consortium :

– Alcatel Microelectronics	Si Foundry (Asic house)
– Barco (co-ordinator)	End user
– Imec	Design & back-end tech.
– Thales Avionics (Sextant Avionique)	End user
– Thales Avionics LCD (Thomson LCD)	LCD assembly house
– University of Stuttgart	Study of LC effects

Technological issues

- Chip size
  - active matrix area: 38x31 mm
  - bigger than field size of stepper (20x20 mm)
- Planarization, light shield, reflectivity
- Pixel clock
  - 80 Hz frame rate : 420 MHz pixel clock needed
- Voltage requirements
  - LC: 4-5 Vrms = 8-10 Vpp
  - C07 technology: max. 5 V

Stitching

Back-end

Parallelism

SDEMOS

Technological issues (2)

- Reflective LC effects
  - PDLC, HAN-cell, SCTN, 52-54º RTN, Fréedericksz, DAP (VAN)

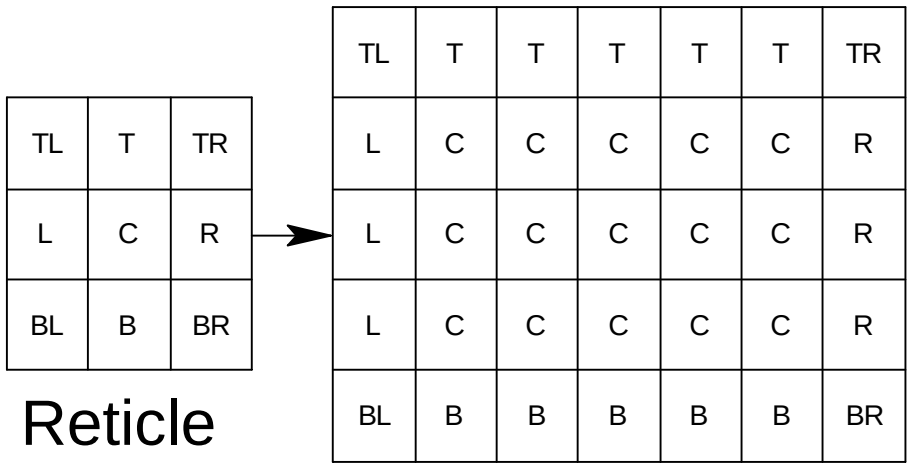
Stuttgart

- Spacer visibility
  - spacer size <≈ pixel size
  - (except VAN)

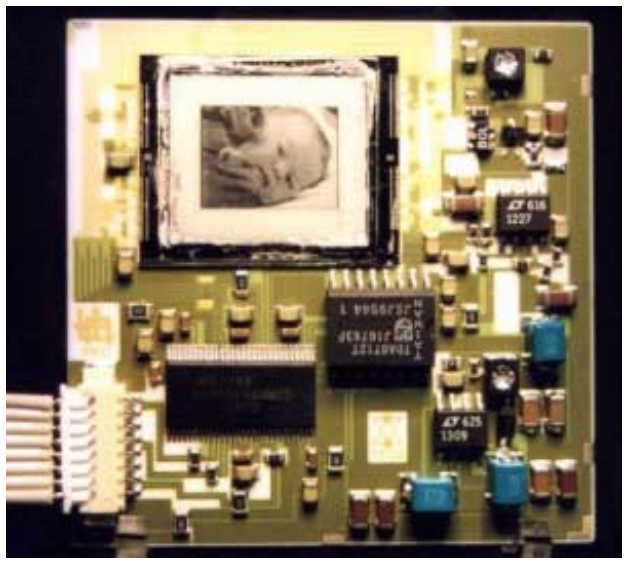
Spacerless

Stitching

- Active Matrix = 38.4x30.7 mm^2
- Stepper lithography: max field size = 20x20 mm^2 = max die size.
- Stitching:
  - split up design in smaller modules that fit on one mask reticle



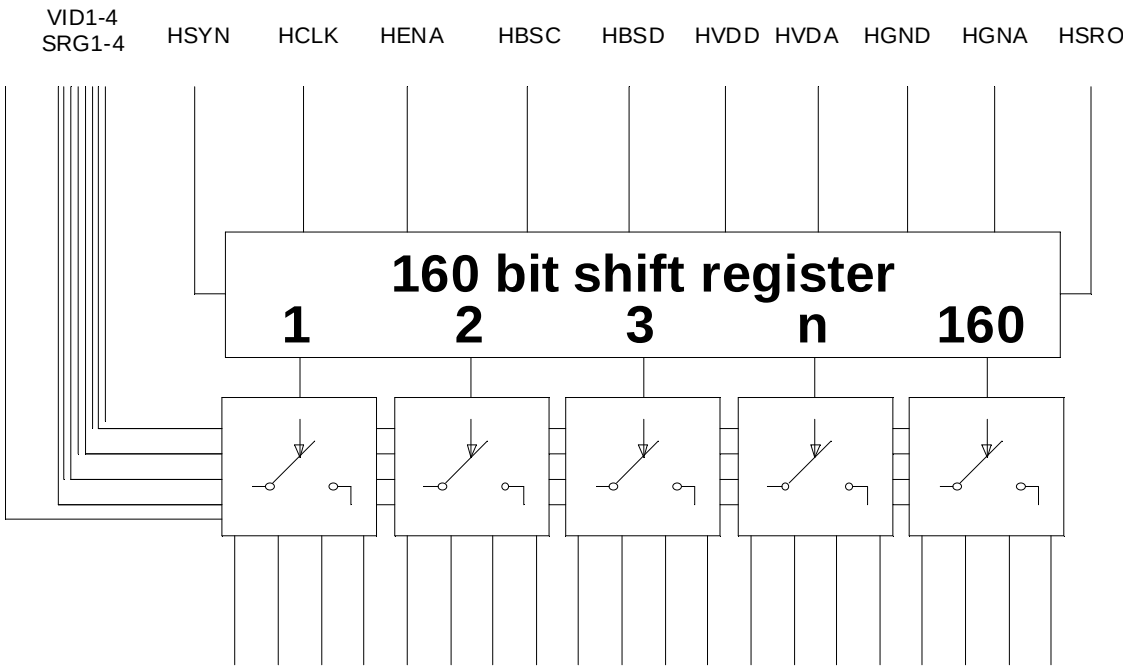
Modified back-end process



- Planarization:
  - organic materials (OLIN)
  - SOG (spin-on glass)
  - CMP (expensive)
- Light shield:
  - Black polyimide (Brewer science DARC)
  - TiN (AR coating)
- Pixel reflectivity
  - unsintered aluminium, cold sputtering

Parallelism in drivers

- GXGA, 80 Hz -> pixel clock = 420 MHz >> .7 µm CMOS
- Parallelism
- 4 x 4 = 16



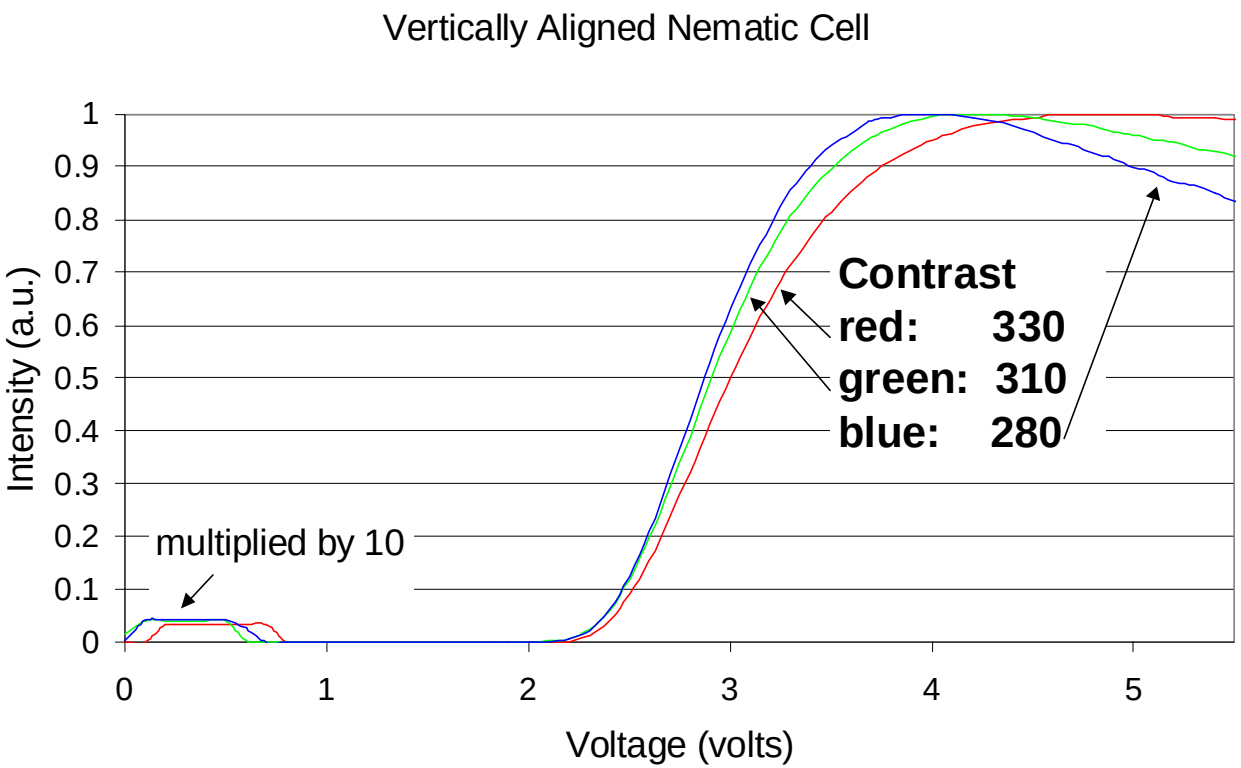
640 columns

SDEMOS

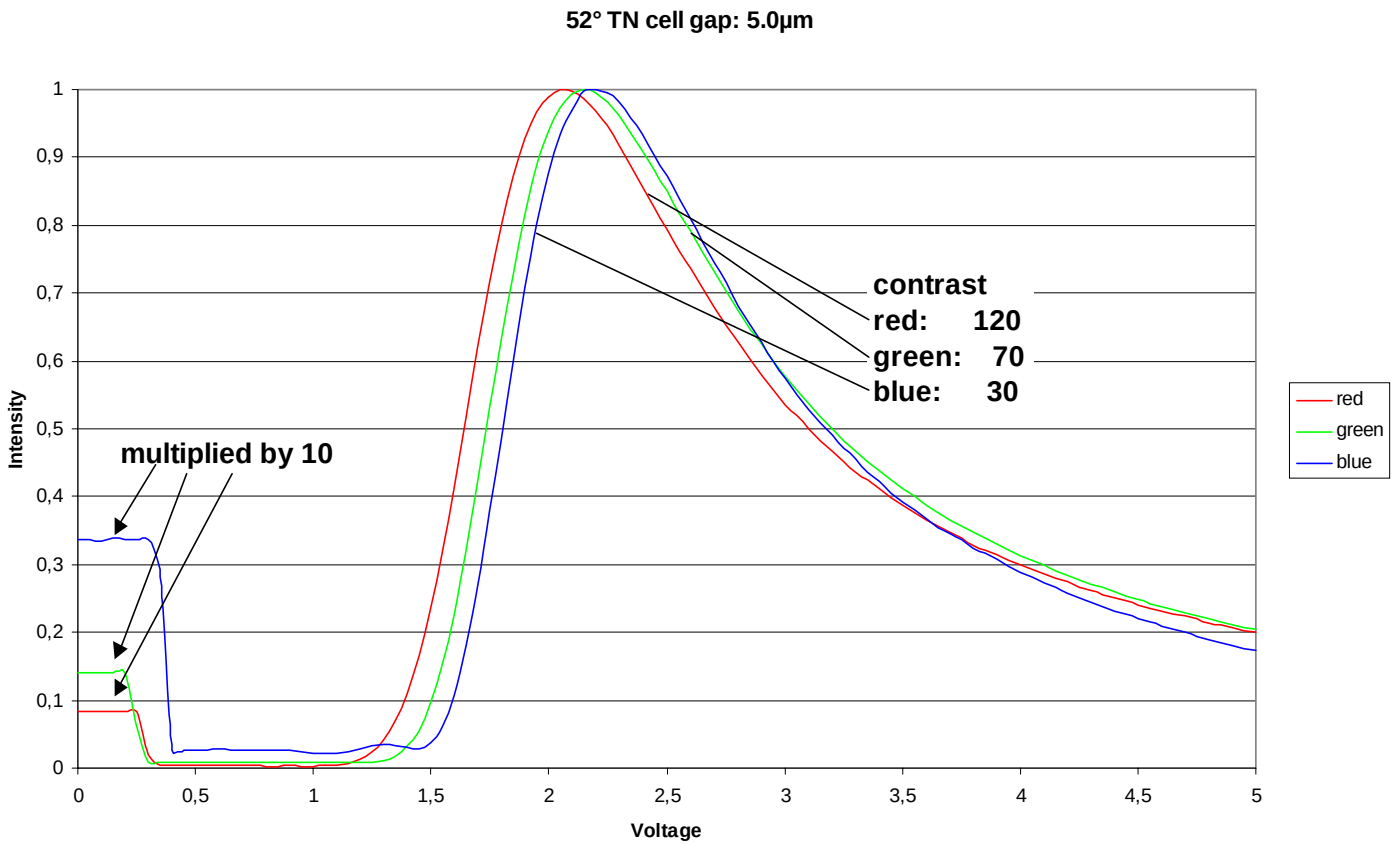
- Reflective LC effects : 4-5 V_{RMS}
- Projector with continuous light source:
  - DRAM type active matrix: no backplane switching
  - $2xV_{RMS}$ to be switched by pixels transistors
  - V_{Gate} : 10-14 V (incl. body effect)
- Mosarel: C07 : max. 5 volts

  $\Rightarrow$ Symmetrical Drain Extended MOS (SDEMOS): up to 15 V

LC effects


Vertically Aligned Nematic Cell
Intensity (a.u.)
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
1
2
3
4
5
Voltage (volts)
multiplied by 10
Contrast
red: 330
green: 310
blue: 280

LC effects (2)

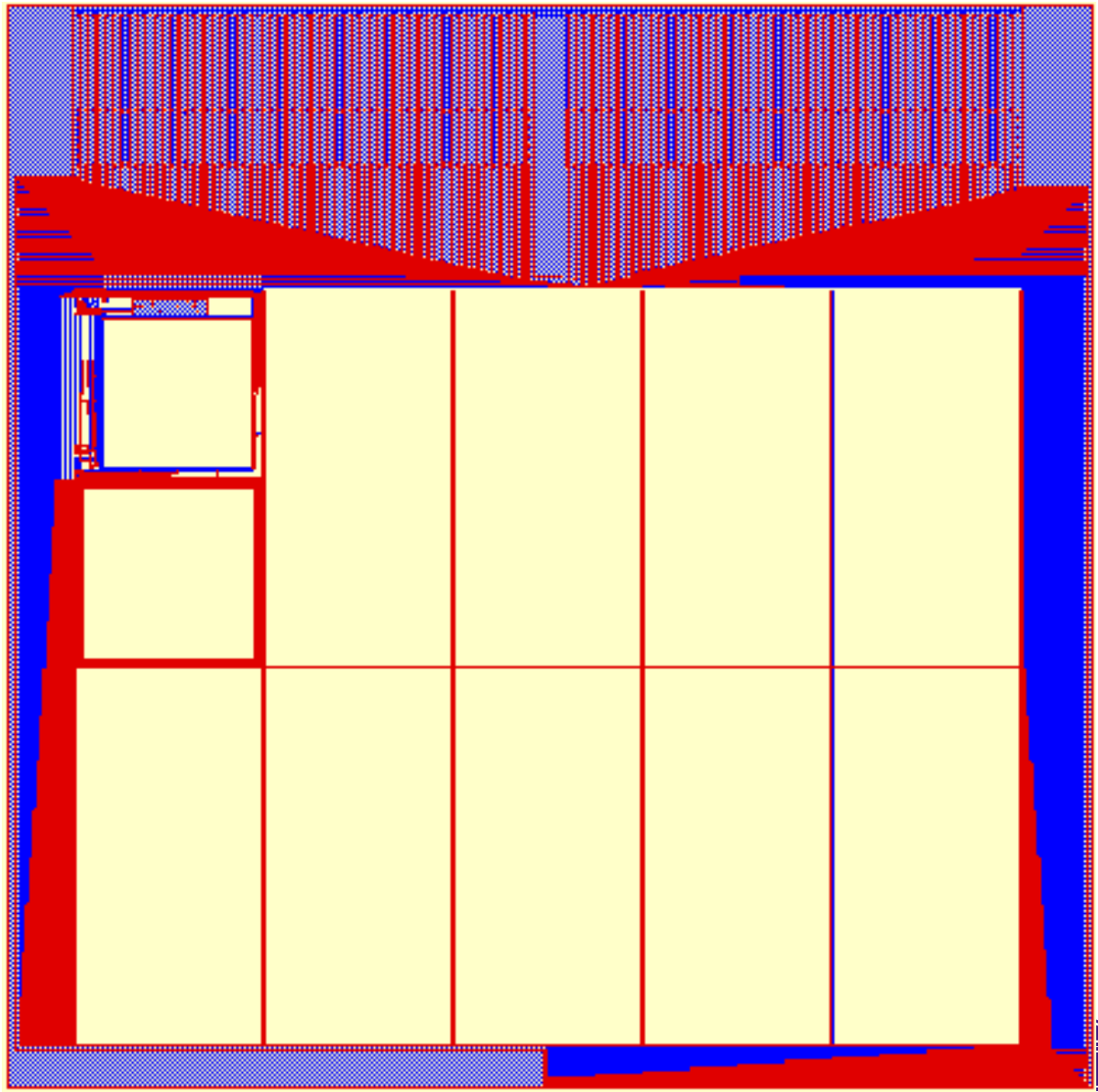

52° TN cell gap: 5.0µm
Intensity
Voltage
contrast
red: 120
green: 70
blue: 30
multiplied by 10
red
green
blue

Project planning

- 2 phases :
  - Test vehicle (15 months)
    - full resolution (2560x2048 pixels)
    - no integrated drivers (addressing in row and column blocks)
    - testing DEMOS pixel transistors
    - testing the back-end technology and stitching
    - testing spacerless assembly
    - electro-optical performance evaluation
  - Final demonstrator (9 months)
    - integrated row and column drivers, with parallelism and redundancy
    - workstation and HUD demonstrator
      - **high-speed peripheral electronics**
      - **optical systems**

Problems test vehicle

- Organic materials incompatible with stepper lithography (5X)
  - back-end process in 1X litho
- Test vehicle w/o integrated drivers (block addressing):
  - routing around matrix not repetitive - not stitchable
  - routing in 1X, matrix in 5X (back-end in 1X tech.)
- Design: mix & match 1X & 5X lithography + stitching = trouble
- Processing: mix & match in 2 different clean rooms (Leuven - Oudenaarde)
- Shorts (1): (massive short all rows & columns)
  - due to conductive stringers between 1X and 5X
- Shorts (2): (many shorted blocks)
  - due to 1X litho in matrix region + block structure of T.V.



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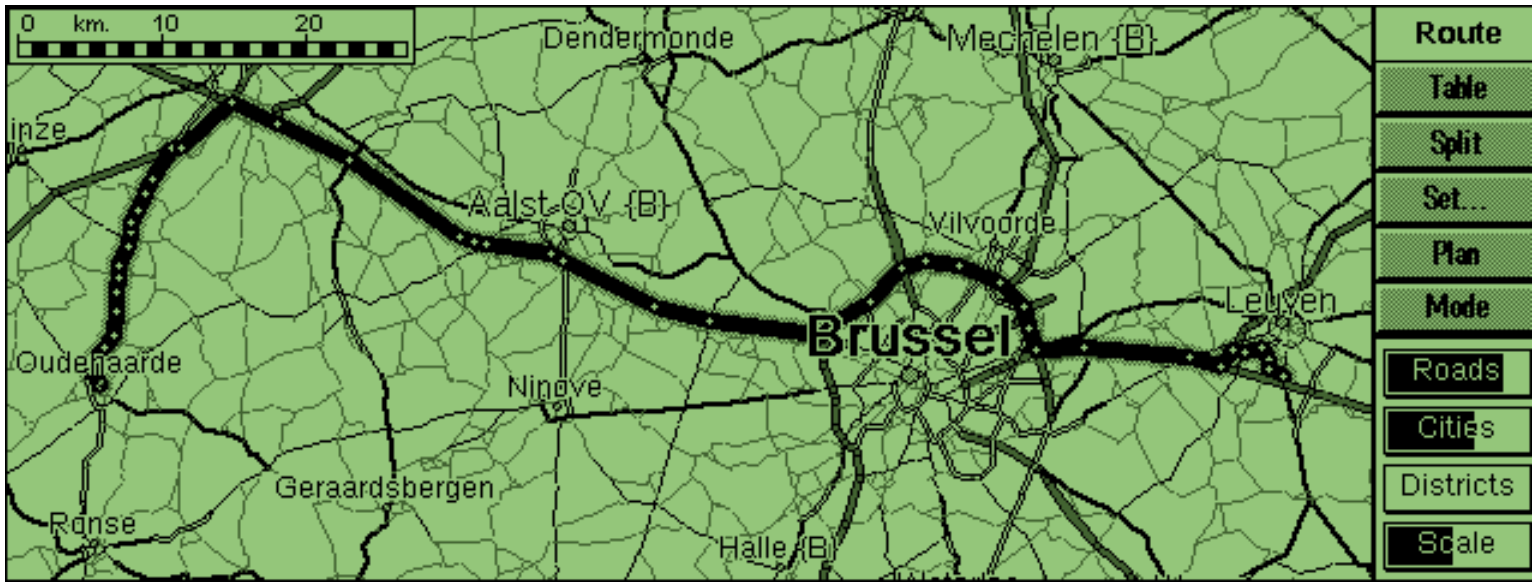
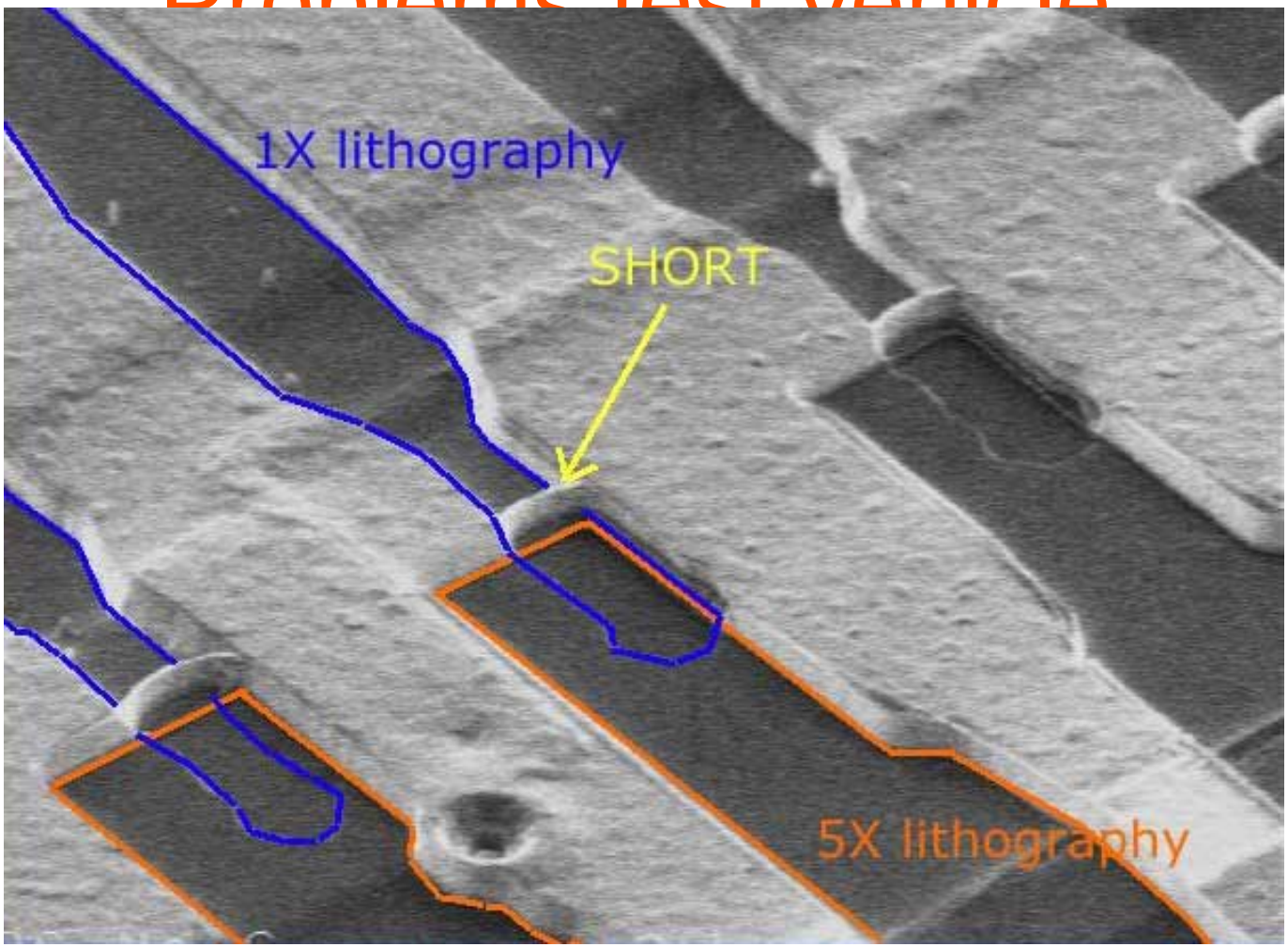
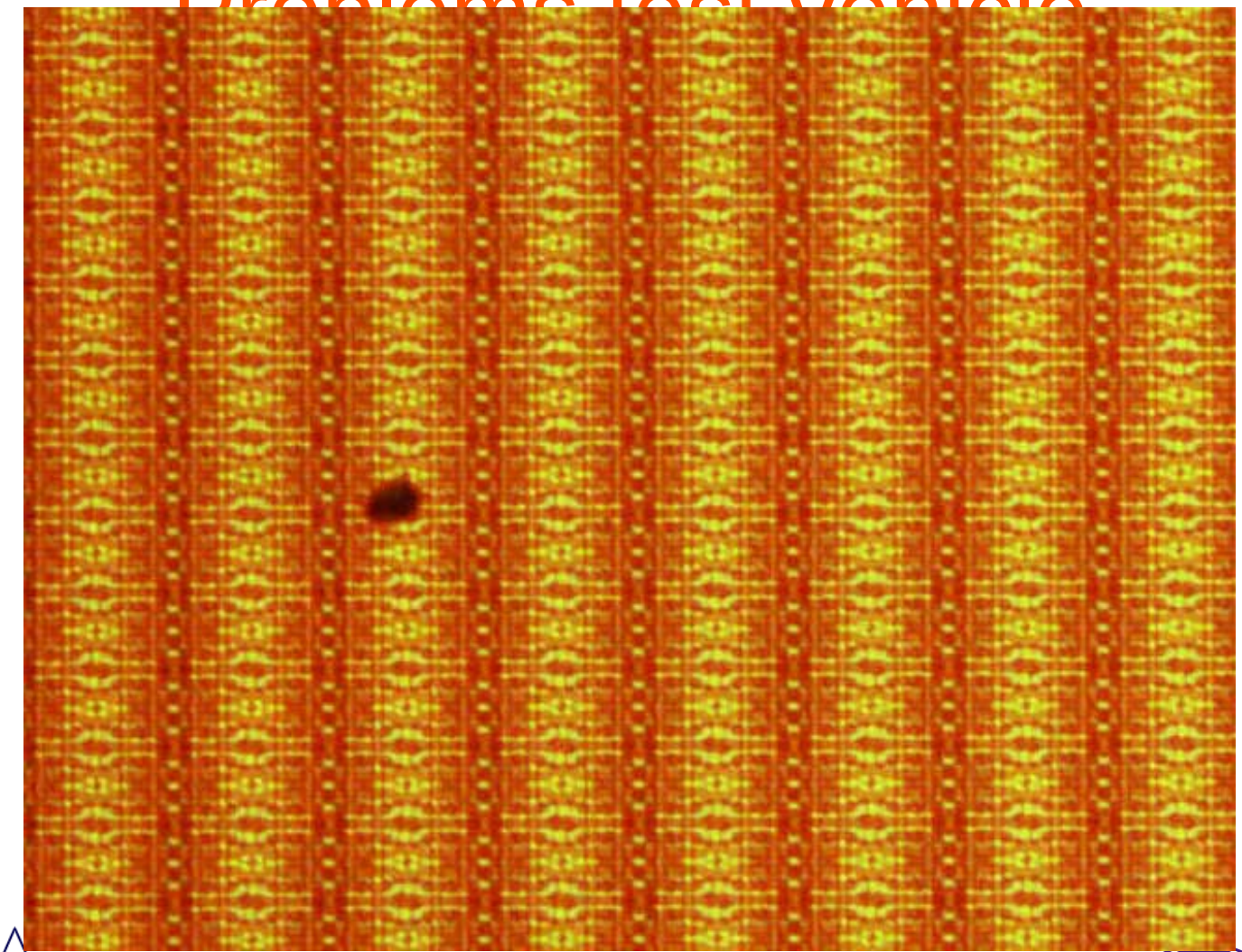
Problems test vehicle



Problems test vehicle



Problems test vehicle



Problems test vehicle (2)

- several months delay accumulated

Change of plan:

- Abandon organic material based back-end process
  - TiN light shield and CMP planarization
- Final demonstrator completely in 5X stepper lithography (no mix & match)

Problems demonstrator

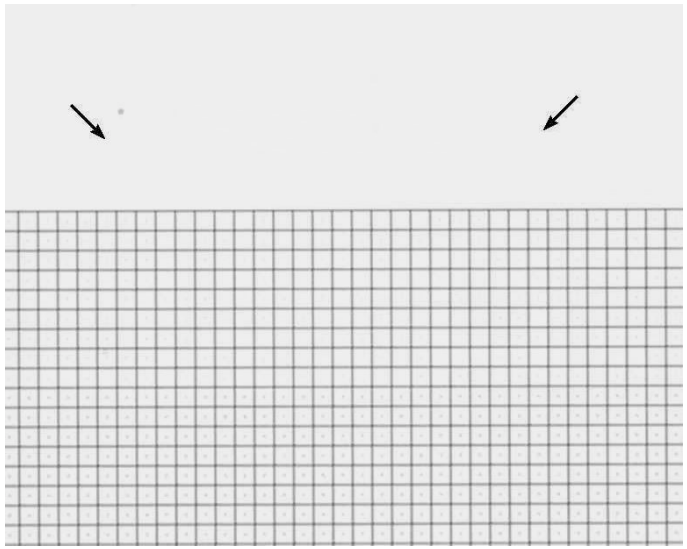
- Automatic design rule checking not compatible with stitching
  - Manual checking necessary
- Redundancy features of drivers contain error:
  - Drivers work but reduced redundancy
- Shorts (3)
  - due to CMP step
  - would require redesign and more CMP steps (like C035 process)

Successes

- Stitching
- DEMOS
- pixel aperture ratio
- pixel planarity
- Al reflectivity
- light shield
- driver design (except redundancy)
- spacerless assembly in test vehicle

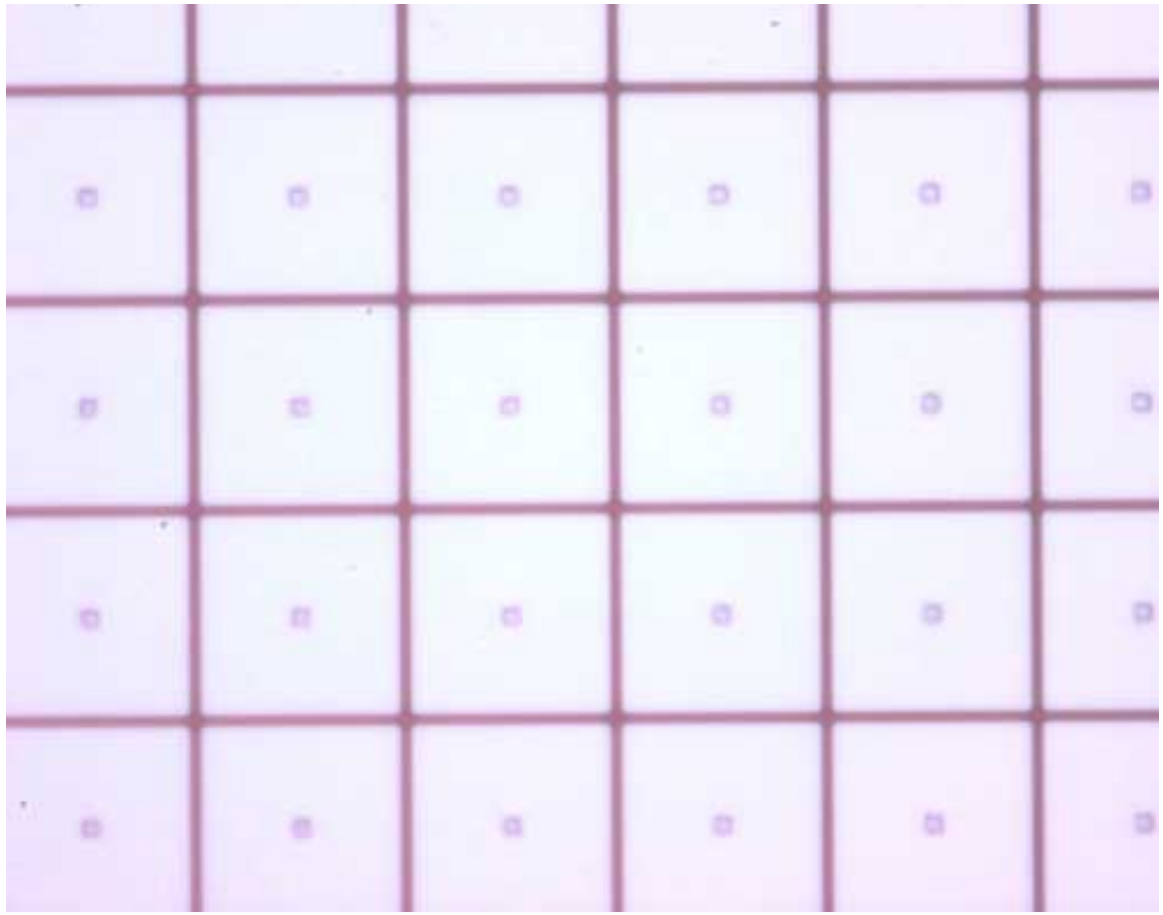
Stitching

- Technical result very good:
  - < 50 nm positioning error
  - stitching lines nearly invisible



  - makes different display formats possible with one mask set: GXGA, SXGA, XGA-p

Pixel aperture ratio

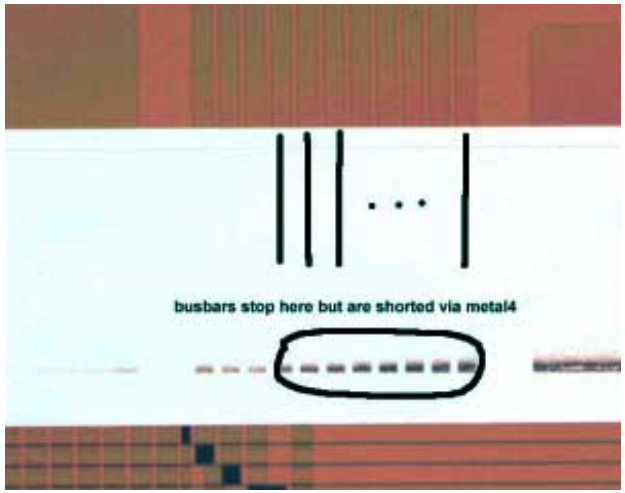


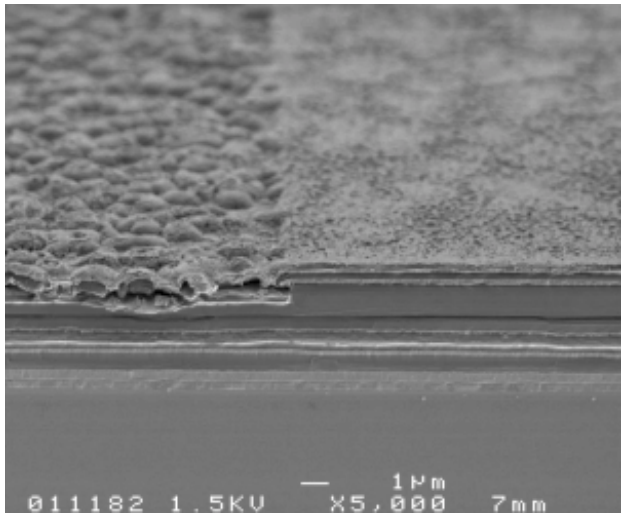
Open issues

- CMP shorts
- planarity outside matrix
- spacerless assembly of demonstrator
- redundancy in driver circuit
- yield (?)

CMP

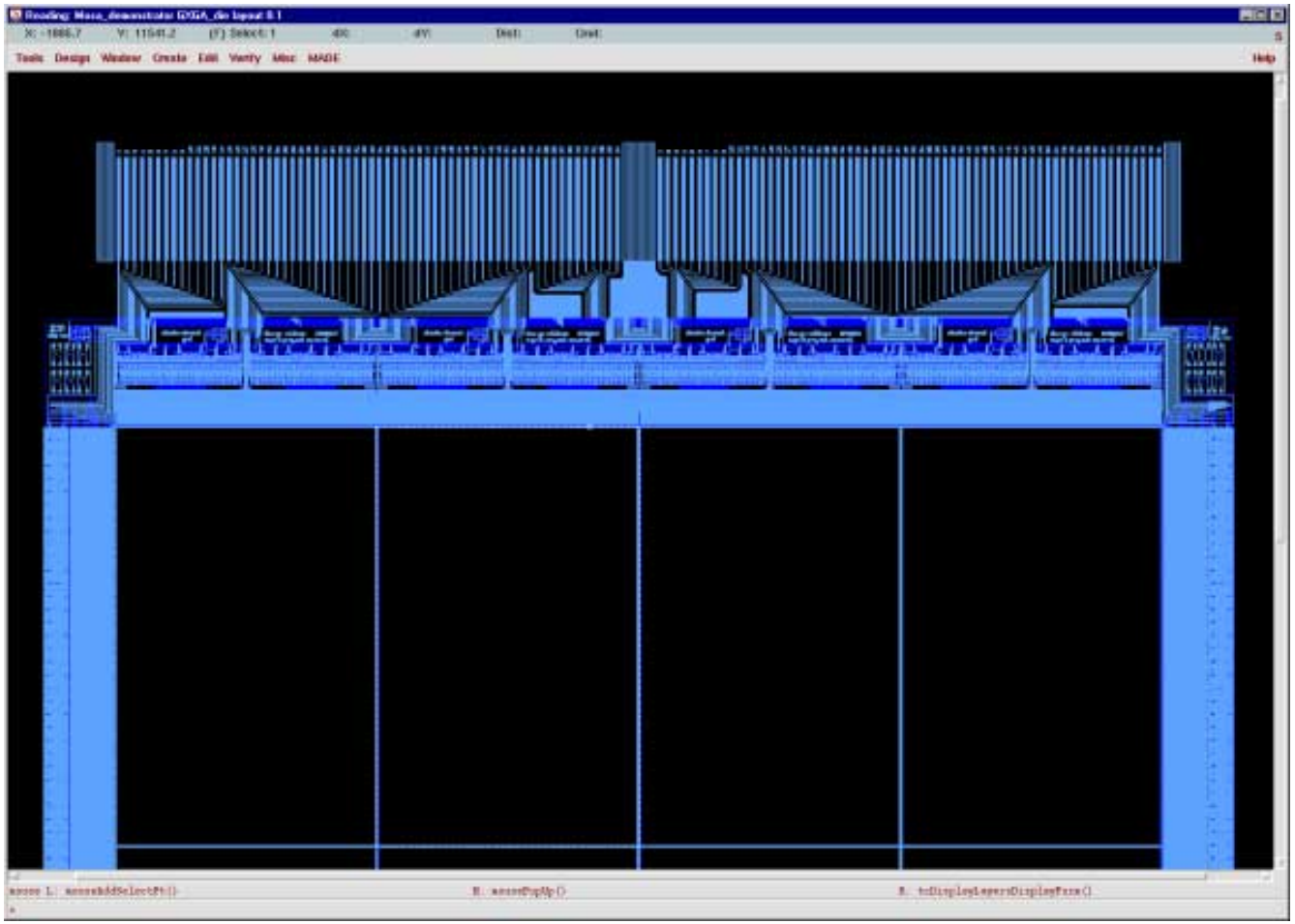
- Shorts



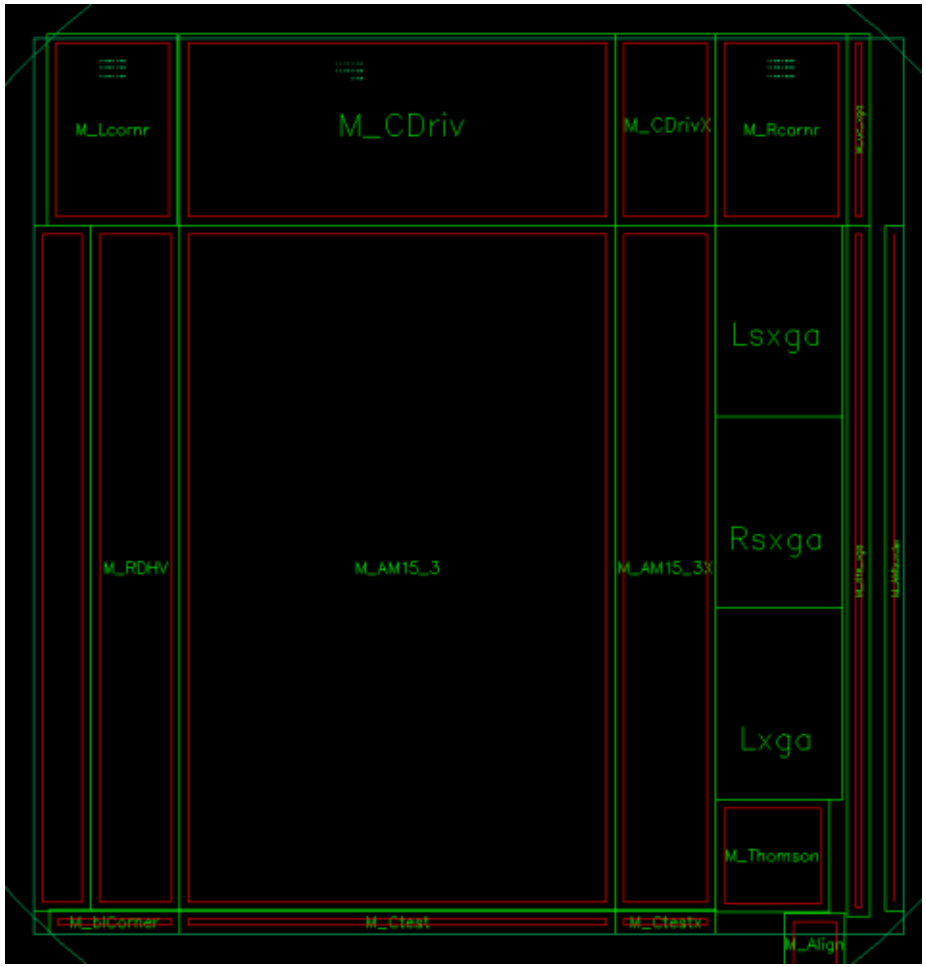


- Chip topology must be limited
  - Dummy metal algorithms:
    - Difficult to combine with stitching
  - More difficult for larger chips

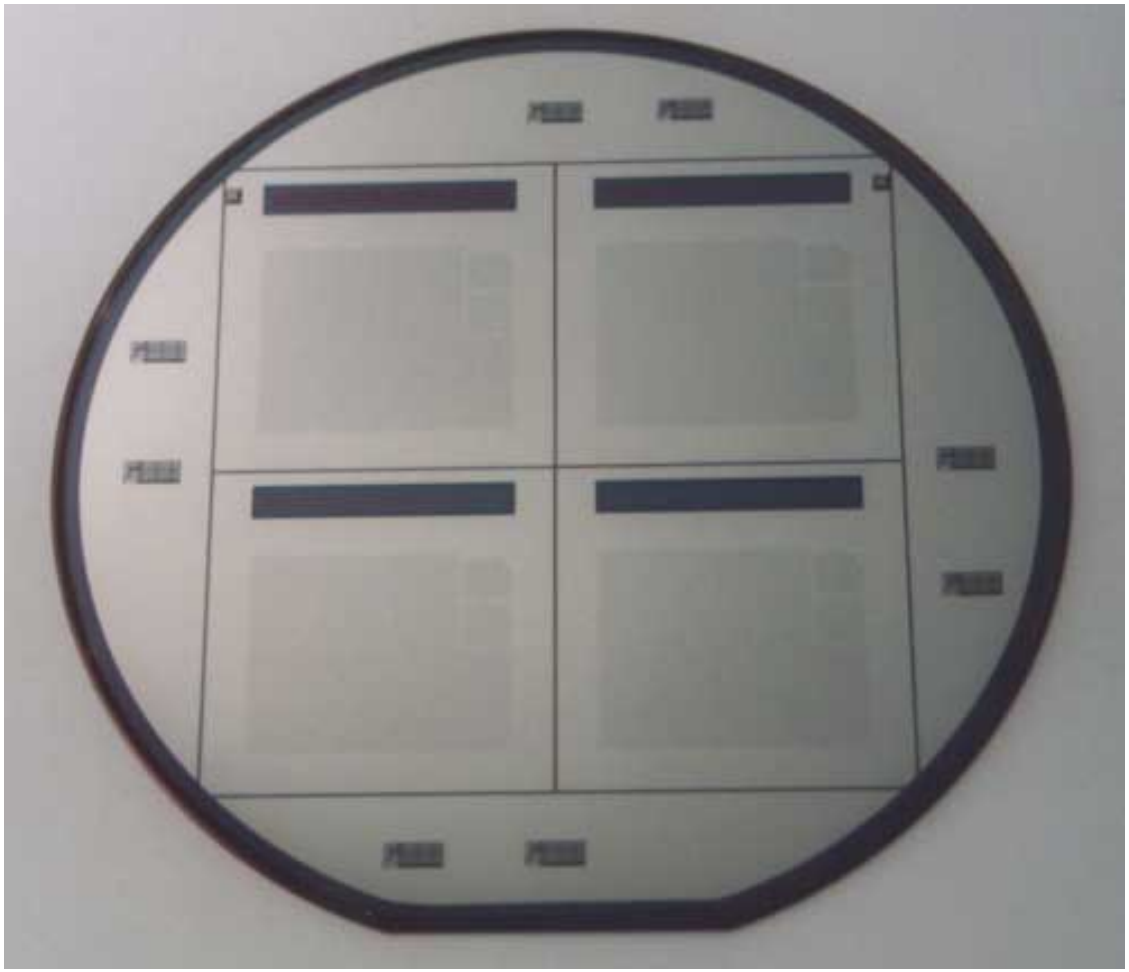
Results



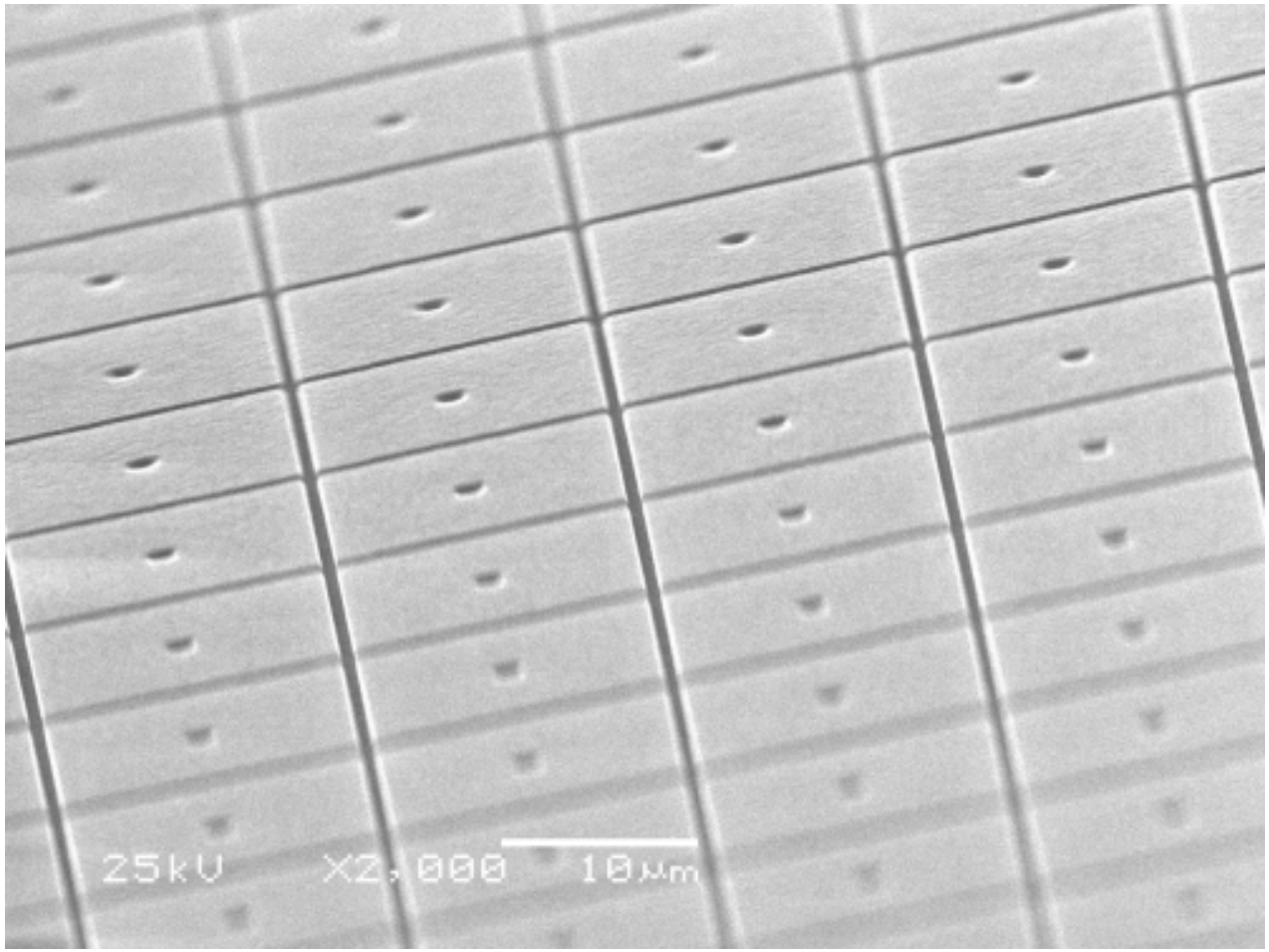
Results


M_Lcornr
M_CDriv
M_CDrivX
M_Rcornr
Lsxga
Rsxga
Lxga
M_RDHV
M_AM15_3
M_AM15_3X
M_Thomson
M_blCorner
M_Ctest
M_Ctestx
M_Align

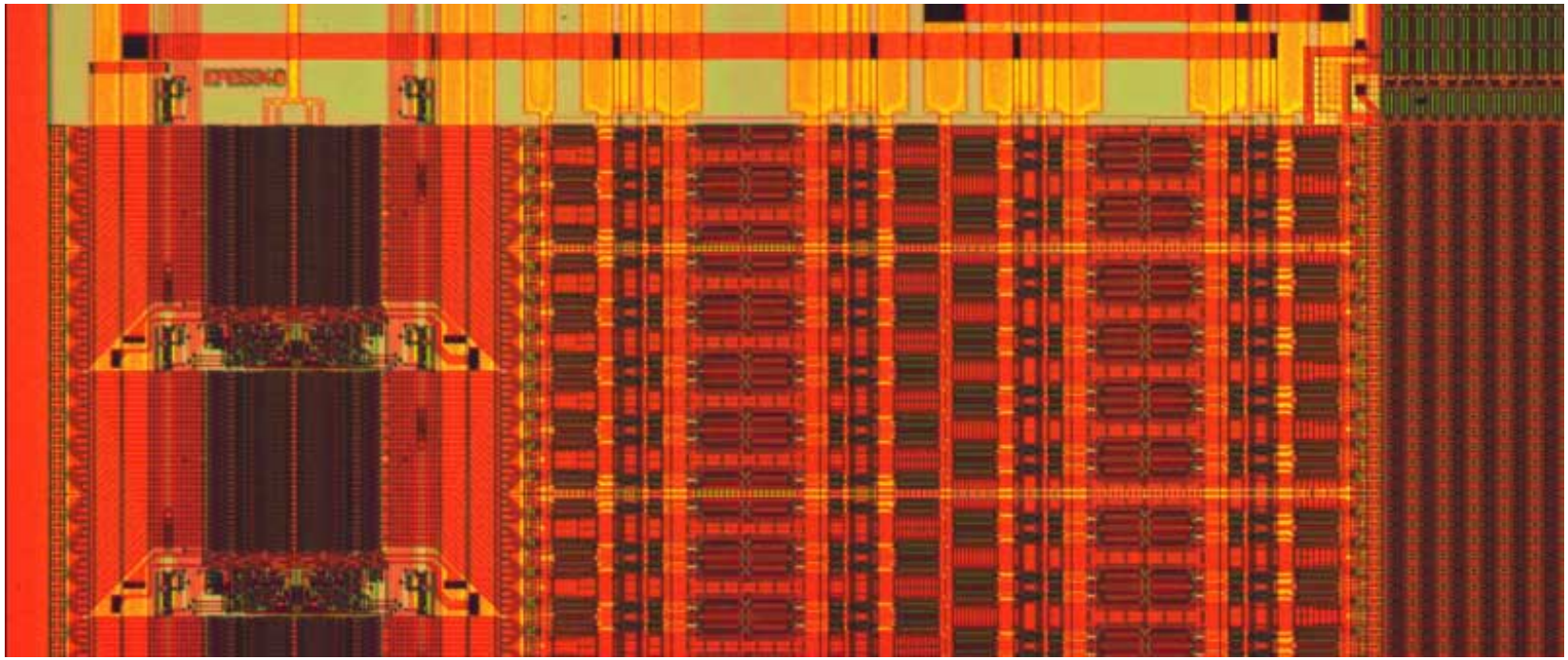
Results



Results

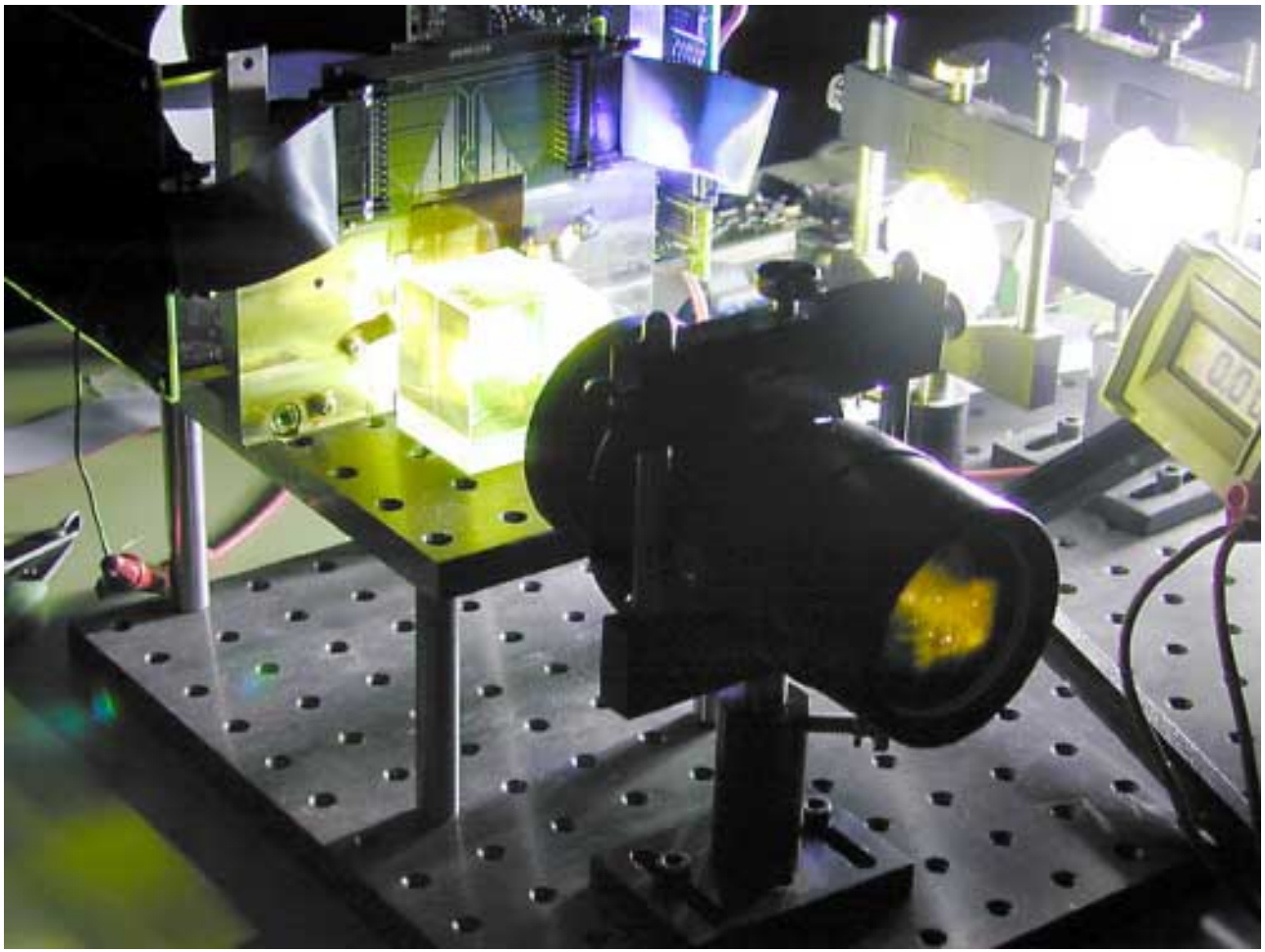


Results

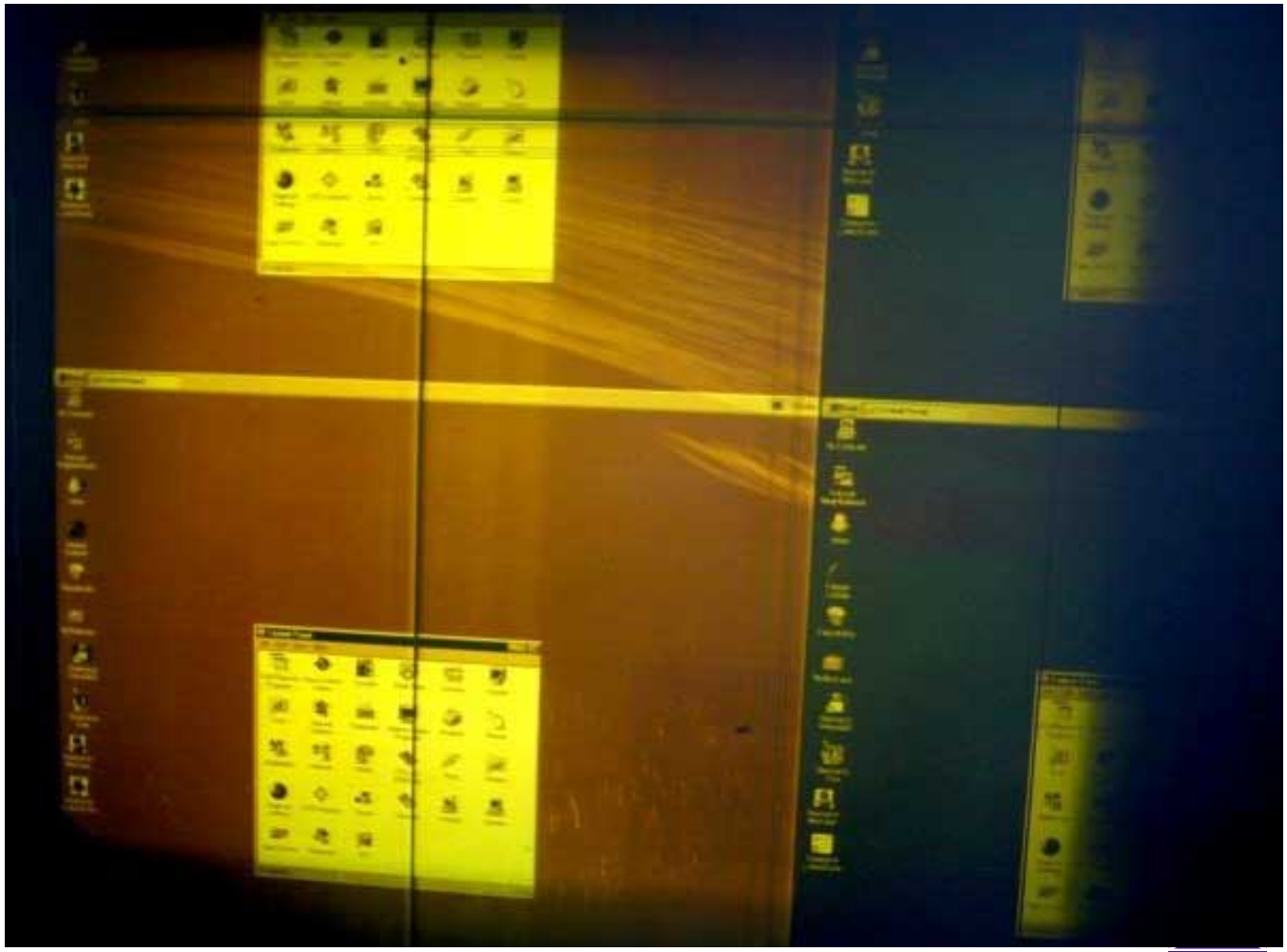


Results

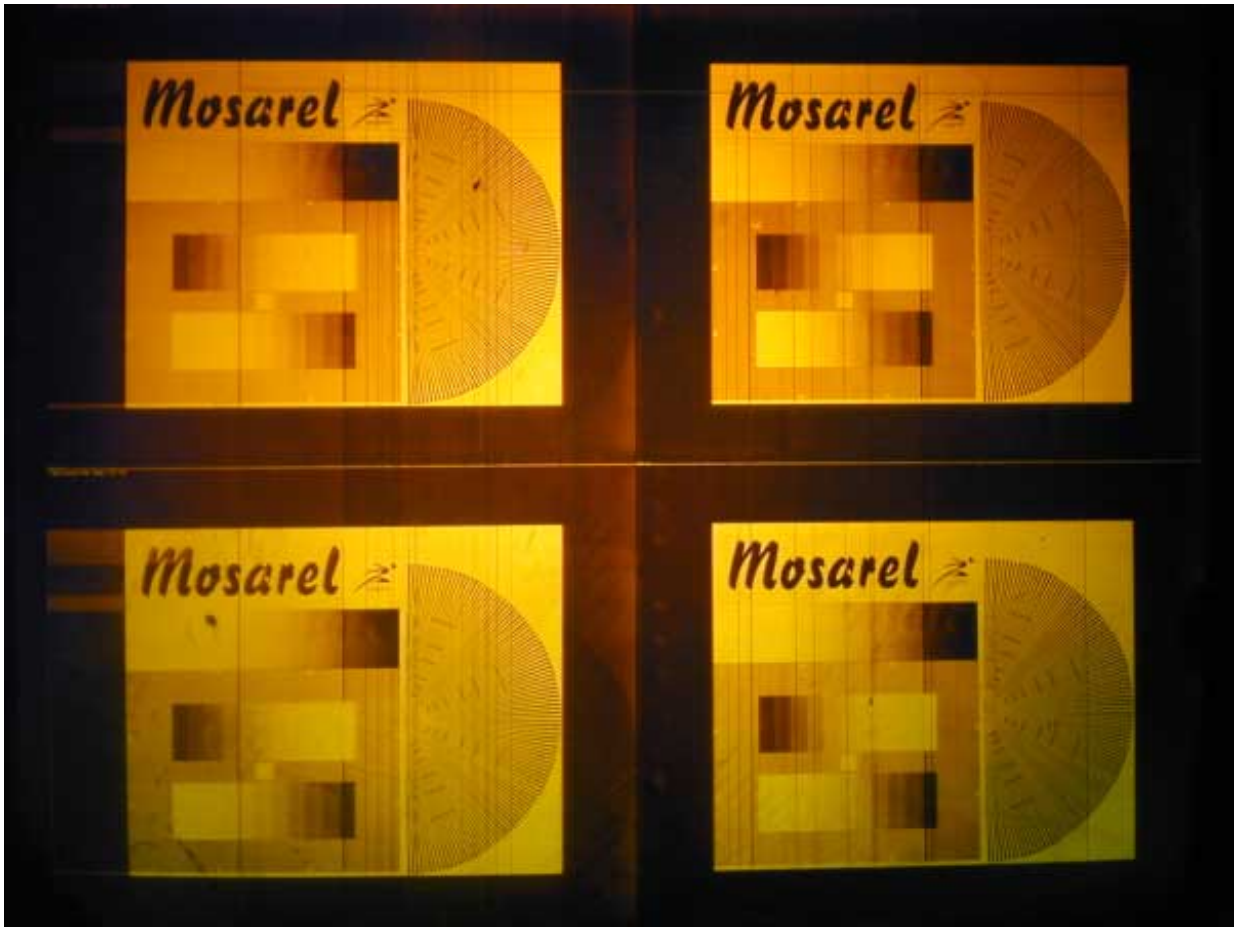
Results



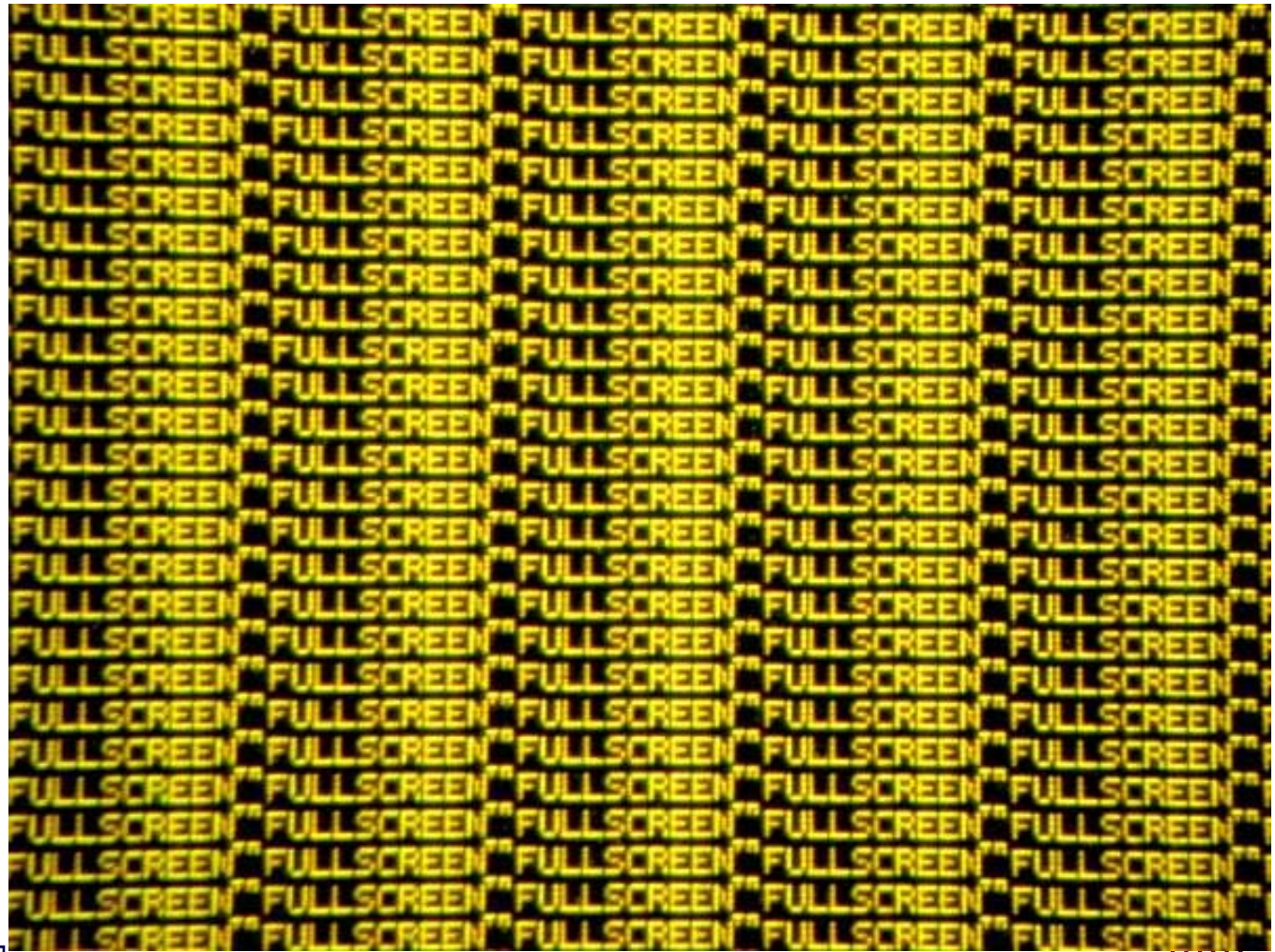
Results



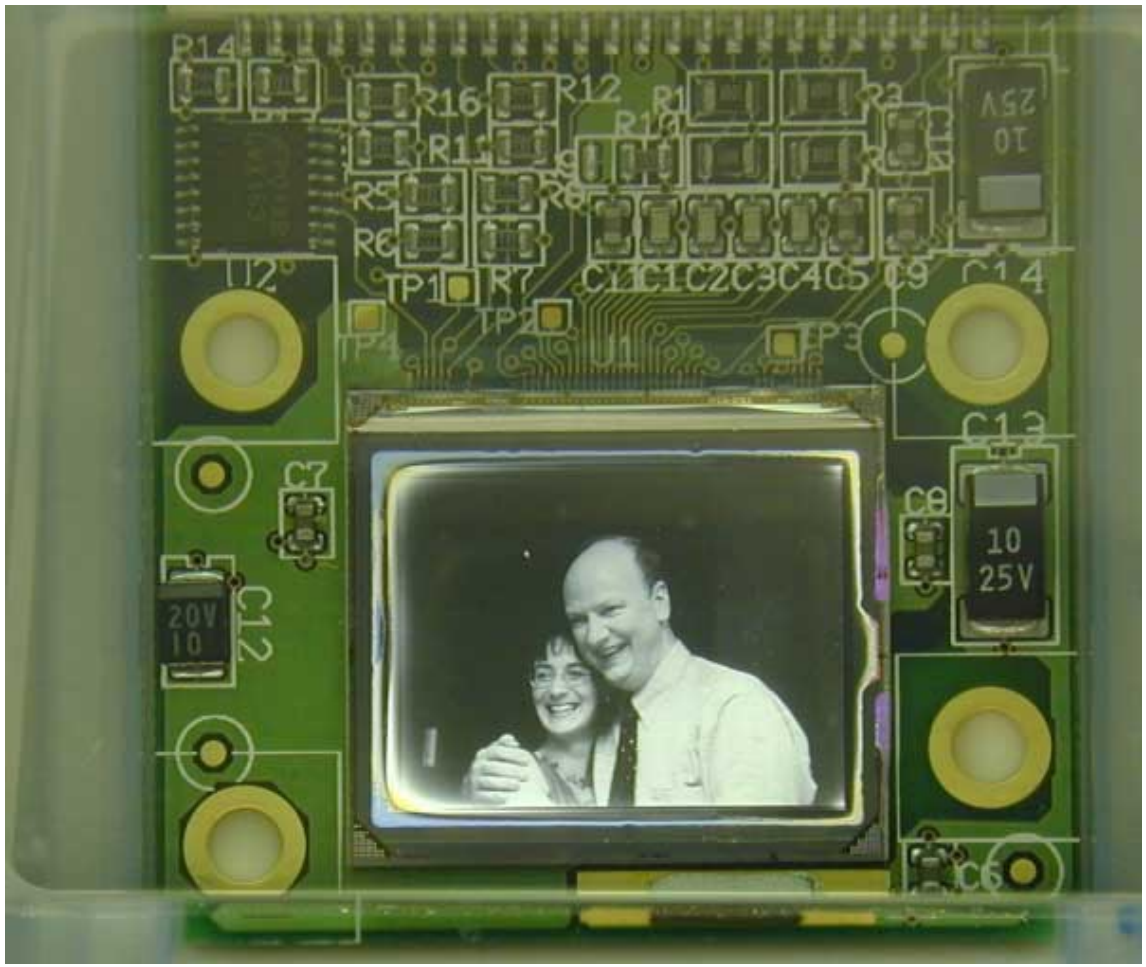
Results



Results



The future


R14
R16
R12
R1
R5
R6
TP1
R7
C1
C2
C3
C4
C5
C9
C14
U2
C7
C8
C12
20V
10
10
25V
C6

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