Aansturing van modulatoren met meerdere kanalen aan hoge snelheid en laag vermogenverbruik voor middellange optische verbindingen

High-Speed Low-Power Modulator Driver Arrays for Medium-Reach Optical Networks

Renato Vaernewyck

Promotoren: prof. dr. ir. J. Bauwelinck, prof. dr. ir. X. Yin
Proefschrift ingediend tot het behalen van de graad van
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Gent, november 2014

Renato Vaernewyck

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List of Acronyms

A

AC	Alternating Current
ADSL	Asymmetric Digital Subscriber Line
AM	Amplitude Modulation
AM-PSK	Amplitude Modulation Phase Shift Keying
ASE	Amplified Spontaneous Emission
ATM	Asynchronous Transfer Mode
AWG	Arrayed Waveguide Grating

B

B2B	Back-To-Back
BER	Bit Error Rate
BERT	Bit-Error Rate Tester
BJT	Bipolar Junction Transistor
BPF	Band Pass Filter
B-PON	Broadbrand Passive Optical Network

C

CFP	Centum Form-factor Pluggable
CM	Common Mode
CMFB	Common Mode Feedback

CML	Current-Mode Logic
CMOS	Complementary Metal Oxide Semiconductor
CO	Central Office
CPON	Composite Passive Optical Network
CW	Continuous Wave
CWDM	Coarse Wavelength Division Multiplexing

D

DAF	Delay-and-Add Filter
DB	Duobinary
DBR	Distributed Bragg Reflector
DC	Direct Current
DFB	Distributed Feedback
DSF	Dispersion Shifted Fibers
DS	Downstream
DSL	Digital Subscriber Line
DSP	Digital Signal Processing
DWDM	Dense Wavelength Division Multiplexing

E

EAM	Electro Absorption Modulator
ECL	Emitter Coupled Logic
EDFA	Erbium Doped Fiber Amplifier
EML	Electroabsoption Modulated Laser
EOM	Electro Optic Modulator
EPON	Ethernet Passive Optical Network
ER	Extinction Ratio

F

FEC	Forward Error Correction

FET	Field Effect Transistor
FIR	Finite Impulse Response
FKE	Franz-Keldysh Effect
FoM	Figure of Merit
FP	Fabry-Perot
FTTB	Fibre To The Business/Building
FTTC	Fibre To The Cabinet/Curb
FTTH	Fiber To The Home
FWHM	Full-Width Half-Maximum

G

Gb/s	Gigabit per second
GCPW	Grounded Coplanar Waveguide
GE-PON	Gigabit Ethernet Passive Optical Network
G-PON	Gigabit-capable Passive Optical Network

H

HiCuM	High Current Model

I

IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IM	Intensity Modulation
I/O	Input/Output
ISI	Inter Symbol Interference
ISP	Internet Service Provider
ITU	International Telecommunications Union

L

LASER	Light Amplification by Stimulated Emission of Radiation
LED	Light Emitting Diode
LPF	Low Pass Filter

M

MEMS	Micro-Electro-Mechanical Systems
MLM	Multiple-Longitudinal Mode
MQW	Multi Quantum Well
MZI	Mach-Zehnder Interferometer
MZM	Mach-Zehnder Modulator

N

NG-PON	Next Generation Passive Optical Network
NRZ-OOK	Non-Return-to-Zero On/Off Keying

O

ODB	Optical Duobinary
OLT	Optical Line Termination
ONU	Optical Network Unit
OSNR	Optical Signal-to-Noise Ratio

P

P2MP	Point-to-MultiPoint
P2P	Point-to-Point
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PDU	Power Distribution Unit
PIC	Photonic Integrated Circuit
PIN	Positive-Intrinsic-Negative
PON	Passive Optical Network
PPG	Pulse Pattern Generator
PRBS	Pseudo Random Bit Sequence
PRS	Partial Response Signaling
PSK	Phase Shift Keying
PWC	Pulse Width Control
PWD	Pulse-Width Distortion

Q

QCSE	Quantum Confined Stark Effect
QW	Quantum Well

R

REAM	Reflective Electro Absorption Modulator
RF	Radio Frequency
RFC	Radio Frequency Choke
RITENET	Remote Interrogation of Terminal Network
RN	Remote Node
RSOA	Reflective Semiconductor Optical Amplifier
RX	Receiver

S

SG-DBR	Sampled Grating Distributed Bragg Reflector
SLM	Single-Longitudinal Mode
SMF	Single Mode Fiber
SNR	Signal-to-Noise Ratio
SOA	Semiconductor Optical Amplifier
SPI	Serial Peripheral Interface
SS	Spectral Slicing

T

TDM	Time Domain Multiplexing
TDMA	Time-Division Multiple Access
TDR	Time Domain Reflectometry
TEC	Thermo-Electric Cooler
TX	Transmitter

U

UI	Unit Interval
UPS	Uninterruptable Power Supply
US	Upstream
UDWDM	Ultra Dense Wavelength Division Multiplexing

V

VCSEL	Vertical Cavity Surface Emitting Laser
VDSL	Very-high-bitrate Digital Subscriber Line
VOA	Variable Optical Attenuator

W

WDM	Wavelength Division Multiplexing

Nederlandstalige samenvatting –Dutch Summary–

Het internet is de dag van vandaag alomtegenwoordig en heeft het leven van vele burgers over de hele wereld veranderd. Handel, overheid, industrie, gezondheidszorg en sociale interacties gebruiken in toenemende mate internetapplicaties als een verbeterde en makkelijke manier van communiceren. Video applicaties zijn hier het grote voorbeeld van en vragen steeds grotere data snelheden en betere kwaliteit van de netwerken. Hogedefinitietelevisie (HDTV) diensten springen als paddenstoelen uit de grond en eisen nadrukkelijk een uitbouw van wijdverspreide netwerken met steeds grotere bandbreedtes.

De huidige passieve optische netwerken (PONs) gebruiken een enkele golflengte voor stroomafwaartse transmissie en een aparte golflengte voor stroomopwaartse transmissie. Door golflengtemultiplexering (WDM) in een PON toe te passen, kunnen veel grotere bandbreedtes in beide richtingen bereikt worden. Terwijl WDM technologieën al jaren worden gebruikt in lange-afstandsnetwerken, zijn ze slechts beperkt aanwezig in toegangsnetwerken. De hoge kost om complete WDM toegangsnetwerken uit te bouwen is de belangrijkste oorzaak hiervoor. Anderzijds kan het hedendaagse optische netwerk de capaciteit voor de toekomstige gebruikers niet bereiken op een kostenefficiënte manier. Bijgevolg is er een grote nood aan nieuwe WDM toegangscomponenten die zowel compact als kostenefficiënt zijn en in grote volumes kunnen geproduceerd worden.

Een toename van het aantal golflengtes voor WDM-PON leidt automatisch tot meerdere zend-ontvangers voor de verschillende golflengtekanalen, wat de totale fysische plaatsinname aanzienlijk vergroot. Fotonische integratie van zend-ontvangers tot een geïntegreerde reeks zou de kost en fysische plaatsinname gevoelig reduceren. Het totale vermogenverbruik van zo'n geïntegreerde reeks vormt echter een probleem. Om het gebruik van thermoëlektrische koeling te vermijden, is de integratiedichtheid van de

componenten streng gelimiteerd door de warmteverspreiding van de componentverpakking. Bijgevolg vereist the WDM-PON visie een vermindering van het vermogenverbruik van de zend-ontvanger.

Dit betoog geeft duidelijk de voornaamste uitdagingen bij de realisatie van toekomstbestendige, optische (toegangs)netwerken weer. Zowel een inperking van de fysische plaatsinname, als een verlaging van de kosten en de reductie van het vermogenverbruik van de actieve componenten zijn problemen die moeten aangepakt worden.

In die zin zou een 100 Gb/s component, dat bestaat uit 10 kanalen aan 11.3 Gb/s per golflengtekanaal, een uitstekende bijdrage zijn bij de uitbreiding van de bandbreedte die klanten ter beschikking krijgen. Vooral optische zenders, die werken aan hoge snelheden, hebben een aanzienlijk vermogenverbruik. De hittegeneratie veroorzaakt door dit vermogenverbruik vormt een vervelende hindernis in de ontwikkeling van 10-kanaalszenders. Dit onderstreept nog eens het belang van het vermogenverbruik.

Naast de invoering van WDM in de toegangsnetwerken, zou een punt-tot-punt connectie in datacenteromgevingen ook gebaat zijn met de WDM visie. Aangezien datacenteroperatoren dikwijls lijden aan een tekort aan optische vezels of hun vezelinfrastructuur niet zelf bezitten, zijn WDM technologieën essentieel om hun bereik en capaciteit uit te breiden. Interdatacentercommunicatie heeft ook baat bij kleine, kosten- en energie-efficiënte componenten die werken bij hoge snelheden om hun doorvoercapaciteit te maximaliseren. Bijgevolg zijn geïntegreerde 100 Gb/s zend-ontvangers, zoals 4 kanalen aan 28 Gb/s, uiterst gewenst.

Het werk beschreven in deze thesis werd gedeeltelijk gefinancierd door het Europese FP7 project C3PO (Colourless and Coolerless Components for low Power Optical Networks) en door het UGent bijzonder onderzoeksfonds (BOF). Het C3PO project streefde naar de ontwikkeling van een nieuwe generatie 'groene' Si-fotonische compatibele componenten met een uiterst laag vermogenverbruik en terzelfdertijd wou men een toename in bandbreedte en een afname in kost bereiken. C3PO stelde zich de uitbouw van een toegangsnetwerk met grote capaciteit tot doel, gebruikmakend van reflecterende fotonische componenten. Om dit te bereiken, was het noodzakelijk om kostenefficiënte reflecterende zenders gebaseerd op electroabsorptie modulatoren (EAM) dicht bij elkaar te plaatsen in geïntegreerde reeksen. Een optische bron die meerdere golflengtes produceert voorziet de nodige golflengtekanalen, zowel voor de stroomafwaartse als voor de stroomopwaartse signalen in de WDM-PON.

Hoofdstuk 1 geeft een kort overzicht van het PON-netwerk en beschrijft de voornaamste implementaties van een WDM-PON toegangsnetwerk. Het introduceert een geïntegreerde zenderreeks met een laag verbruik te gebruiken in een kostenefficiënte architectuur van WDM-PONs en inter-datacentercommunicatie.

Hoofdstuk 2 vergelijkt verschillende optische zenders en geeft een kort overzicht van hun belangrijkste karakteristieken. Externe modulatie met zowel Mach-Zehnder modulatoren (MZMs) als met EAMs wordt er beschreven. Er wordt aangetoond dat EAMs de beste keuze zijn voor geïntegreerde zender reeksen met laag vermogenverbruik, dankzij hun lage spanningszwaai en kleine afmetingen, in vergelijking met MZMs.

Om een laag verbruik te bereiken, wordt de elektronische driver topologie bestudeerd in hoofdstuk 3. De uitdaging in het ontwerpen van modulator drivers is de noodzaak om zeer grote stromen te leveren in combinatie met een hoge spanningszwaai. Vier verschillende uitgangsconfiguraties worden er vergeleken en technieken om het vermogenverbruik van de modulator drivers te verlagen worden beschreven.

Hoofdstuk 5 beschrijft duobinair (DB), een modulatieschema dat steeds meer gebruikt wordt in de hedendaagse optische communicatie. Aangezien de nodige bandbreedte ongeveer de helft is van NRZ, kunnen de bandbreedtespecificaties van de zender gemilderd worden. Dankzij zijn smalle optische spectrum is DB bovendien minder gevoelig aan chromatische dispersie in lange-afstandsverbindingen en kan het de spectrale efficiëntie verhogen in WDM architecturen. Voor optische DB is er ook precodering nodig om te verzekeren dat het ontvangen signaal gelijk is aan het originele binaire signaal.

Het uitgevoerde onderzoek dat leidde tot deze thesis heeft 2 geïntegreerde modulator driver reeksen voortgebracht:

- Een 10 kanaals 113 Gb/s geïntegreerde modulator driver reeks met ultra-laag vermogenverbruik.
- Een 2 kanaals 56 Gb/s duobinair geïntegreerde modulator driver reeks met een differentiële uitgang.

Beide ontwerpen worden uitgebreid geanalyseerd in hoofdstuk 4 en 6 respectievelijk. Voor zover bekend is de 10 kanaals geïntegreerde modulator driver reeks de eerste in zijn soort, terwijl hij het laagste vermogenverbruik

voor een EAM driver haalt, 50% lager dan voorheen gerapporteerd. De 2 kanaals geïntegreerde modulator driver reeks is de snelste modulator driver met op-chip DB encodering en precodering tot nu gerapporteerd.

Het laatste hoofdstuk geeft een overzicht van de belangrijkste conclusies van het gepresenteerde onderzoek en geeft een aantal suggesties voor toekomstig onderzoek.

English summary

The internet is becoming the ubiquitous tool that is changing the lives of so many citizens across the world. Commerce, government, industry, healthcare and social interactions are all increasingly using internet applications to improve and facilitate communications. This is especially true for video-enabled applications, which currently demand much higher data rates and quality from data networks. High definition TV streaming services are emerging and these again will significantly push the demand for widely deployed, high-bandwidth services.

The current access passive optical networks (PONs) use a single wavelength for downstream transmission and a separate one for upstream transmission. Incorporating wavelength-division multiplexing (WDM) in a PON allows for much higher bandwidths in both directions. While WDM technologies have been successfully deployed for many years in metro and core networks, in access networks they are not commonly used yet. This is mainly due to the high costs associated with deploying entire WDM access networks. However, the present optical networks cannot be simply and cost-effectively scaled to provide the capacity for tomorrow's users. As an effect there is a strong need for new WDM access components which are compact, cost-competitive and mass-manufacturable.

Increasing the number of wavelengths for WDM-PON automatically leads to an increase in the number of single pluggable transceivers, which brings substantial design challenges and additional costs. The multitude of TXs and RXs for different wavelength channels increases the total footprint considerably. Photonic integration of transceivers into arrays will significantly reduce the footprint and cost. However, the total power consumption of an array device is an issue. To avoid the use of a thermoelectric cooler, the integration density of components is severely limited by the heat dissipating capabilities offered by their package. As a result the WDM-PON philosophy necessitates the reduction of the transceiver's power dissipation.

From this plea it is apparent that the main technology challenges for real-

izing future-proof optical (access) networks are reducing active component power consumption, shrinking form factors and lowering assembly costs.

In this perspective an over 100 Gb/s throughput component, composed of 10 channels at 11.3 Gb/s per wavelength channel would be a great contribution to the expansion of customer bandwidth. It can provide increased line rates to the end users at speeds of 10 Gb/s per wavelength. As RXs typically consume much less power than externally modulated TXs, they can relatively easily be integrated into an array. Mainly high speed optical transmitters have significant power consumptions and the heat generation caused by power dissipation forms a critical obstacle in the development of a 10-channel transmitter, which again underlines the importance of power reduction.

Alongside the introduction of WDM in access networks, also inter-office point-to-point connections in data center environments could benefit from the WDM philosophy. As data center operators often suffer from fiber scarcity or do not own their fiber infrastructure, WDM technologies are essential to deliver reach and capacity extension for these scenarios. Inter-data center communication also benefits from cost-, footprint- and energy-efficient components operating at high speed to maximize the throughput. As an effect integrated over 100 Gb/s transceivers, such as 4 channels at 28 Gb/s, are highly desirable.

The research described in this dissertation was partly funded by the European FP7 ICT project C3PO (Colourless and Coolerless Components for low Power Optical Networks) and the UGent special research fund. The C3PO project aimed to develop a new generation of green Si-photonic compatible components with record low power consumption, that can enable bandwidth growth and constrain the total cost. C3PO envisioned building high-capacity access networks employing reflective photonic components. To achieve this, cost-competitive reflective transmitters based on electroabsorption modulators (EAM) needed to be closely integrated into arrays. A multi-wavelength optical source provides the required wavelength channels for both downstream and upstream signals in the WDM-PON.

Chapter 1 gives a short overview of a PON and describes the main implementations of a WDM-PON access network. It introduces integrated low power transmitter arrays for a cost-effective architecture of WDM-PONs and inter-data center communication.

Chapter 2 compares different optical transmitters and gives a short overview

of their most important characteristics. External modulation through both Mach-Zehnder modulators (MZMs) and EAMs is described. It shows that EAMs are the best choice for low power transmitter array integration, thanks to their lower drive voltage and smaller form factor, compared to MZMs.

To achieve a reduced consumption, the electronic modulator driver topology is studied in chapter 3. The challenge in designing modulator drivers is the need to deliver very large currents in combination with high voltage swings. Four distinct output configurations are compared and techniques to reduce the power consumption of the drivers are described.

Chapter 5 presents duobinary (DB), a modulation scheme that is gaining interest in today's optical transmission. As the required bandwidth is about half that of NRZ, it softens the constraints on the transmitter bandwidth. Thanks to its narrow optical spectrum, it has an improved tolerance to dispersion in long haul single mode links and it can improve the spectral efficiency in WDM architectures. For optical DB a precoder is necessary to assure the received signal is equal to the original binary signal.

The conducted research that resulted in this dissertation produced 2 low power EAM driver arrays:

- A 10-channel 113 Gb/s modulator driver array with state-of-the art ultra-low power consumption.
- A 2-channel 56 Gb/s duobinary driver array with a differential output with low power consumption.

Both designs are elaborately analyzed in chapter 4 and 6 respectively. To the best of our knowledge the 10-channel EAM driver array is the first in its kind, while achieving the lowest power consumption for an EAM driver so far reported, 50% below the state of the art in power consumption. The 2-channel EAM driver array is the fastest modulator driver including on-chip duobinary encoding and precoding reported so far.

The final chapter provides an overview of the foremost conclusions from the presented research. It is concluded with suggestions for further research.

List of publications

Publications in international journals

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- T. De Keulenaer, **R. Vaernewyck**, J. Bauwelinck, and G. Torfs, *Improvements in or Relating to Signal Processing*, European patent application, EP14161804, filed on 26 March 2014.

1 Introduction

The internet becomes the ubiquitous tool that is changing the lives of so many citizens across the world. Commerce, government, industry, healthcare and social interactions are all increasingly using internet applications to improve and facilitate communications. This is especially true for video-enabled applications, which now demand much higher data rates and quality from data networks. High definition TV streaming services are emerging and these again will significantly push the demand for widely deployed, high-bandwidth services. High speed networks are also being installed across Europe, giving end customers access to data rates (over 100 Mb/s) that used to be the preserve of telecom carriers entirely on their own.

1.1 ICT infrastructure and power consumption

With the ever increasing bandwidth demands, the internet needs to grow continuously. In parallel with the rising demand for bandwidth, there is an urgent need to significantly reduce the energy consumption of existing networks. Besides the ecological issues, the interest also stems from economic needs, since both energy costs and electrical requirements for telecom operators and internet service providers (ISPs) show a continuously rising trend. The dramatic increase in network energy consumption essentially depends on new services being offered, as well as on data traffic volume increase, which follows Moore's law, by doubling every 18 months [1].

In 2012 the global communication networks were estimated to consume about 350 TWh or 1.7% of the worldwide electricity consumption [2]. This number excludes data centers and consumer's personal computation devices, such as desktops, laptops, etc.

Passive optical networks (PONs) are considered to be the most energy efficient network architecture for broadband fiber access [3]. A PON basically consists of an optical fiber star topology, where a large number of subscribers are connected to the optical line terminal (OLT) at a central office (CO). The standard PON operates in the "single-wavelength mode" where one wavelength is used for downstream (DS) transmission and a separate one is used for upstream (US) transmission. PONs will be explained in more detail in Section 1.2. Incorporating wavelength-division multiplexing (WDM) in a PON allows one to support much higher bandwidth, since multiple wavelengths are used, both in DS and US directions.

WDM technologies have been successfully deployed for many years in metro and core networks as they provide tremendous system capacity with long distance transmission. In access networks, however, WDM technology is not commonly used yet. This is due to the relatively low required per-user data rates at present and more importantly due to the high costs associated with deploying entire WDM access networks. However, the present optical networks cannot be simply and cost-effectively scaled to provide the capacity for tomorrow's users. As an effect there is a strong need for new WDM access components which are compact, cost-competitive and mass-manufacturable. This is particularly true at the OLT, where a high degree of integration is a must. While a WDM-PON OLT could in principle be built from pluggable transceivers, a cost-, footprint- and energy-optimized solution is not available today, mainly due to the lack of highly integrated multi-channel transceiver arrays [4].

The necessity to increase the number of wavelengths for WDM-PON automatically leads to an increase in the number of single pluggable transceivers, which brings substantial design challenges and additional costs. In traditional PONs an OLT only contains a single DS transmitter (TX) and a single US receiver (RX). However, in WDM-PON the OLT hosts multiple TXs and RXs for different wavelength channels, increasing the total footprint considerably. Photonic integration of OLT transceivers into arrays will significantly reduce the footprint and cost of WDM-PON OLTs. However, the total power consumption of an array device is an issue. A single multi-channel integrated photoelectronic component consumes much more power than a discrete component. To avoid the use of a thermoelectric cooler, the integration density of components is severely limited by the heat dissipat-

ing capabilities offered by their package. Every watt of power consumed by the optoelectronics would be multiplied by a factor of 6 if we consider the power needed to drive thermoelectric coolers to maintain 25°C operating temperature and the power used by air conditioning systems to remove the generated heat in a building. As a result the WDM-PON philosophy necessitates the reduction of the transceiver's power dissipation.

While the ultimate solution is to have coolerless components, an interim step would be to design the components to operate semi-cooled, at 40°C, for example. This recent trend of increasing the operating temperature of the electronics on equipment cards aims at reducing rack cooling costs. In this way the cooling requirements are eased and temperature control power dissipation is reduced. This will obviously increase the power load on today's thermoelectric cooled optoelectronic devices, as they will have to work even harder at higher ambient temperatures. From this plea it is apparent that the main technology challenges for realizing future-proof optical (access) networks are reducing active component power consumption, shrinking form factors and lowering assembly costs.

In this perspective a 100 Gb/s throughput component, composed of 10 channels at 11.3 Gb/s per wavelength channel would be a great contribution to the expansion of customer bandwidth. It can provide increased line rates to the end users at speeds of over 10 Gb/s per wavelength. As RXs typically consume much less power than externally modulated TXs, they can relatively easily be integrated into an array. High speed optical TXs, on the other hand, have significant power consumptions, ranging from 0.5 W up to a few Watts. The heat generation caused by power dissipation forms a critical obstacle in the development of a 10-channel transmitter, which again underlines the importance of power reduction.

Alongside the introduction of WDM in PON networks, also inter-office point-to-point connections in data center environments can benefit from the WDM philosophy. As data center operators often suffer from fiber scarcity or do not own their fiber infrastructure, dense wavelength division multiplexing (DWDM) technologies are essential to deliver capacity extension for datacom applications. In Europe distances between data centers do typically not exceed 80 km, with the majority of the links being shorter than 40 km. Inter-data center communication also benefits from cost-, footprint- and energy-efficient components operating at high data rates to maximize the throughput. As an effect integrated $>$100 Gb/s transceivers, such as 4 channels at 28 Gb/s, are highly desirable.

1.2 Passive Optical Network

The general structure of a modern telecommunication network can be subdivided in three main sections called *tiers*, as shown in Figure 1.1 [5]. On the highest level, the *backbone* or *core tier* is used for long-distance transport and to interconnect continents and countries across hundreds to thousands of kilometers in a mesh topology. The *metro* networks reside at a lower level and consist of ring topologies that link several COs over tens to hundreds of kilometers. The *access tier* provides end-user connectivity. Access networks typically span several kilometers to tens of kilometers and are deployed in large volumes. They can be configured in bus, star or ring topologies [6].

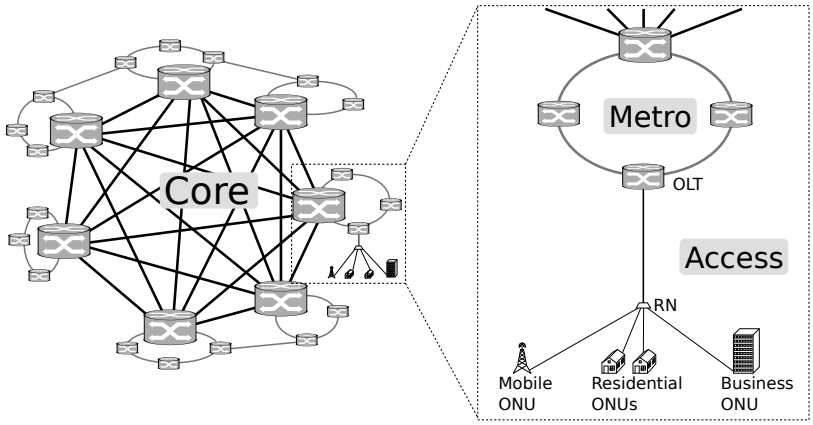

Figure 1.1: Geographical overview of the network tiers

While the core and metro networks incorporate optical fibers, most access networks still consist of copper. However, the bulk, low-speed copper cables can't cope with the increase in speed demanded by the next generation. Even though advanced transmission techniques are being used to augment the data speed towards end-customers, the present, already deployed access infrastructure can't possibly guarantee gigabit rates over distances surpassing 500 m. The copper cables pose a limitation, as they suffer from limited bandwidth, large attenuation and dispersion, added with crosstalk between different lines. Figure 1.2 shows the line rate of the different digital subscriber line (DSL) technologies over distance [7, 8]. Despite their short-distance data rate of over 200 Mb/s, they suffer from a low bandwidth distance product, which results in a mere 50 Mb/s rate after 1 km of transmission. The emerging G.fast standard does reach a top speed of 1.1 Gb/s

over a distance of 70 m, however, after 200 m the data rate quickly drops to 200 Mb/s [9]. A medium that is able to follow the data rate increase is the optical fiber, which can cope with extremely high bandwidths. Compared with copper, optical fibers have many advantages, which are summarized in Table 1.1 [10].

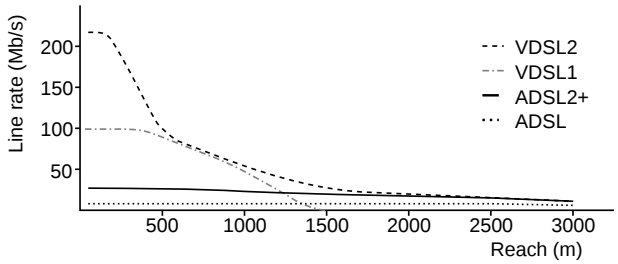

Figure 1.2: Performance characteristics of ADSL, ADSL2+, VDSL1 and VDSL2 [7, 8]

The legacy copper network can be replaced by an optical access network, which has a number of possible topologies. The CO can be connected to subscribers by point-to-point (P2P) fibers. This has the drawback of a high cost due to the huge amount of fibers needed. To reduce the fiber quantity, a star topology is used, in which case there is a splitting point, known as the remote node (RN) close to the end subscribers, which is connected to the CO. This splitting point can be implemented using an active node that incorporates a transceiver per customer which has to be powered and maintained, while future-proofness isn't guaranteed. When the splitter is implemented passively, the network is called a passive optical network. A PON consists of a single mode fiber-based point-to-multipoint (P2MP) topology, where a number of optical network units (ONUs) at subscriber side are connected to the OLT at the CO via passive splitters. The passive infrastructure benefits from a low installation and maintenance cost and reduces the power consumption, since no power supplies are needed at the RN.

To increase the bandwidth of the subscribers, a fiber to the home (FTTH) scenario is preferred. In this topology a high speed fiber is distributed to every subscriber's premise [11]. Even though this strategy is future proof, it hasn't been globally deployed yet due to the economic considerations that come with laying out such a vast network of optical cables. The equipment and fibers needed for the deployment, together with the civil works for installing the fibers are the main contributors to the immense cost. As a midterm solution a hybrid fiber access is provided by routing fiber to a cabinet in the street, so called fiber to the curb (FTTC), or to a building

Small size	The total diameter of the core and the cladding is typically 125 μm, although a protection jacket brings the total diameter typically to 400 μm. Coaxial cable has a diameter greater than 6 mm. For cramped conduits in buildings and underground layout, the advantage of small size is considerable.
Light weight	The mass density of silica is about a quarter of that of copper. Additionally, much less material is used, which makes the weight of a finished fiber 10 to 30% that of a copper cable.
Large bandwidth	The potential bandwidth, and hence data rate, of optical fibers is immense. Experiments have achieved over 100 Tb/s over one single standard SMF [12].
Low loss	With an attenuation of less than 0.2 dB/km, at a wavelength of 1550 nm, transmission links of tens of kilometers with passive splitters are possible.
Electromagnetically robust	Optical fibers are not affected by external electromagnetic fields.
Very low crosstalk	No energy is radiated by fibers and very little light escapes, implying good crosstalk characteristics.
Difficult to tab	High degree of security from eavesdropping.
Low dispersion	The dispersion is about 17 ps/(nm.km) at 1550 nm and around 1300 nm it can be 0.
Physical flexibility	Optical fibers can be bent. The surface tension on a fiber is proportional to the ratio of the fiber diameter and the bend radius.
Photonic, not electronic	Since the fibers will never generate sparks, they are safe to use in flammable or explosive environments.
Material availability	Copper is fundamentally rare and must be mined. Silica is abundantly available, as it consists of two most occurring elements: oxygen and silicon.
Easy multiplexing	A great number of wavelengths can be transmitted over a single optical fiber.

Table 1.1: Advantages of optical fiber

containing multiple end-users, e.g. an apartment building, called fiber to the building (FTTB).

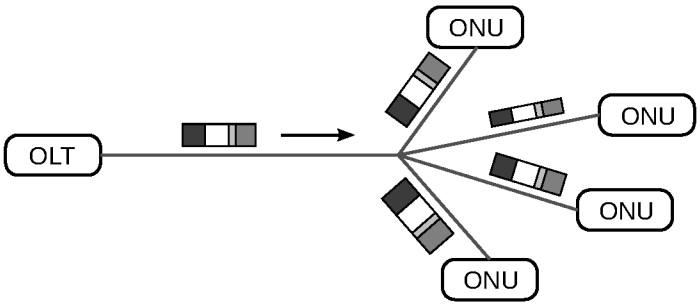

Figure 1.3: Schematical representation of TDM-PON downstream transmission

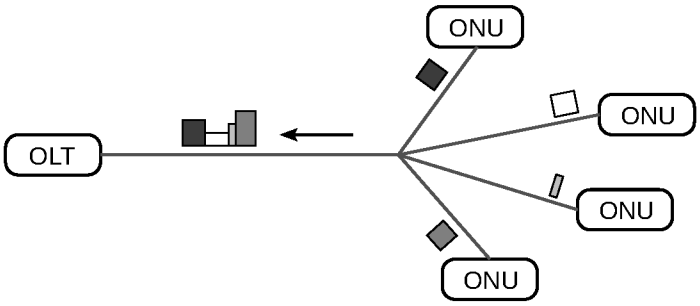

Figure 1.4: Schematical representation of TDM-PON upstream transmission

Since in a PON, the section between the OLT and the first splitter, known as the feeder section, is shared between all subscribers, a multiplexing technique is needed to ensure the co-existence of multiple signals from and to different subscribers. Time division multiplexing (TDM) is the most common variant. In this scheme a single OLT broadcasts all downstream traffic to every ONU in the link by using a power splitter at the RN (Figure 1.3). Each ONU extracts its own packets and discards all others. For the upstream communication (Figure 1.4), the OLT dynamically allocates specific time slots to active subscribers, during which the ONU can transmit data [13]. In this way packets are time interleaved at the splitter and the ONU is able to transmit at the full upstream bandwidth for the duration of the specified time slot. This method requires a precise synchronization packet transmission instant at the ONUs. By means of grants sent from the

OLT, the ONU knows when it is allowed to transmit data, which enables the synchronization. Furthermore, ranging protocols are implemented to ensure correct timing by sensing the distance between the OLT and the individual ONUs.

Since 1995 various TDM-PON standards have been specified by two standard bodies: the international telecommunications union (ITU) and the institute of electrical and electronics engineers (IEEE). The first PON standard came in 1998 with asynchronous transfer mode-based PON (ATM-PON) and was followed by broadband PON (B-PON) in 2005, which is an amendment of ATM-PON [14]. The 1Gb/s limit was exceeded by both gigabit-capable PON (G-PON) [15] and gigabit Ethernet PON (GE-PON) [16]. Next up were 10 Gb/s links with the 10G-EPON [17] and the XG-PON (X standing for the Roman number 10) [18] standards. The most recent standard is the next generation PON2 standard (NG-PON2) [19]. Table 1.2 summarizes the standards and their US and DS data rates.

PON	Standard	US rate (b/s)	DS rate (b/s)
ATM-PON	ITU-T G.983	155M	155M
B-PON	ITU-T G.983	155M/622M	622M
GE-PON	IEEE 802.3ah	1G	1G
G-PON	ITU-T G.984	1.25G	2.5G
10G-EPON	IEEE 802.3av	1G/10G	10G
XG-PON	ITU-T G.987	2.5G	10G
NG-PON2	ITU-T G.989.2	2.5G/10G	4x10G

Table 1.2: Different TDM-PON standards.

All versions use a particular wavelength band for the US transmission and a separate band for the DS transmission. Such a solution was envisaged primarily to keep the cost of the access network (especially optical transceivers) low and to allow for low cost ONUs.

Although the TDM-PON provides higher bandwidth than traditional copper-based access networks, it is not the ultimate solution. Intensive research is done to look beyond the 10 Gb/s TDM-PON. The new network concepts aim to increase either the bandwidth per ONU, the network reach, the splitting ratio or a combination of the above. The implementation of WDM achieves these goals. In the WDM-PON multiple wavelengths are supported in either or both upstream and downstream directions. The ONUs are assigned a downstream and upstream wavelength, as depicted in Figure 1.5 in which λ_{nu} denotes the US wavelength and λ_{nd} the DS

wavelength. A virtual P2P link is established between the ONU and the OLT. All wavelengths are aggregated onto a single fiber at the RN by a wavelength-multiplexer, typically an arrayed waveguide grating (AWG). Compared with a TDM-PON power splitter, the AWG gives reduced loss, increasing reach and splitting ratio. Each ONU can also operate at a data rate up to the full bit rate of a wavelength channel. Moreover, different wavelengths can be operated at different bit rates, hence, different varieties of services can be supported over the same network. At the OLT all upstream signals are demultiplexed and impinged on a separate RX. Even though every ONU requires its own dedicated DS-RX, time synchronization between the channels is no longer needed. The wavelength channels can even carry different signal formats as they constitute independent communication channels.

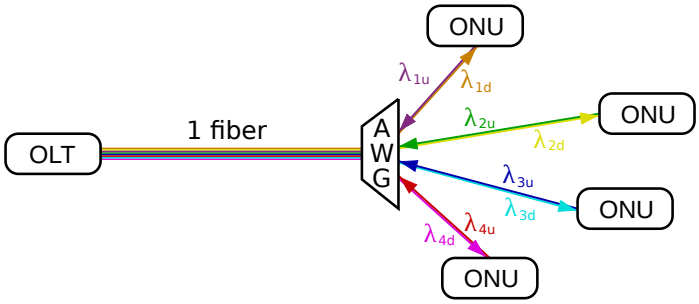

Figure 1.5: Schematical representation of WDM-PON

The first wavelength grid defined by ITU-T G.694.2 [20] is known as coarse wavelength division multiplexing (CWDM). This CWDM technology has a wavelength spacing of 20 nm and 18 channels were assigned between 1271 nm and 1611 nm. Since the transmission medium is the standard single mode fiber (SMF), typically the 8 wavelength channels around the 1550 nm wavelength window are utilized as they experience less attenuation, as shown in Figure 1.6. The CWDM-PON requires no strict wavelength tuning, thanks to its large wavelength spacing. As an effect no thermal control, such as a thermo-electric cooler (TEC), is needed, making CWDM-PON a relatively cheap network. Of course the limited number of wavelengths, and thus of channels, is a disadvantage. To accommodate a larger number of channels per fiber dense WDM (DWDM) is used. In ITU-T G.692 a channel spacing of 100 and 50 GHz, or about 0.8 nm and 0.4 nm respectively, were defined between 1528.77 nm and 1560.61 nm [21]. Narrower channel spacings below 25 GHz are called ultra dense WDM (UDWDM). With spacings as low as 6.25 GHz, over 1000 channels on a single SMF

have been achieved [22].

This staggering multitude of different wavelengths does demand a great number of TXs and RXs at the OLT, which exposes the main drawback of the (D)WDM network architecture. As a traditional single-wavelength PON only requires one TX and RX for the down- and upstream signal, the cost of the OLT is shared by a large number of ONUs. To achieve a cost-, footprint- and energy-efficient solution in DWDM-PON, close integration of the TXs and RXs is unavoidable.

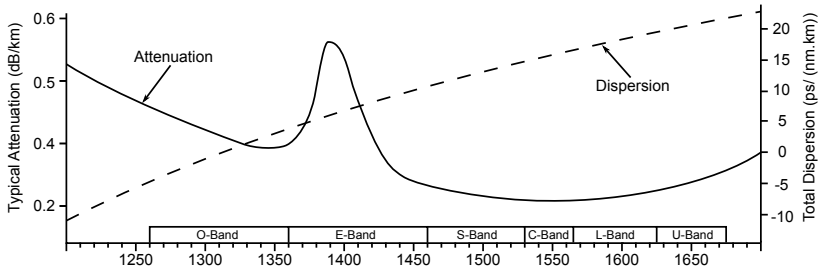

Figure 1.6: Attenuation and dispersion in SMF [5, 6]

For WDM upstream communication, every ONU needs a wavelength-specific TX. Utilizing wavelength specific lasers would give inventory problems and increase the burden of network operation and maintenance. In order to avoid these issues, so called *colourless* ONUs are used, which don't have a fixed wavelength source. This solution benefits from economy of scale and has lower costs. Typical approaches are described below.

The deployment of a wavelength *tunable laser* in the ONU is a straightforward solution [23]. A multitude of wavelengths can be produced by it, which makes it viable to be used in every ONU TX. The main downside of this scheme is the cost of the tunable lasers, which is momentarily too high to incorporate this light source in the ONUs [24]. Moreover, a deviation of the wavelength assigned to an ONU would not only degrade the signal channel of the ONU itself, but also the adjacent channels.

A broad-spectrum source can also be used at the ONU. *Spectral slicing (SS)* is then performed on the upstream spectrum by the AWG at the RN [25]. Even though the source is much cheaper and the SS implementation is simple, the modulation speed of the broad-spectrum source is typically low and it has a limited optical power.

Many researchers opt to eliminate the presence of a light source at the ONU. By placing a continuous wave (CW) light source at the OLT that is modu-

lated at the ONU, the wavelength generation and management are relaxed in a controlled environment. *Injection-locking* uses such an OLT based CW seed light source. Even though a Fabry-Perot (FP) laser is present at the ONU, its wavelength is defined by the injected seed light source coming from the OLT. The FP laser modulates the light, then sends the US signal to the OLT. In this scheme the CW injected light is typically provided by a multiwavelength light source at the OLT as a centralized light source. Instead of the injection locked laser, a reflective semiconductor optical amplifier (RSOA) can be used to modulate and amplify the signal at the ONU [27]. Both schemes, however, suffer from relatively low modulation speeds. Another issue affecting the cost and reliability of the RSOA is the temperature dependence [28]. Furthermore, the presence of the DS CW seed light on the fiber causes Rayleigh backscattering, that interferes with the US signal.

The integration of a(n) (reflective) electroabsorption modulator and semiconductor optical amplifier ((R)EAM-SOA) seems to be the solution for DWDM-PONs. The amplification of the SOA ensures high optical power, while the EAM modulates the CW seed light and provides a large bandwidth. In this way both the reach and customer bandwidth can be increased considerably. Moreover, the integration of the EAM together with the SOA enhances the prospect for low-cost manufacturing of the ONUs in high volumes [24]. Using the SOA in saturation gain even reduces the Rayleigh backscattering [29].

For the DS signal generation at the OLT a multi-wavelength light source can again be used in combination with colourless TXs, such as REAM-SOAs. This approach benefits from economy of scale and the light source can again be placed in a controlled environment without being affected by the heat generated by the transceiver electronics. Moreover, the scalability for higher speeds and capacity is simplified, as the channel generator remains unchanged while the reflective modulators are upgraded for higher speeds.

Because the deployment of a WDM-PON comes with a vast number of challenges, a hybrid WDM-TDMA PON is currently being investigated and deployed as a transition from TDM-PON towards WDM-PON. Here each WDM wavelength is further shared by a group of customers using TDM. NG-PON2 is an example of this hybrid solution.

1.3 Data centers

Data centers are an essential part of the infrastructure supporting the internet and the electronic communications sector. They support and sustain the rapidly growing web-based applications including video content hosting and distribution, social networking and large-scale computations (e.g., data mining, bioinformatics, indexing). With the rise of cloud computing, service hosting in data centers has become a multi-billion dollar business that plays a crucial role in the future information technology industry [30].

Today's data centers may contain tens of thousands of computers with significant aggregate bandwidth requirements, which are the back-bone infrastructure and enforce the development of cloud computing. Migrating systems onto the cloud is an emerging and accelerating trend. The cloud provides an interface, which enables the execution of a wide variety of applications on the same hardware platform. Cloud performance hinges on the computation, storage and network capacity provisioned at the data centers [31]. Continued growth of cloud applications requires a reliable infrastructure as interruptions in digital services will have significant economic consequences.

Due to the increasing scale of provided cloud services requiring more and more computing resources, the cloud should be conceived as a multi-data center environment able to offer orchestrated computing and storage services. The provided services should be capable of migrating a service from one data center to another in order to exploit, for instance, geographical variations of energy costs. Moreover, to improve the performance as well as to offer high availability under failure, multiple geographically distributed data centers need to replicate data that is communicated between the different sites by inter-data center links.

This inter-data center replication and redundancy imposes high bandwidth requirements on the inter-data center links, which are traditionally leased or owned by the data center itself. Of course these distributed networks are expensive and even cost more than the internal network of a data center [32]. To justify the fiber investments data centers want to achieve as much capacity as possible. Consequently the, at present typical, 10 Gb/s per wavelength channel links are no longer profitable and 100 Gb/s links are expected to be widely used in the near future [33]. However, commercially available centum form-factor pluggable (CFP) transceivers for 100 Gb/s are quite large. The excess dimensions drive a strong demand for small and cost-effective 100G transceivers, which achieve higher port density. In most of the current CFP transceivers the optical transmitter section

consists of four discrete 25 Gb/s EAMs and drivers [34, 35]. These are designed for use over a distance greater than 100 km, as e.g. inter-data center communication. To enable the miniaturization of the transmitter section, a compact 4 by 25 Gb/s optical transmitter module requires the close integration of the drivers and the EAMs.

Even though transceivers with four 25 Gb/s channels deliver a spectral efficiency that is 2.5 times greater compared to 10 Gb/s DWDM systems, coherent detection can yield an even greater spectral efficiency, requiring only a 50 GHz channel for 100 Gb/s transmission. Coherent technologies combined with digital signal processing (DSP) have a number of advantages such as improved noise tolerance, distortion compensation and polarization demultiplexing, which leads to supported reaches up to 1000 km [36]. On the other hand, the coherent transceivers are expensive, large and power hungry.

The optical duobinary (ODB) modulation scheme is a good candidate for data center applications. Thanks to its reduced bandwidth requirements, the TXs can work with cheaper 10 Gb/s optics at 25 Gb/s and the RXs employ simple direct detection. ODB is also more resilient to dispersion than a standard on-off keying scheme and offers closer channel spacing such that 25 Gb/s can be transmitted with a 25 GHz channel spacing.

However, one of the remaining issues in reaching the indispensable size reduction of 100 Gb/s transceivers is the power consumption. Downsizing the module increases the heat generation density [34]. A smaller package thus requires a reduced power consumption, while the module performance still needs to be ensured. A power reduction is naturally also beneficial for the operational costs of data centers, as the electrical utility costs are estimated at about 15% of the total costs [37]. Additionally, the reduction in power has an ecological purpose as well. In 2010 electricity used in global data centers likely accounted for between 1.1% and 1.5% of global electricity use [38]. Even though the rate of growth in electricity consumption slowed down from doubling between 2000 and 2005, to an increase of about 50% in the following 5 years, the continuously increasing trend doesn't seem to stop. The rack density increase in less developed markets will endow the rising tendency.

1.4 Overview of the work

This dissertation is based on the research the author has conducted over the last 4 years at the INTEC Design laboratory of the department of informa-

tion technology (INTEC) at Ghent University.

The INTEC Design laboratory offers young engineers a PhD training in advanced electronics, including the specification, design and testing of advanced electronic hardware, firmware and embedded software. Through collaboration with industrial partners, real-world problems are tackled. This gives the graduate the opportunity to process through the entire design cycle, from extensive study to realisation of the first prototype and thorough testing. The main applications concern RF and broadband communication, including fiber optics.

This work in particular was based on the author's research performed in the framework of the FP7 ICT project C3PO (Colourless and Coolerless Components for low Power Optical Networks). The C3PO project was funded by the European Commission through the Seventh Framework Programme FP7. The C3PO project aimed to develop a new generation of green Si-photonic compatible components with record low power consumption, that can enable bandwidth growth and constrain costs. A radically different and power-efficient 100 Gb/s throughput solution was proposed that was based on colourless, coolerless and reflective photonic integrated transceiver modules and optical switches. The project demonstrated the concepts of building next generation access, metro and storage area networks at 100 Gb/s and 10-channel WDM-PON networks using reflective photonic prototypes, verifying that its system and network concepts can be successfully implemented. C3PO hardware can be deployed for building next generation high-speed metro nodes collocated with optical access terminals, significantly reducing complexity and cost in architectures where fiber reaches the end-user.

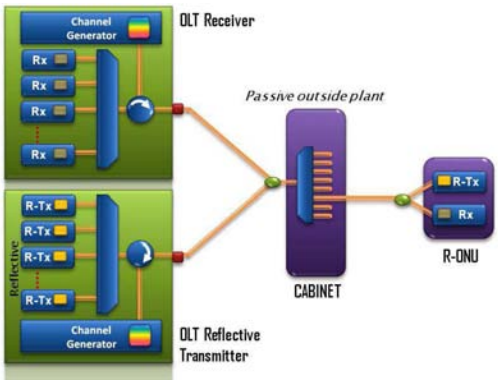

Figure 1.7: WDM-PON envisioned by C3PO project

C3PO envisioned building high-capacity access networks that circumvent the requirement for tunable lasers by employing reflective photonic components. As shown in Figure 1.7, at the OLT, the transmitting part is based on reflective TX arrays with a multi-wavelength optical channel generation providing all the required wavelengths. Such multi-wavelength sources are also used to provide carrier signals for the upstream signal in the WDM-PON. These CW carriers are modulated with the downstream data and are remodulated with user traffic at the ONU, where they are reflected back and fed into an array of receivers at the OLT. In this way, a tunable light source is avoided at the customer end.

The author's contribution to this project was the development of the ultra-low power 10-channel 11.3 Gb/s per channel electronic driver arrays required to modulate the reflective optics (R-EAMs). The necessity to achieve ultra-low power was demanded by the desire to reduce the overall power consumption, enable close integration and omit the power hungry cooling.

1.5 Outline of the dissertation

This chapter describes PONs and proposed WDM as the solution for the necessary bandwidth growth of the access network. Compact $>$100 Gb/s integrated low power transmitter arrays are introduced for a cost-effective architecture of WDM-PONs and inter-data center communication. Chapter 2 describes different possibilities of transmitting and modulating light. Chapter 3 focuses on the electronics of optical transmitters with an explanation of the typical topology of a modulator driver. It discusses driver power dissipation, while concentrating on potential power consumption reduction techniques for different topologies. Based on these insights the integrated driver arrays were conceived. The design and results of a 10-channel 11.3 Gb/s per channel EAM driver array are detailed in Chapter 4. To the best of our knowledge this driver array is the first in its kind and achieves the lowest power consumption for an EAM driver so far reported. Furthermore, a description of the duobinary modulation scheme and its generation is given in Chapter 5. Chapter 6 reports the design and results of 2 generations of 2-channel 28 Gb/s per channel duobinary EAM driver arrays. To the best of our knowledge, the proposed ICs are the fastest modulator driver including on-chip duobinary coding, reported so far. Finally, this dissertation ends with the conclusions in Chapter 7.

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2 Optical transmitters

2.1 Introduction

One of the key components in optical communication is the optical transmitter (TX), consisting of a directly modulated light source or a light source with an external optical modulator. The light can be modulated by changing its intensity, frequency, phase or polarization. We will mainly consider the change of the light's instantaneous power, also denoted as intensity modulation (IM). IM consists of intervals of high or low optical power, coinciding with '1' or '0' bits. The modulation can be performed directly or indirectly. In the case of direct or *internal* modulation the bias point of a laser or light emitting diode (LED) is adjusted directly by an applied electrical signal, representing a data stream. With indirect or *external* modulation an additional device or *modulator* is needed. In this arrangement a light source transmits a continuous stable light signal, with the modulator attached to the optical output. The electrical data stream acts on the modulator, that modulates the light passing through.

2.2 Optical light sources

First of all, we will explain the basic concept of the generation of light in semiconductor light sources. Consider Figure 2.1, where the energy levels

E_1 and E_2 respectively correspond to the ground state and the excited state of atoms in a medium. Two fundamental processes induce the emission of light: spontaneous emission and stimulated emission. In the case of spontaneous emission excited atoms return to the ground state and along the way photons are emitted in random directions with no phase relationship among them [1]. The energy of these photons is $E_2 - E_1$ or hv with h the Planck constant and v the photon frequency. On the other hand stimulated emission is initiated by an existing photon, which causes an excited atom to return to the ground state, resulting in more emitted photons. The photons emitted by stimulated emission not only match the initiating photon in energy and frequency, but also in other characteristics, such as the direction of propagation. In this way it is said that stimulated emission results in coherent light, while spontaneous emission leads to incoherent light.

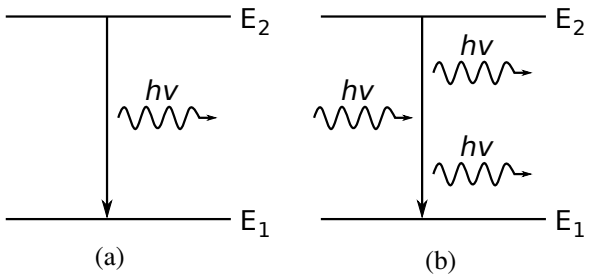

Figure 2.1: Fundamental emission processes: (a) spontaneous emission (b) stimulated emission

For long reach optical communication the ideal light source is compact, monochromatic, stable, and long lasting (many years). In practice, there are no perfectly monochromatic light sources; there are merely light sources that generate light within a very narrow band of wavelengths. Stability of a light source implies constant intensity level (over time and temperature variations) and constant wavelength (no drift).

A number of characteristics need to be introduced before going deeper into the advantages and disadvantages of direct and indirect modulation.

Extinction ratio (ER): In the ideal case there is no light emitted when a '0' bit is transmitted. In reality the transmitter doesn't totally shut off and there is always some remaining optical power present. For a typical two-level modulation format, this undesired effect is quantified by the extinction ratio:

$$ER = \frac{P_1}{P_0} \tag{2.1}$$

where P_1 and P_0 are the optical powers emitted for respectively a '1' bit and a '0' bit [2]. The ER is usually expressed in dB using the formula $10log(ER)$. In the ideal case the ER would be ∞, but for high speed direct modulation it has a maximum in the range of 9 to 14 dB, whereas indirect modulation can reach an ER of over 15 dB [3].

Spectral linewidth: The energy of a photon determines its wavelength as E = *hv*, with *v* the photon frequency, which is the ratio of the speed of light, *c*, and the wavelength, λ. In an ideal case, a single mode light source emits all photons with the same energy, and thus the same wavelength, it is said to be monochromatic. However, in reality, the light is not truly monochromatic. Due to e.g. spontaneous emission coupling in laser mode a variation in wavelength is caused. In this way the generated light consists of a narrow band around a single, central wavelength. The width of this band is called the linewidth of the single mode light source [4].

Chirp: The modulation process doesn't only change the light amplitude. In most light sources also the phase and frequency of the light is altered during IM. This undesirable frequency modulation leads to a sort of wavelength jitter and noise, which broadens the linewidth and is known as chirp. A good example is the directly modulated laser diode. The laser diode is driven by a current that changes the refractive index of the lasing medium when the output amplitude is changed. As a consequence the emitted wavelength is shifted.
Considering a perfect monochromatic light source and a perfect intensity modulator, for non-return-to-zero (NRZ) modulation the optical spectrum of the output looks as shown in Figure 2.2(a). The 3-dB bandwidth, Δf, of one sideband is about half the bit rate, B/2, leading to a full bandwidth equal to the bit rate. This gives the following wavelength linewidth:

$$\Delta\lambda = \frac{\lambda^2}{c}\Delta f \approx \frac{\lambda^2}{c}B \tag{2.2}$$

However when there is optical chirping the spectrum broadens as shown in Figure 2.2(b) and the linewidth becomes:

$$\Delta\lambda \approx \frac{\lambda^2}{c}\sqrt{\alpha^2+1}\cdot B \tag{2.3}$$

where α is known as the chirp parameter or linewidth enhancement factor, with a typical value of 4 for a directly modulated laser [5].

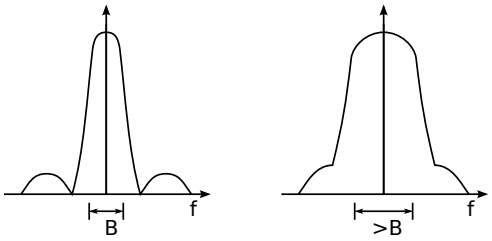

Figure 2.2: Optical transmitter spectrum of NRZ: (a) ideally vs. (b) chirped

Since chromatic dispersion exists in single-mode fibers, a wide linewidth is problematic. Dispersion is a consequence of different wavelengths travelling at different speeds through a fiber. It is specified by a change in group delay per nm wavelength and km fiber. The dispersion parameter D is typically measured in ps/nm/km. Chromatic dispersion causes the optical pulses to spread out quickly in a dispersive medium such as a single-mode fiber. In addition, a narrow linewidth is favorable for a reduced channel spacing in DWDM systems, in which 50 GHz spacing (0.4 nm) and below is becoming the trend [6].

Chirp can be subdivided into 2 different types: transient chirp and adiabatic chirp. Transient chirp only exists when the emitted power varies with time, during transitions of the applied electrical signal. As shown in Figure 2.3(a), the frequency deviations occur only at the slopes of a pulse. With respect to the flat part of the pulse, the rising edge propagates faster and the falling edge slower. Adiabatic chirp, on the other hand, is responsible for the different emission frequencies observed under steady state, Figure 2.3(b). With an increase in optical power comes a proportional increase in output frequency. With a positive fiber dispersion coefficient this causes a faster rising edge at the fiber output than at the input and analogously a slower falling edge. Figure 2.3(c) shows an illustration of pulse distortion due to the interaction of a combination of both chirp components with fiber dispersion [7].

Below is a short description of the most used and best known laser diodes [8].

Fabry-Perot (FP) laser In an FP laser the resonance is based on the Fabry-Perot principle. The cavity is formed by 2 reflecting facets. It is an multiple-longitudinal mode (MLM) laser with a quite large spectral linewidth of typically 3 nm.

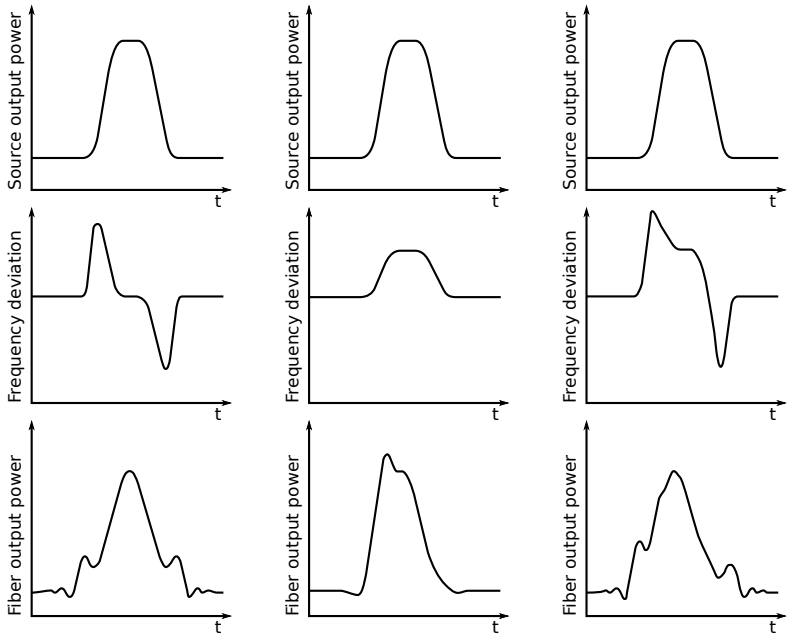

Figure 2.3: Illustration of chirp-dispersion induced pulse distortion: (a) transient, (b) adiabatic, (c) both chirp components

Distributed feedback (DFB) laser A DFB laser is similar to an FP laser but it has a built-in grating acting as a reflector. This grating provides distributed feedback and selects only one wavelength, making it a single-longitudinal mode (SLM) laser with a very narrow linewidth in unmodulated operation of less than 0.001 nm. This makes it ideal as continuous wave (CW) source for indirect modulation, but DFB lasers are also widely used for direct modulation.

Distributed Bragg reflector (DBR) laser The DBR laser looks like an FP laser, but with wavelength-selective Bragg mirrors instead of the facets. The wavelength selectivity makes this an SLM laser. The DBR laser properties are similar to those of an DFB.

Vertical cavity surface-emitting laser (VCSEL) The VCSEL doesn't emit light at the edge of the chip, but perpendicular to the wafer surface. It has a very short gain medium using Bragg mirrors. The short cavity length only exerts one wavelength, making the VCSEL

an SLM laser. The linewidth is larger than for DFB/DBR lasers at about 1 nm. However, VCSELs are easy to test and package at lower cost. In addition, VCSELs operate at lower current (max. 10-15 mA), so lower power consumption compared to FP/DFB/DBR lasers.

Semiconductor quantum well (QW) laser QW lasers have an active layer ten times smaller than bulk active region lasers. As a result small currents produce large amounts of coherent light within a narrow linewidth.

2.3 Direct modulation of a semiconductor light source

Direct or internal modulation alters the optical output power of a light source by adjusting its operating current. In this way it is a current driven process without the need for other components except for a driver that modulates the current. It is a compact solution, but in general gives worse performance than external modulation with respect to ER, chirp, linewidth and bandwidth. A number of different sources exist.

A LED is a monolithically integrated p-n semiconductor device or diode. When voltage is applied across its two terminals, it emits light through spontaneous emission. It is an incoherent multi-mode light source with a large angular spread and a wide spectral width of 30-60 nm. Both its bandwidth and output power are low at about 1 Gb/s and 10 μW respectively.

Despite these drawbacks, the LED remains a widely used light source for short distances. It is fairly simple to fabricate, cheap, very reliable and has proven to be very resilient to gradual degradation. The LED lacks the temperature-dependent threshold current typical for lasers and its light output against current is less affected by temperature [9]. This also makes it easier to drive as temperature compensation is unnecessary. Finally, as shown in Figure 2.4, a LED has a practically linear light output against current, which is beneficial for analog modulation.

Compared to LEDs, laser diodes emit light through the process of stimulated emission. Strictly speaking they amplify light, as is evident from the acronym LASER, which stands for light amplification by stimulated emission of radiation [10]. Photons traveling through the laser medium induce a cascaded and rapid process, in which excited atoms drop from their high-energy state to a low-energy state and release energy in the form of light. Simply put a single photon with the right properties causes many photons to follow. The stimulated photons are generated in an active material, placed inside a cavity. Inside of the cavity the photons are reflected back and

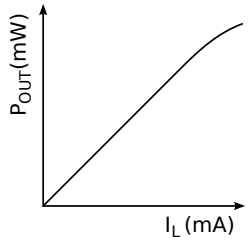

Figure 2.4: LED light output power vs. drive current

forth and a strong coherent monochromatic beam is formed. In this way the cavity operates as a reservoir with positive feedback through stimulated emission. This process is started by spontaneous emission, which causes incoherent light. However, when the energy pumped into the cavity is large enough, lost photons are replenished, a large positive gain is achieved and stimulated emission starts the lasing action. This is shown in Figure 2.5, where light amplification starts from a certain threshold. In this case a current driven laser diode is assumed, with a current threshold I_{th}. Above the threshold the output power grows approximately linear with the current. This is quantified by the slope efficiency of the laser, which is the change in output power divided by the change in current. Again for larger drive currents the output starts to saturate. Note that for direct modulation of the laser diode a bias current needs to be introduced to overcome the threshold current. Figure 2.5 also shows the lasers dependency on aging and temperature. As the laser becomes older or its temperature increases, the threshold rises and the slope efficiency lowers.

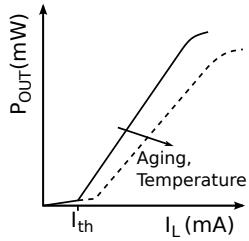

Figure 2.5: Laser diode light output power vs. drive current

The wavelength of the emitted light is defined by the grating period and the laser medium material. If there is sufficient difference in threshold gain between the longitudinal modes of the laser, it is called a SLM laser. When the

laser cavity oscillates at several frequencies simultaneously, it is an MLM laser [11].

The laser medium can be a gas, a liquid, an amorphous solid or a semiconductor [12]. The semiconductor laser is also called injection laser, junction laser or laser diode and is most frequently used for high speed communication. This is because of its many advantages, such as the compact size, wavelength tunability along with a narrow spectral linewidth, high stability and high efficiency. For example a HeNe gas laser consumes 10 to 20 W, while a semiconductor laser diode requires less than 0.5 W of power [13]. Thanks to the exploitation of the stimulated emission, the laser diode is capable of emitting a high optical power of around 100 mW. The spatially coherent nature of the emitted light induces a narrow angular spread of the output beam. This permits a high fiber coupling efficiency. Moreover, the laser diode is a very efficient component that is easily modulated by modulating the forward current through the diode, whereas other lasers need e.g. optical pumping to emit light. The relatively narrow spectral width of emitted light allows operation at high bit rates, since fiber dispersion becomes less critical for such an optical source. In addition, the semiconductor laser can achieve direct modulation at high frequencies (up to 25 GHz) as it has very short photon lifetimes associated with the stimulated emission. Because of the superior performance over LEDs, laser diodes are the most important light sources for fiber optical communication systems.

2.4 External modulation

As explained in the introduction, external modulation requires an additional modulator to modulate the CW light from a laser or LED. There are two distinct types of modulators: the electro-optic modulator (EOM) and the electroabsorption modulator (EAM). In EOMs the refractive index of a waveguide material is altered by inducing an electric field across it. For EAMs an electric field is also employed, but in this case the material absorption is modified. For both devices the electric field is produced by the introduction of a voltage.

2.4.1 Electro-optic modulator

The working principle of EOMs is known as the Pockels effect [14]. This is a linear electro-optic effect in which the refractive index of the used materials is modified through an external electric field. Moreover, the refractive

index changes proportionally to the applied voltage and this happens instantaneously, i.e. within the range of a few femtoseconds (10^{-15} s). Phase modulators are a straightforward application of this effect: they employ a voltage to modulate the refractive index of waveguides and hence induce a phase shift to a propagating light wave. To achieve intensity modulation the phase modulation must be transformed by using an interferometric structure. The most popular EOM is based on such a structure: the Mach-Zehnder modulator (MZM), founded on the homonymous Mach-Zehnder interferometer (MZI). EOMs can be fabricated out of several electro-optic materials. Lithium-niobate ($LiNbO_3$) is the most general building material, but also other piezoelectrics, semiconductors or polymers can be employed [11].

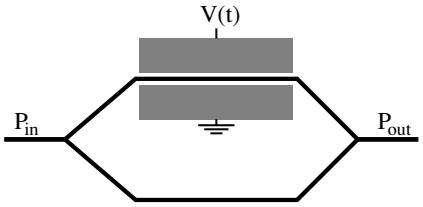

Figure 2.6: MZM with electro-optic material in one arm

The MZM consists of 2 arms, in which constructive or destructive interference can be obtained by a phase shift in between both arms. If the phase shift is 0°, the interference is constructive and the optical output is high. When the phase shift is 180°, the interference is destructive and the optical output is low. In its simplest form only one arm is equipped with electro-optical material, as shown in Figure 2.6. Assuming the optical input power P_{in} is split equally at the input, the light is equally combined by the output couplers and there is no internal loss, the output is:

$$P_{out} = P_{in} cos^2 \frac{\phi(t) - \phi_0}{2} \tag{2.4}$$

with $\phi(t)$ and ϕ_0 respectively the phase shifts experienced by the light in the upper and lower arm of the device in Figure 2.6 [15]. The phase shift in the upper arm depends on the refractive index, which itself depends on the applied external electric field exerted by a voltage V(t). By applying a time dependent voltage, the output is time dependent and a continuous optical input is modulated according to V(t). The phase shift value depends on many different parameters, such as geometry and material. The half-wave voltage, V_π, makes abstraction of these parameters and is defined as the

voltage needed to induce a phase shift of π. The electro-optically induced phase shift $\phi(t)$ can therefore be related to the applied voltage:

$$\phi(t) = \pi \frac{V(t)}{V_\pi} \tag{2.5}$$

Figure 2.7 shows the optical output power as a function of the applied drive voltage together with the periodic transfer function. For binary intensity modulation, such as NRZ, the peak-to-peak drive voltage is ideally chosen equal to V_π for optimal ER and output power. To achieve this optimal operation, the MZM needs to be biased correctly by a DC-voltage equal to V_{bias}. From Equation 2.5 it is, however, evident that the induced phase shift is time dependent. Consequently, the single arm drive Mach-Zehnder experiences phase modulation, which is equivalent to frequency chirping.

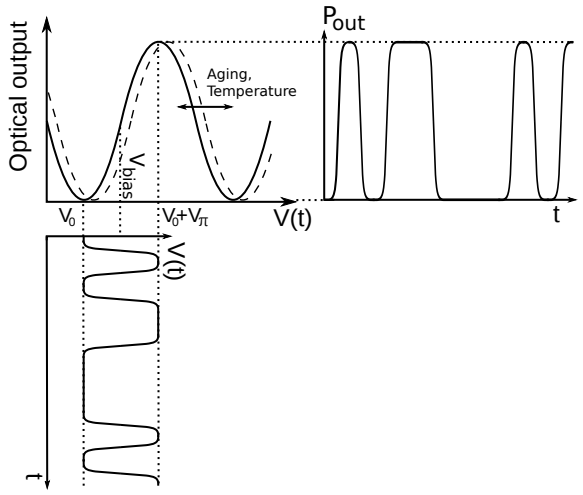

Figure 2.7: MZM transfer function and output as a function of drive voltage

This issue can be overcome by a dual drive MZM, where both arms have electro-optic material and are driven by 2 separate voltages, V_1(t) and V_2(t). In this case the phase becomes:

$$\phi(t) = \pi \frac{V_1(t) + V_2(t)}{V_\pi} \tag{2.6}$$

The phase is still time dependent, unless the sum of V_1(t) and V_2(t) is a constant, leading to:

$$\frac{dV_1(t)}{dt} = -\frac{dV_2(t)}{dt} \tag{2.7}$$

Since the DC components are of no importance, this comes down to 2 requirements for V_1(t) and V_2(t):

1. Equal peak-to-peak voltages.
2. Opposite data signals.

When these conditions hold, it is said that the dual drive MZM is operated in push-pull, which generally leads to chirp-free operation. Of course the output transfer function is also slightly altered as it is now dependent on the difference of V_1(t) and V_2(t), rather than on the single drive voltage V(t).

$$P_{out} = P_{in}cos^2(\frac{\pi V_1(t)}{2V_\pi} - \frac{\pi V_2(t)}{2V_\pi}) \tag{2.8}$$

Thanks to the dual drive operation the required peak-to-peak drive voltage is halved per arm. As V_π is typically large, in the order of 4 to 6 V, this reduces the requirements on the driver amplifier considerably [8]. However, two driver amplifiers are needed instead of one. Each of them needs an equal delay and output swing to achieve chirp-free transmission. All of this results in increased complexity necessary for push-pull operation.

This complexity can be omitted by driving a MZM in push-pull with only a single drive signal. This is possible by using a clever design, named an x-cut MZM. A cross section of such an x-cut is represented in Figure 2.8. The external electric fields applied across the waveguides have an opposite orientation, ensuring opposite phase shifts. Careful alignment and balancing are no longer required, at the cost of a higher drive voltage. Of course another solution might be a differential driver that outputs two complementary signals, these are, however, rare.

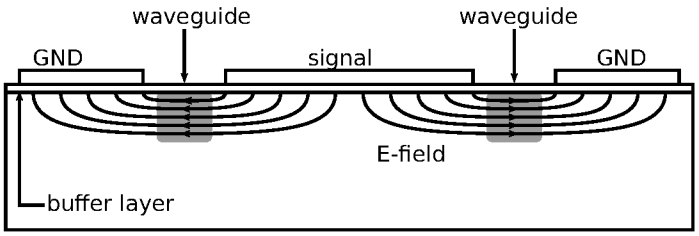

Figure 2.8: X-cut MZM

As the change in refractive index is nearly instantaneous when an external voltage is applied, one would assume that the bandwidth of a MZM is in

principle infinite. Obviously this isn't the fact as some bandwidth limitations do exist in the device. The reason is the small change of the refractive index. This necessitates a long interaction length between the optical wave and the electrical driving signal in order to acquire a sufficient phase shift for switching the modulator between the desired output states. Since the optical wave travels at the speed of light, travelling wave electrodes are needed for the drive signal to assure efficient interaction at high frequencies. However, the velocity of the optical and electrical signal are different, due to a different dielectric permittivity at optical and microwave frequencies. This causes the bandwidth limitations.

Thanks to the implementation of the travelling wave electrodes, the MZM looks like a transmission line from an electrical point of view. This results in the electrical signal to be free of bandwidth limitation in the modulator. In general the transmission line impedance is 50 Ω, allowing the use of standard connectors and cables.

Typically, MZMs can transmit 40 Gb/s, with a number of commercial devices available today requiring a half-wave voltage between 2.5 and 7 V_{pp} [16, 17]. It is even possible to find commercial MZMs able to transmit 80 Gb/s [18]. While the chirp-free operation of a MZM is a major advantage, sometimes chirp is desired for optimal transmission. In optical fiber systems operating in the non-zero dispersion window of fibers at 1.5 μm a modulator with negative chirp is needed for optimal performance [19, 20]. Another advantage of the MZM is its high ER in the range of 15 up to 20 dB [5]. In the case of lithium-niobate devices, also wavelength independent modulation characteristics and relatively low insertion losses of around 5 dB, make the MZM the most favorable option [21].

The main disadvantages are the large peak-to-peak drive voltages needed and large dimensions. Furthermore the operation of the MZM is temperature and age dependent, as is the case for laser diodes. The dependency is expressed by a horizontal drift of the transfer function shown in Figure 2.7. To counter this drift a bias controller is typically employed. For this reason a separate bias pin is added to the package [17].

2.4.2 Electroabsorption modulator

An EAM works on the principle of the Franz-Keldysh effect (FKE). This effect causes the effective bandgap of a semiconductor to decrease when an increasing electric field is applied. In the absence of an electric field the energy needed to promote an electron to the conduction band is too large for the photons of the transmitted laser light. As an effect no photons

are absorbed and the EAM remains transparent. By applying a voltage an electric field is induced, which starts to bend the energy levels, reducing the energy bandgap. When the applied voltage is sufficiently large, the photon energy is large enough to promote the atoms. This leads to absorption, rendering the EAM opaque.

The active region of the EAM can also be structured as a multi quantum well (MQW) which exploits the quantum confined stark effect (QCSE). The principle of this effect is similar to the FKE, but more intricate as the quantum wells exhibit a band structure with several subbands. Due to these subbands the absorption is polarization dependent. The absorption is stronger for QCSE than it is for FKE and it is optically narrowband. This gives QCSE-based modulators the possibility to modulate a single channel, making them more convenient to be integrated together with a laser source.

The principal materials for fabricating EAMs are III-V semiconductors, which are configured in a positive-intrinsic-negative (PIN) doped structure [22, 23]. This PIN-diode is similar to a PN-diode with a wider depletion region integrated by a lightly doped intrinsic layer. The extra intrinsic layer improves the frequency response and the high-frequency efficiency, without the need of an excessively large reverse voltage. As the layer has a higher optical refractive index than the surrounding p- and n-type layers, it supplies optical confinement, acting as a waveguide.

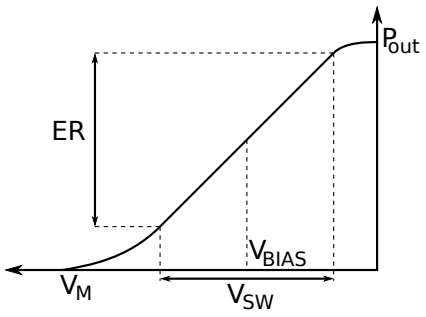

Figure 2.9: Typical EAM switching characteristics with ER, voltage swing and bias voltage indicated

Figure 2.9 shows a typical switching characteristic of an EAM. This represents the relationship between the optical output power and the applied voltage, V_M. While the required switching voltage, V_{SW}, is relatively low with a typical value of 2.5 V_{pp}, the ER is limited to a range of 11 to 13 dB [8, 24]. Figure 2.9 also indicates that a certain reverse bias voltage,

V_{BIAS}, can be set e.g. to optimize the ER or the chirp. While the region covered by the V_{SW} is linear in Figure 2.9, this isn't the case in reality. Even though the switching characteristic is linear in a small region, it doesn't produce a satisfactory ER, forcing non-linear operation. As a consequence the non-linearity causes pulse-width distortion (PWD) in the optical domain. PWD is the shortening or lengthening of output pulses relative to their ideal width of one unit interval (UI). A perfectly symmetric electric pulse with a certain rise- and fall-time is transformed into a non-ideal pulse that is wider or narrower, as shown in Figure 2.10.

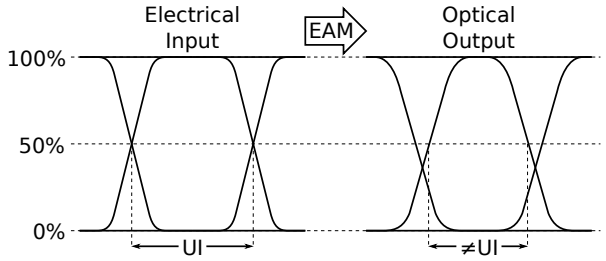

Figure 2.10: Example of PWD

From an electrical point of view the EAM is a reversed diode, which comes down to a mostly capacitive device when the CW laser is off. Turning on the laser generates a photocurrent, resulting in a non-linear photoresistance shunted with a capacitive load. The EAM photocurrent is large when the device is absorbing and thus opaque, but small when the reverse voltage is low and practically no absorption takes place. Generally an EAM is packaged in parallel with a 50 Ω load resistor to match the transmission line connecting the driver and the EAM. This load in parallel with the EAM capacitance (and the driver output impedance) causes a bandwidth limitation. This limitation introduces a trade-off. Reducing the EAM length lowers its capacitance and improves the bandwidth, but it also lowers the absorption and consequently increases the required switching voltage to achieve the desired ER. Reducing the intrinsic layer thickness improves the switching voltage, but at the same time it enlarges the capacitance, lowering the bandwidth.

The RC bandwidth limitation can be resolved by incorporating the RF electrode as a transmission line, creating a distributed electroabsorption modulator. The transmission line runs in parallel with the optical waveguide and causes the modulating microwave signal to co-propagate with the optical signal. The distributed EAM does have a number of drawbacks. It

has a high optical insertion loss, limiting the length to a few hundred μm. Also the RF propagation loss is very high due to the heavily doped layers. Finally, the velocity mismatch between the RF and the optical signal is quite large, which does cause limitations on the bandwidth. Because of the limited length, however, this limitation can be overlooked.

The chirp of an EAM is defined by the material it is made of. Where in MZMs the chirp is geometry dependent and can be eliminated, in EAMs it always exists. However, it is smaller than in the case of directly modulated lasers, as it only consists of transient chirp and no adiabatic chirp is present. By introducing a clever design it can be reduced or made negative.

The main advantage of EAMs over MZMs is their small switching voltage and small size. Moreover, they can be easily integrated together with a laser, as both devices are made on the same semiconductor substrate. This leads to a compact transmitter package known as an electroabsoption modulated laser (EML). Typically, the fiber-to-fiber insertion loss for stand alone EAMs is also high at about 10 dB. This is due to the optical coupling loss with fibers [25]. EMLs have a reduced insertion loss, as the high loss at the input fiber to the EAM chip interface is avoided. To achieve a high ER or zero chirp a MZM is preferred. Considering the bandwidth, both devices are more or less equal. The EAM isn't as wavelength independent as the MZM, but typically works across a wide window of 20 nm.

2.5 Conclusion

In light of high speed low power consumption transmitters for metro and long reach access networks the EAM seems the most fitting solution. The EAM provides indirect modulation with low chirp, high speed and high signal quality, necessary for the transmission over tens to hundreds of kilometers. Furthermore, the external modulation is quasi-wavelength independent, which is beneficial for WDM-PON implementation in combination with a multi-wavelength source. Compared to MZMs, the drive voltage required by the EAM is typically low. Moreover, the EAM's small form factor makes it easier to employ into an array.

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3

Modulator driver topologies and power consumption

3.1 Modulator driver circuit

In what follows we will go deeper into the design of a typical modulator driver amplifier. The main building blocks will be discussed and the most important properties will be examined. The focus will lie on bipolar transistor designs as the realized circuits use bipolars. Even though making the amplifier distributed is a good method in designing a modulator driver, we will not examine this option. The main reason is the bulky dimensions of this type of amplifier, which makes it impossible to use in an array of drivers.

Since the driver array design requires minimum power consumption per driver, a number of possible driver topologies is examined for power consumption reduction techniques.

3.1.1 Output stage

Typically the last driver stage is based on a current steering circuit, similar to an invertor in the current-mode logic (CML) family. The circuit is shown in Figure 3.1 and is also denoted as a differential pair. By varying the input voltage, the tail current I_{MOD} is switched through either the right

or left transistor. Due to the high speed in combination with the large currents needed, it is typically implemented with bipolar junction transistors (BJT), but it can also utilize field effect transistors (FET), cfr. Section 4.3. Equation 3.1 derives the required differential input voltage to achieve full switching of the modulation current I_{MOD} for a BJT circuit without degeneration. Since full switching requires I_{C1} to be equal to I_{MOD} and I_{C2} to be 0 (or vice versa), the fraction of currents in the last step of Equation 3.1 becomes 1. Considering that tanh(4) $\approx$ 1, a differential input swing of about 8 times the thermal voltage V_T is sufficient. At room temperature this adds up to 200 mV. For a FET circuit the required swing is dependent on the transistor dimension and the tail current.

$$
\begin{aligned}
V_{in1} - V_{be1} &= V_{in2} - V_{be2} && \Leftrightarrow \\
\Delta V_{in} &= V_T ln(\frac{I_{C1}}{I_S}) - V_T ln(\frac{I_{C2}}{I_S}) && \Leftrightarrow \\
\Delta V_{in} &= V_T ln(\frac{I_{C1}}{I_{C2}}) && \Leftrightarrow \\
\frac{I_{C1}}{I_{C2}} &= exp\frac{\Delta V_{in}}{V_T} && \Leftrightarrow \\
\frac{I_{C1} - I_{C2}}{I_{C1} + I_{C2}} &= \frac{exp(\frac{\Delta V_{in}}{V_T}) - 1}{exp(\frac{\Delta V_{in}}{V_T}) + 1} && \Leftrightarrow \\
\frac{I_{C1} - I_{C2}}{I_{MOD}} &= tanh(\frac{\Delta V_{in}}{2V_T}) && (3.1)
\end{aligned}
$$

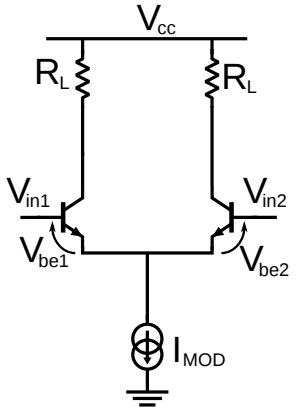


Figure 3.1: BJT current steering circuit or differential pair

The implementation of the differential pair has a number of advantages [1]:

- The modulation swing is easily controlled by changing the tail current.
- The voltage across the tail current is set by the common mode (CM) voltage of the input and it remains essentially constant no matter which arm is sourcing current. As an effect current variations are limited.
- The differential design is insensitive to input common mode noise, which leads to low jitter operation.
- The total current remains constant, minimizing the generation of power supply and ground bounce due to parasitics.

3.1.2 Back termination

In most cases the driver chip and the actual EAM chip lie relatively far apart. Both devices are then connected by a transmission line that has a certain characteristic impedance [2]. The most commonly used characteristic impedance is 50 Ω, so a 50 Ω resistor is packaged in parallel with commercial EAMs, as mentioned in Section 2.4.2. By matching the EAM load to the transmission lines characteristic impedance, reflections from the load end of the transmission line are minimized. However, since the EAM is capacitive, a mismatch occurs at higher frequencies and a reflected wave will propagate back to the driver. In case of an open collector at the driver, the output impedance is high, producing a second reflection towards the modulator. This deteriorates the signal quality by the addition of jitter and a reduction in ER. To assure good matching between both devices, the driver output impedance should also be chosen 50 Ω. The driver output resistance is determined by the load resistor of the differential pair, R_L in Figure 3.1. It is called the *back termination resistor* as it *terminates* the transmission line at the driver side. Every wave that is echoed back due to a load mismatch is absorbed by the back termination resistor, preventing double reflections. Of course this resistor increases the modulation current, and with it the power consumption. The current is even doubled compared with an open collector output, when the same swing is attained. An active back termination can reduce the power consumption and will be discussed in Section 3.2.5.

In case the driver chip and EAM chip are co-designed, they can be placed close together or copackaged, allowing direct bonding or 3D stacking. The

main advantage of keeping the devices in close proximity is the nullification of reflections. When the length of the interconnect is beneath a 20th of the wavelength of the data signal, it is no longer considered as a transmission line and matching considerations can be ignored [3]. In doing this, the power consumption can be reduced, as will be examined in more detail later on.

3.1.3 Bandwidth and parasitics

The presence of the back termination does have a positive effect on the RC-constant of the output. The shunting of the resistors lowers the impedance, which increases the possible bandwidth, thanks to a lower RC product. Of course the driver design, also has a major effect on the bandwidth. Due to the required high current levels, the differential pair transistors are large devices contributing a great amount of (parasitic) capacitance. In combination with IO-pads, ESD-protection diodes and wide traces, needed to support the large current flow, the total parasitic capacitance at the output of the driver can be as large as 200 fF. This will have a significant influence on the bandwidth of the driver.

On the other hand, parasitic inductance exists in long traces and bondwires. This inductance can be used as series peaking to increase the bandwidth [4]. Keeping these factors in mind, it becomes difficult to calculate the theoretical bandwidth of the driver without simulation tools.

3.1.4 Predriver

As already mentioned previously, the output stage uses large transistors to switch the large currents needed in achieving the desired swing. As a result, the output driver has a substantial input capacitance. A typical on-chip block, e.g. a retiming block, generally isn't designed to drive such a capacitive load. Moreover, if the output driver stage was directly driven from off chip, the input capacitance would induce poor matching, making the input prone to reflections. Furthermore, the current steering output stage ideally switches all or nearly all of the modulation current. A large input swing is required to assure this. Even though an input voltage swing of 200 mV is potentially sufficient for a bipolar differential pair. This doesn't include the possibility of degeneration, which would enlarge the requisite swing. A FET implementation could require a small swing when large devices are used, but this increases the input capacitance significantly.

To resolve these issues a block, known as the predriver, is used to drive the

output stage. The predriver must be able to drive a high capacitive load, while having a small input capacitance. Meanwhile the predriver's output swing needs to be sufficiently large to assure full, or near full, switching. In general, the design of the predriver is optimized together with the transistor size of the output stage to acquire optimal signal quality [5].

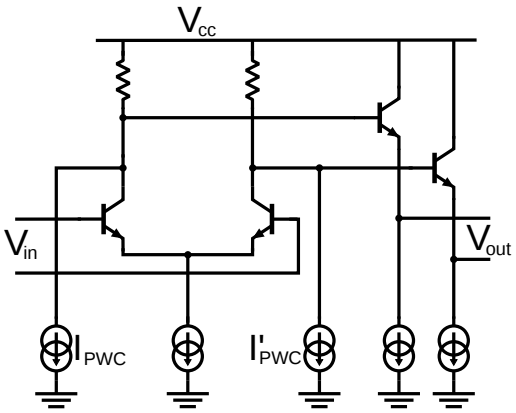


Figure 3.2: A simple predriver circuit

Most predrivers consist of a current steering stage followed by an (emitter) follower or a cascade of followers, as shown in Figure 3.2 (the current sources I_{PWC} are explained in Section 3.1.5). The current steering stage produces an output smaller than the driver output stage, while employing load resistors with larger values. Consequently the tail current is limited, leading to relatively small transistors and thus a small input capacitance. To reduce the input capacitance even further a follower can be added at the input. The output followers ensure a low output impedance, enabling the predriver to drive a large capacitive load at high speeds. In a practical implementation, multiple cascaded emitter followers may be used to provide more impedance transformation and level shifting [6, 7]. Furthermore, multiple gain stages can be implemented to establish sufficient output voltage swing [5, 8].

The modulation current of the output stage usually is programmable, making the desired predriver output swing variable. This can be resolved by changing the predriver tail current according to the change in the modulation current [7]. Also the common mode voltage at the output of the predriver is critical. If it is too low the driver output stage's tail current source will be pushed into saturation. If it is too high the differential pair's headroom might become too small. Typically, a number of bandwidth en-

hancing techniques can also be employed in the predriver [9], but these won't be discussed here.

3.1.5 Pulse width control

In Section 2.4.2 it was noted that the EAM usually isn't linear, which causes pulse width distortion in the optical output. The predriver can incorporate pulse width control (PWC), which minimizes the distortion and compensates for the PWD. Mostly a pulse width controller operates by introducing a variable offset voltage. In this way the electrical signal becomes predistorted, improving the optical signal quality after electrical to optical conversion, as shown in Figure 3.3. In addition, possible random offsets of the predriver can be dealt with by the PWC as well.

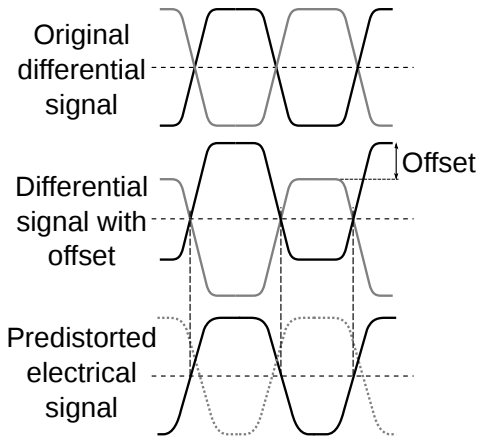


Figure 3.3: Operation of PWC

The control can be simply implemented with 2 adjustable current sources, as shown in Figure 3.2, labeled as I_{PWC}. Of course this implementation limits the amount of compensation as a too large PWC current will diminish the differential output, hindering the output stage from fully switching.

3.1.6 Collector emitter breakdown voltage

The large output swings that are required to drive EAMs can damage the transistors of the circuit. Especially at high bit rates the technologies are scaled down, which makes them more sensitive to breakdown. CMOS (complementary metal oxide semiconductor) FET technologies are particularly prone to breakdown. For speed of 10 Gb/s a transition frequency

f_T of about 50 GHz is required, which demands a technology with a gate length of 180 nm or less. These small devices, however, have a limit on the maximum drain-source voltage V_{ds} of about 2 V and are typically operated with a supply voltage of 2.5 V [10, 11]. These values make it difficult to achieve a voltage swing of 2.5 V, superimposed on a bias voltage of e.g. 2 V.

The issue can be resolved by migrating towards a SiGe BiCMOS technology, which incorporates both BJTs and MOSFETs. The BJTs typically have a higher f_T than the FETs within an equal technology node [12]. As an effect they can withstand higher voltages at higher speeds. When the collector-emitter voltage exceeds the breakdown voltage BV_{CEO}, there is an excess in collector current I_C, but the transistor is typically not damaged after the breakdown occurs. Moreover, BV_{CEO} is defined for an open base. If the base is connected to a common point, the breakdown voltage becomes much higher and is denoted as BV_{CES}. When the base perceives a certain resistance, the breakdown voltage BV_{CER} lies in between BV_{CEO} and BV_{CES}. For example, the 0.13 μm SiGe BiCMOS technology of [13] has a BV_{CEO} of 1.8 V at an f_T of 240 GHz. The maximum V_{ds} for CMOS would be below 1 V for an equivalent f_T.

It is possible that the required swing is still too large for a safe operation of the SiGe BiCMOS BJTs. In that case, one can still switch toward GaAs and InP technologies. These technologies can achieve a breakdown voltage of over 5 V, while the f_T is above 100 GHz [12, 14]. The main disadvantage of these technologies is the high cost associated with III-V semiconductors [15].

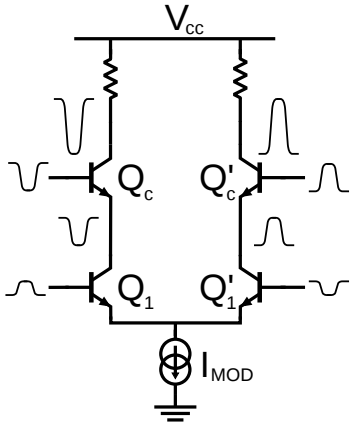


Figure 3.4: Breakdown doubler technique

To extend the use of SiGe BiCMOS to large output voltage swings a technique called breakdown voltage doubling can be applied. Here a current steering circuit with cascode transistors divides the output swing over 2 stacked transistors, reducing the collector-emitter voltage of each transistor. This is done by applying approximately half the swing to the base of the cascode transistor Q_c, as shown in Figure 3.4. The emitter of Q_c follows the base, leading to half the swing across Q_1 and Q_c. When the circuit is properly designed, the two transistors will evenly share the output swing, doubling the achievable voltage swing. The generation of half the swing at the cascode base can be done in 2 ways: 1) generated by the predriver [16]; 2) fed back from the output [17].

Both ways do require careful design considerations, especially the capacitance at the base of the cascode transistor is critical in order to minimize delay or overshoot. The technique can even be extended by stacking 3, 4 or even more transistors to further enlarge the feasible output swing [18]. It is important to remark, however, that for operating circuits at high supply voltages one should apply ESD circuits and voltage clamps with a sufficiently high voltage rating [19].

3.1.7 Simple driver architecture

Figure 3.5 shows the typical top level architecture of an EAM driver. The predriver and PWC, shown as a separate block, precede the driver stage. The EAM cathode and its shunt 50 Ω are connected to the driver stage supply.

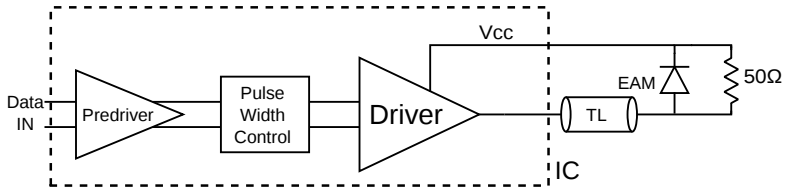


Figure 3.5: Simple EAM driver IC top level block diagram

3.2 Topology comparison to minimize the power consumption

Electric power *P* is denoted as a rate of doing work, measured in watts (W). The electric power produced by an electric current *I* consisting of a

charge of coulombs *Q* every second *t* passing through an electric potential difference or voltage *V* [20] is given by:

$$P = \frac{Q \cdot V}{t} = I \cdot V \tag{3.2}$$

A commercial EAM driver typically uses a supply voltage of +5.2 V to realize a swing of 2.5 V_{pp}. To circumvent reflections a back termination of 50 Ω is used, which requires a modulation current of 100 mA. In this respect, the output stage alone already consumes a minimum of 520 mW. This leads to a typical total power consumption of 1 to 2 W for commercial drivers [21–24].

To minimize the power consumption of the driver stage, different topologies need to be examined. The output can be made either DC- or AC-coupled with either a single ended or differential output. In this way 4 distinct output configurations can be compared. We will go deeper into all 4 approaches for a typical current steering output stage and also briefly examine the 4 output configurations with an active back termination. In the calculations of the power an output swing of 2.5 V_{pp} will be assumed, as this dissertation focusses on driving an EAM which typically demands such a swing. Due to the integration into an array, a bias-tee can't be used as it is too bulky. Consequently this topology is not examined.

3.2.1 Single ended DC-coupled output

The most straightforward topology of a modulator driver stage is a differential pair with a single ended DC-coupled output, as shown in Figure 3.6. Even though there are some MZMs that can be driven differentially, when operated in push-pull. Generally most optical modulators have a single ended input, which makes the single ended approach legitimate.

Although the interconnects in Figure 3.6 are drawn as bondwires, it can consist of a number of different connection methods. For instance, both the driver and the EAM can be packaged and connected through transmission lines and/or RF-cables or they can be directly bonded to a transmission line, etc. We will assume no transmission line is present, so we don't have to worry about reflections.

Equations 3.3 to 3.6 show how to calculate the minimum power consumption. Here V_{SW} is the output voltage swing, V_{BIAS} the reverse EAM DC bias voltage and V_{cc} is the supply voltage connected to the EAM cathode. Furthermore V_x is the voltage headroom required by the differential pair

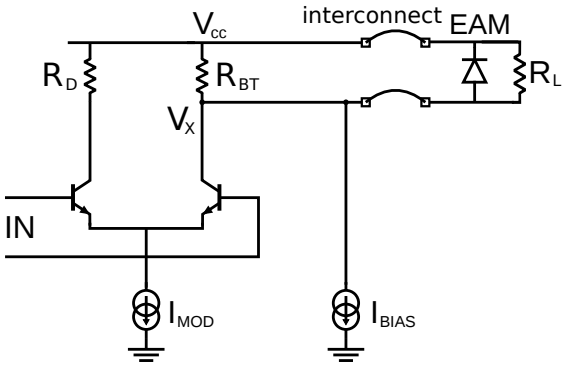


Figure 3.6: Typical configuration with a single ended DC-coupled output

and the modulation current source I_{MOD} and I_{BIAS} is the bias current required to set V_{BIAS}. It should be noted that these equations assume optimal conditions for the absolute minimal power consumption. This means e.g. that I_{MOD} is entirely switched, either through the left arm or the right arm, that no current is lost through the bases of the BJTs, etc.

$$I_{MOD} = V_{SW}\frac{R_{BT} + R_L}{R_{BT} \cdot R_L} = \frac{V_{SW}}{R_{BT}//R_L} \tag{3.3}$$

$$I_{BIAS} = (V_{BIAS} - \frac{V_{SW}}{2})\frac{R_{BT} + R_L}{R_{BT} \cdot R_L} = \frac{V_{BIAS} - \frac{V_{SW}}{2}}{R_{BT}//R_L} \tag{3.4}$$

$$V_{cc} = V_{BIAS} + \frac{V_{SW}}{2} + V_x \tag{3.5}$$

$$P_{DC} = V_{cc} \cdot (I_{BIAS} + I_{MOD}) \tag{3.6}$$

The use of the differential pair generates a differential output, while only a single-ended output is needed for driving the EAM. In this way half of the power isn't used. The pair switches the modulation current between the right arm, containing the EAM, and the left arm, connected to a dummy load R_D, which is equal to R_L and R_{BT} in parallel to preserve symmetry. Since only the right arm drives the EAM, the current in the left arm is a waste of power. The current through 'the dummy arm' can't be changed, because I_{MOD} is determined by the required voltage swing. However, the supply voltage doesn't need to be the same value for both arms, since the voltage swing of the dummy arm can be smaller than the output swing. A

separate supply V_{dd} can be used at the dummy arm, as shown in Figure 3.7 [25]. V_{dd} can be as low as 1.8 V for a headroom voltage V_x of 1.5 V. As a result of the extra power supply, the formula of the power dissipation changes, as shown in Equation 3.7.

$$P_{DC} = V_{cc} \cdot (I_{BIAS} + \frac{I_{MOD}}{2}) + V_{dd} \cdot \frac{I_{MOD}}{2} \tag{3.7}$$

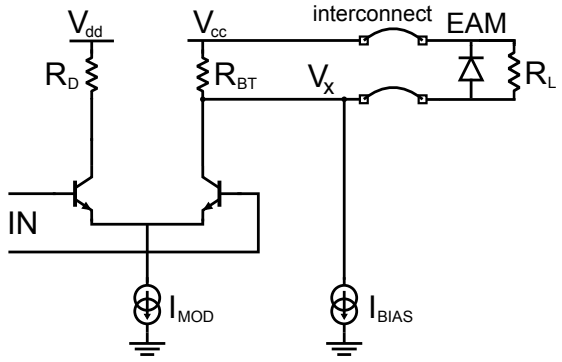


Figure 3.7: Typical configuration with a second supply for a single ended DC-coupled output

Equations 3.3 and 3.4 show that the resistor values of the parallel resistors R_L and R_{BT} have a large effect on the power consumption. If they are doubled, both I_{MOD} and I_{BIAS} are halved, which also implies the power consumption P_{DC} is halved. In this manner the close integration of both the modulator and its driver plays an important role in power consumption reduction. As most optical modulators have a 50 Ω input impedance, only R_{BT} can be increased to reduce the power, while neglecting matching thanks to the short interconnect. The change of the power consumption for an increasing R_{BT} is shown in Figure 3.8. This graph was calculated for an I_{BIAS} of 0 mA, a voltage swing of 2.5 V, a voltage headroom of 1.5 V and a V_{dd} of 1.8 V as will be presumed in all following figures. Clearly a slight increase of R_{BT} above 50 Ω has a significant impact on the power consumption. For instance, when R_{BT} is doubled to 100 Ω, a 25% power reduction is achieved. On the other hand it is evident that this reduction saturates at a certain point, e.g. increasing R_{BT} from 1 kΩ to 5 kΩ provides only a 4% power reduction. Since I_{BIAS} is also inversely proportional to R_L//R_{BT}, the same trend exists when I_{BIAS} is different from 0 mA and V_{BIAS} is set to a value other than half the voltage swing.

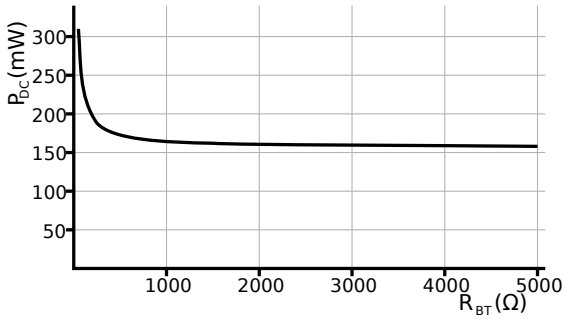


Figure 3.8: Power consumption in function of R_{BT} in a configuration with a single ended DC-coupled output (R_L = 50 Ω)

Another candidate to reduce the power consumption is the headroom voltage V_x. The voltage headroom of a current source and a differential pair is dependent on the technology, but a change of technology will only introduce small differences. It should, however, be noted that in some technologies the differential pair topology needs to alter into a cascode, which will increase V_x with at least 0.5 V. When going to high speeds the required V_x can even rise to 1 V or more, as the differential pair needs a larger headroom. Moreover, even a substantial decrease in V_x would only have a limited effect on the power consumption. For instance, halving V_x from 2 V to 1 V would only result in a power drop of less than 16%.

For now we presumed the modulators input impedance is 50 Ω. However, when the driver chip and the EAM chip are co-designed it is possible to modify R_L. The increase of R_L is anyhow limited due to the bandwidth requirements of the driver. Figure 3.9 shows the change of P_{DC} when R_L increases from 50 Ω to 100 Ω for an R_{BT} of 250 Ω. By doubling this load resistor the power consumption drops by almost 42%.

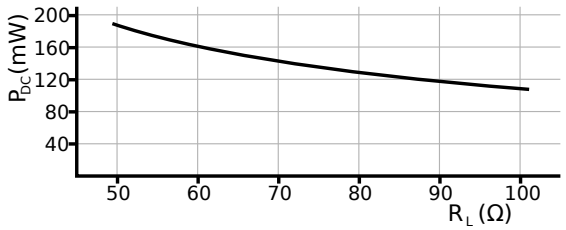


Figure 3.9: Power consumption in function of R_L for a configuration with a single ended DC-coupled output (R_{BT} = 250 Ω)

When the voltage swing needed to achieve a satisfactory ER is lowered, the greatest improvement in power consumption reduction can be made. This is clearly understood by looking at the formulas, as both I_{MOD} an V_{cc} are proportional to V_{SW}. Figure 3.10 shows the effect in case R_{BT} and R_L are 250 Ω and 50 Ω respectively. This shows that halving V_{SW} from 2.5 V to 1.25 V gives a decrease in power consumption of over 60%.

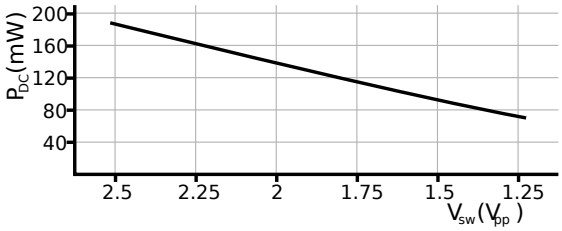


Figure 3.10: Power consumption in function of V_{SW} for a configuration with a single ended DC-coupled output (R_{BT} = 250 Ω, R_L = 50 Ω)

3.2.2 Single ended AC-coupled output

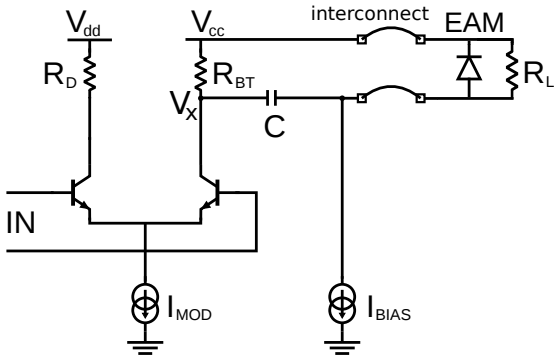


Figure 3.11: Typical configuration with a second supply and a single ended AC-coupled output

Figure 3.11 shows a driver stage with a single ended AC-coupled output. To minimize the power consumption a lower supply V_{dd} is again introduced at the dummy arm. Calculating the power consumption according to equations 3.8 to 3.11 gives a much larger result with respect to the DC-coupled output.

$$I_{MOD} = V_{SW}\frac{R_{BT} + R_L}{R_{BT} \cdot R_L} = \frac{V_{SW}}{R_{BT}//R_L} \tag{3.8}$$

$$I_{BIAS} = \frac{V_{BIAS}}{R_L} \tag{3.9}$$

$$V_{cc} = V_{SW} \cdot (1 + \frac{R_{BT}}{2R_L}) + V_x \tag{3.10}$$

$$P_{DC} = V_{cc} \cdot (I_{BIAS} + \frac{I_{MOD}}{2}) + V_{dd} \cdot \frac{I_{MOD}}{2} \tag{3.11}$$

While Equation 3.8 and 3.11 remain the same compared with the single ended DC-coupled case, the increase is mainly caused by a higher supply voltage V_{cc}. This can be explained as follows. The average current through the coupling capacitor C and thus through R_L, is zero. As a consequence, R_L is either sinking or sourcing a current I_L that has to realize half of V_{SW}. This current is equal to:

$$I_L = \frac{V_{SW}}{2R_L} \tag{3.12}$$

When the output is high, R_{BT} sources the current I_L that is sinked into the load. When the output is low, both R_{BT} and R_L source a current that is sinked by the I_{MOD} current source. Because the output needs to be low at both sides of the coupling capacitor, the voltage drop across R_{BT} needs to be V_{SW} greater than when the output is high. As an effect the supply voltage V_{cc} needs to be increased by $R_{BT} \cdot I_L$ compared with the DC-coupled case, to obtain the same voltage headroom.

In Figure 3.12 the power consumption and the supply voltage are plotted with respect to the back termination resistor for an R_L of 50 Ω and 0 mA bias current. It is clear that the supply voltage rises substantially with increasing R_{BT}. Moreover, in this case the power consumption has a minimum for a back termination resistor of 107 Ω. The optimum ratio between R_{BT} and R_L can be calculated from Equations 3.8 to 3.11 and is given in Equation 3.13. This shows that one can't simply increase R_{BT} to achieve a smaller power consumption as in the DC-coupled case.

$$\frac{R_{BT}}{R_L} = \sqrt{\frac{2(V_{SW} + V_x + V_{dd})}{2V_{BIAS} + V_{SW}}} \tag{3.13}$$

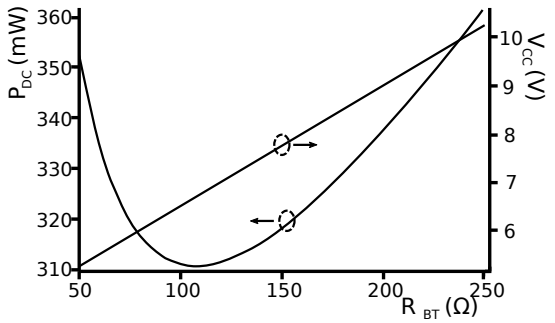


Figure 3.12: Power consumption and V_{cc} in function of R_{BT} for a configuration with a single ended AC-coupled output (R_L = 50 Ω)

For a typical EAM bias voltage the bias current will also be larger in the AC-coupled case. For the DC-coupled output the reverse EAM DC bias voltage is already partly obtained by the modulation current, which contributes half of V_{SW}. For the AC-coupled case, however, the output swing, and thus the modulation current, has no effect on the bias, as shown in Figure 3.13.

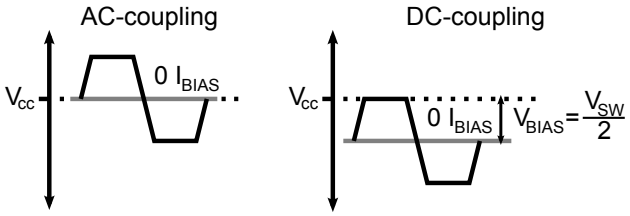


Figure 3.13: V_{BIAS} with I_{BIAS} = 0 mA for AC- and DC-coupled output

3.2.3 Differential DC-coupled output

By using a differential pair as the last driver stage, it makes sense to have a differential output. Consequently no power is "wasted" on a dummy arm and the output of one arm only has to be half the desired voltage swing. Figure 3.14 shows the driver stage with a differential DC-coupled output. For matching considerations R_{BT} is 25 Ω or half of the value of R_L.

Equations 3.14 to 3.17 show how the minimum power consumption of this configuration is calculated. Compared with the single ended configuration, the formulas are more complex, as the two arms of the differential pair are no longer completely independent.

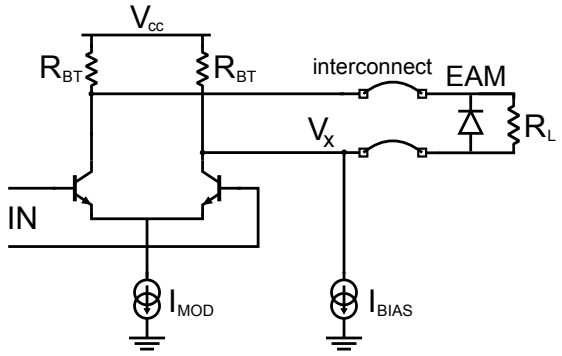


Figure 3.14: Typical configuration with a differential DC-coupled output

$$I_{MOD} = \frac{V_{SW}}{2} \frac{2R_{BT} + R_L}{R_{BT} \cdot R_L} \tag{3.14}$$

$$I_{BIAS} = V_{BIAS} \cdot \frac{2R_{BT} + R_L}{R_{BT} \cdot R_L} \tag{3.15}$$

$$V_{cc} = (I_{BIAS} + I_{MOD}) \cdot \frac{R_{BT} + R_L}{2R_{BT} + R_L} \cdot R_{BT} + V_x \tag{3.16}$$

$$P_{DC} = V_{cc} \cdot (I_{BIAS} + I_{MOD}) \tag{3.17}$$

Naturally increasing R_{BT} and R_L will have a beneficial influence on the current consumption. However, as in the single ended AC-coupled output case, they also affect V_{cc}. Figure 3.15 plots the power consumption and the supply voltage in function of the back termination resistor for an R_L of 100 Ω and 0 mA bias current. With growing R_{BT} the supply voltage increases linearly. Moreover, the power consumption again has a minimum for an optimum ratio of R_{BT} and R_L, as given in Equation 3.18.

$$\frac{R_{BT}}{R_L} = \sqrt{\frac{(\frac{V_{SW}}{2} + V_x + V_{BIAS})}{2V_{BIAS} + V_{SW}}} \tag{3.18}$$

Because the output swing can be halved per arm, a substantial power consumption reduction is expected. However, so far the reverse EAM DC bias voltage was assumed 0 V. When V_{BIAS} is set to a realistic value, a dramatic increase in power consumption is noticed, as shown in Figure 3.16.

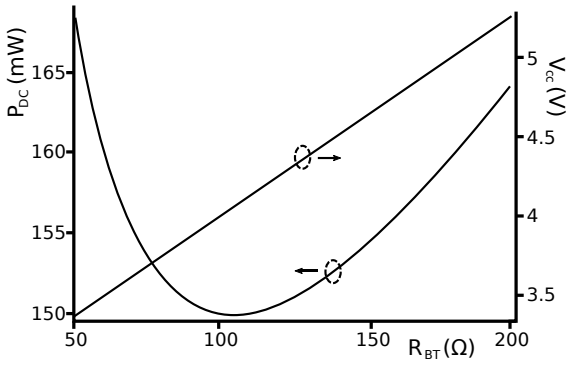


Figure 3.15: Power consumption and V_{cc} in function of R_{BT} for a configuration with a differential DC-coupled output (R_L = 100 Ω)

This is due to the connection between both arms, which causes R_{BT} of the right arm not to source all of the bias current. As an effect a part of I_{BIAS} is sourced by the left arm through the EAM, inducing an extra DC voltage drop V_L across the back termination resistors, given in Equation 3.19. To maintain sufficient head room, this drop needs to be compensated by increasing V_{cc}. Furthermore this makes I_{BIAS} 3 times higher compared with the single ended AC-coupled case for equal R_L and R_{BT}. It should be noted that the partition of I_{BIAS} also holds for the switched modulation current I_{MOD}, giving a power consumption worse than expected.

$$V_L = \frac{R_{BT}}{2R_{BT} + R_L} \cdot R_{BT} \cdot I_{BIAS} \tag{3.19}$$

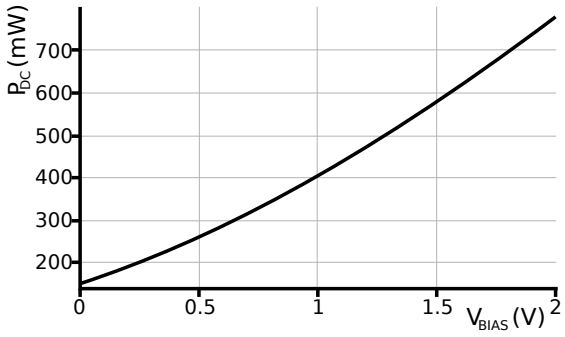


Figure 3.16: Power consumption in function of V_{BIAS} for a configuration with a differential DC-coupled output (R_L = 100 Ω, R_{BT} = 100 Ω)

3.2.4 Differential AC-coupled output

Figure 3.17 shows the driver stage topology with a differential AC-coupled output. Here two AC-coupling capacitors, C_1 and C_2, are added and an extra RF-choke is needed to set the reverse EAM DC bias voltage. Equations 3.20 to 3.23 give the formulas to calculate the minimum power consumption. In comparison with the differential DC-coupled topology, Equations 3.20 and 3.23 are the same, while Equations 3.21 and 3.22 are (slightly) altered. Thanks to the coupling capacitors, I_{BIAS} no longer has any effect on the supply voltage V_{cc} and it can be considerably smaller. In this way, AC-coupling the differential output has an advantageous effect on the power consumption, as shown in Figure 3.18.

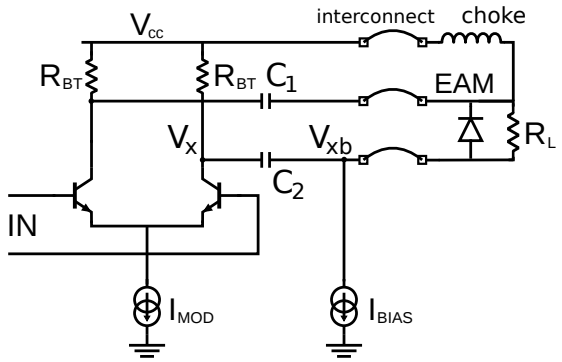


Figure 3.17: Typical configuration with a differential AC-coupled output

$$I_{MOD} = \frac{V_{SW}}{2} \frac{2R_{BT} + R_L}{R_{BT} \cdot R_L} \tag{3.20}$$

$$I_{BIAS} = \frac{V_{BIAS}}{R_L} \tag{3.21}$$

$$V_{cc} = I_{MOD} \cdot \frac{R_{BT} + R_L}{2R_{BT} + R_L} \cdot R_{BT} + V_x \tag{3.22}$$

$$P_{DC} = V_{cc} \cdot (I_{BIAS} + I_{MOD}) \tag{3.23}$$

Nevertheless it should be noted that Equation 3.22 doesn't take into account the voltage headroom of the bias current source, V_{xb}. Typically, V_x is larger than V_{xb}. However, would the required V_{BIAS} be large and V_{xb}, instead of V_x, becomes the limiting factor for calculating V_{cc}, Equation 3.22 becomes:

$$V_{cc} = \frac{V_{SW}}{2} + V_{BIAS} + V_{xb} \tag{3.24}$$

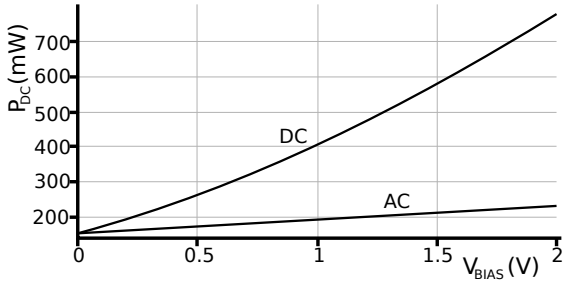


Figure 3.18: Comparison between AC- and DC-coupled differential configuration of the power consumption in function of V_{BIAS}

3.2.5 Active back termination

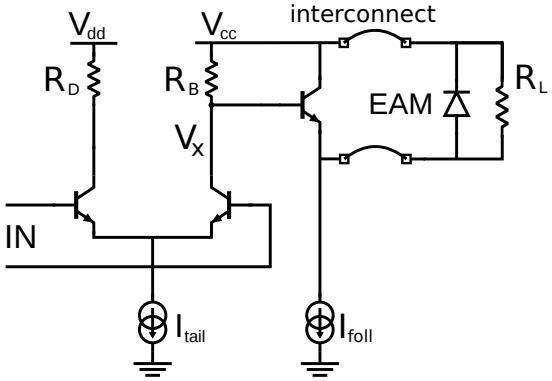


Figure 3.19: Simple driver circuit with active back termination

An alternative topology is a driver stage in which the output impedance isn't determined by a passive resistor, but rather by an active last stage. This is called an active back termination. The last stage consists of a unity gain amplifier that provides a matched output impedance and buffers the output of the previous stage, which produces the desired voltage swing [26]. Typically, an emitter follower is used for this last matching stage, as shown in Figure 3.19 [27]. Without going into further detail, we will examine if this topology can result in a lower power consumption compared with the conventional topologies. Considering the penultimate stage, typically a current steering circuit, a large supply voltage is needed to achieve the desired swing, meaning low power consumption might be a challenge.

Again 4 possibilities arise: single ended vs. differential and DC-coupled vs.

AC-coupled outputs, shown in Figure 3.20. The power consumption will be investigated and the active back termination with minimum dissipation will be selected in what follows.

With a DC-coupled output the reverse bias voltage already needs to be set in the differential pair stage. For the differential output of Figure 3.20(c), this is achieved through the current I_{BIAS1}. Due to the differential implementation, the reverse bias voltage is defined as $R_B \cdot I_{BIAS1}$. This will increase the necessary supply voltage, which makes this topology very power hungry, certainly in combination with the necessity of a second bias current, I_{BIAS2}.

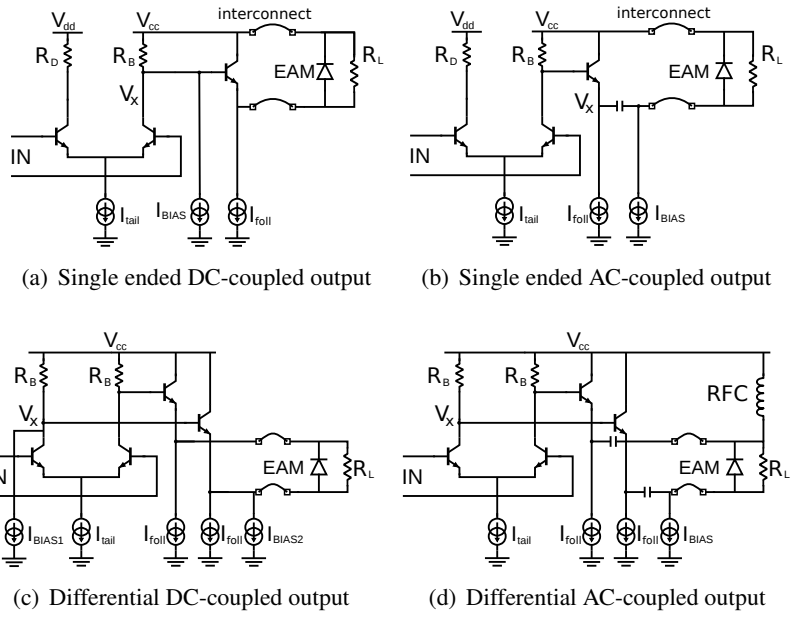
The single ended output of Figure 3.20(a) uses the current I_{BIAS} to set the reverse bias, defining it as $R_B \cdot I_{BIAS} + V_{SW}/2$ plus a threshold voltage. As the threshold is temperature dependent, this may cause a precision problem, that can be resolved by a control loop. However, the threshold voltage also determines the minimum reverse bias voltage, which becomes quite high with a typical threshold of 0.7 to 0.9 V. The use of a source follower can resolve the issue, but will reduce the power efficiency as a source follower generally has an amplification smaller than 1. Furthermore an extra bias current is again needed, incorporated into I_{foll} in Figure 3.20(a). All of this also disregards the single ended DC-coupled output as the least power consuming solution.

The power consumption of the AC-coupled output topologies lie very close together for the single ended and differential output. Equations 3.25 to 3.29 denote how to calculate the minimum power consumption for the single ended case of Figure 3.20(b). Equation 3.28 shows that the minimum required supply voltage V_{cc} is defined by a maximum of two values. It takes into account V_X, which is defined as the voltage headroom of either the current source I_{foll} or I_{BIAS}. One of these two will saturate when the supply is too small, depending on the desired swing, bias and the voltage threshold of the follower. The headroom of the differential pair is of less importance, since the headroom of I_{foll} plus a threshold is typically larger. As in Sections 3.2.1 and 3.2.2 a second supply voltage is again used to lower the power consumption.

$$I_{tail} = \frac{V_{SW}}{R_B} \tag{3.25}$$

$$I_{BIAS} = \frac{V_{BIAS}}{R_L} \tag{3.26}$$

$$I_{foll} = \frac{V_{SW}}{2R_L} \tag{3.27}$$



(a) Single ended DC-coupled output

(b) Single ended AC-coupled output

(c) Differential DC-coupled output

(d) Differential AC-coupled output

Figure 3.20: Different possibilities for the active back termination topology

$$V_{cc} = max(V_X + V_{th} + V_{SW}, V_X + V_{BIAS} + V_{SW}/2) \tag{3.28}$$

$$P_{DC} = V_{cc}(I_{BIAS} + I_{foll} + I_{tail}/2) + V_{dd}I_{tail}/2 \tag{3.29}$$

Equations 3.30 to 3.34 denote how to calculate the minimum power consumption for the differential output case, shown in Figure 3.20(d) where an RF-choke (RFC) is used. The minimum required supply voltage is again a maximum of 2 values. Compared with the single ended topology the supply is generally smaller for realistic voltage bias and swing. Also the differential pairs tail current, I_{tail}, is halved, as the desired single ended swing is halved. On the other hand the differential implementation does require two I_{foll} current sources, which increase the power consumption considerably.

$$I_{tail} = \frac{V_{SW}}{2R_B} \tag{3.30}$$

$$I_{BIAS} = \frac{V_{BIAS}}{R_L} \tag{3.31}$$

$$I_{foll} = \frac{V_{SW}}{2R_L} \tag{3.32}$$

$$V_{cc} = max(V_X + V_{th} + V_{SW}/2, V_X + V_{BIAS} + V_{SW}/2) \tag{3.33}$$

$$P_{DC} = V_{cc}(I_{BIAS} + 2I_{foll} + I_{tail}) \tag{3.34}$$

Figure 3.21 plots a comparison in power consumption between both AC-coupled configurations for a varying load resistor, R_L. This was calculated with a V_X of 0.6 V, V_{dd} of 1.8 V, a voltage swing of 2.5 V and a reverse bias of 1.5 V. The load resistor R_B was chosen to be 300 Ω and the threshold is 0.9 V. The single ended case consumes the least power. Even though the difference is modest, it would rise with growing reverse bias voltage and swing. It needs to be noted that if R_B is larger, the differential approach would be favoured. The increased resistance would, however, cause a decreased bandwidth that would be insufficient.

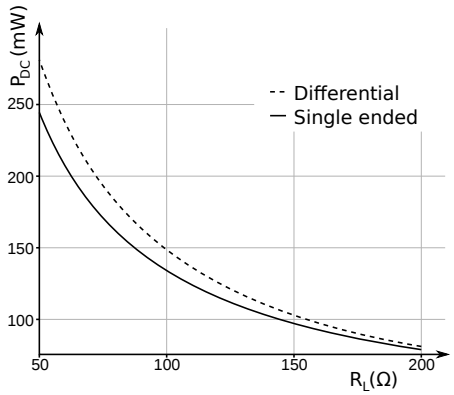


Figure 3.21: AC-coupled active back termination comparison between single ended and differential output

3.3 Comparison

From the discussion above it seems that there are 3 main contenders for the smallest power consumption:

1. The conventional single ended DC-coupled output topology.
2. The conventional differential AC-coupled output topology
3. The single ended AC-coupled ouput with active back termination topology.

The differential implementation does have a couple of drawbacks. First of all, it needs an EAM with two floating pins, which is not commercially

available and is difficult to fabricate. Secondly, the topology desires an RF-choke to set the bias voltage. This is a bulky component, that would be difficult to integrate into an array. Moreover, it has a larger power consumption compared with the single ended DC coupled topology, considering equal conditions and a load resistor R_L of 100 Ω for both configurations. This is represented in Figure 3.22, where the power consumption is calculated for different output swings with V_{BIAS} 1.5 V and V_X 1 V. The R_{BT} for the differential case and the single ended case are respectively 100 Ω and infinite (so no R_{BT} is present). This would give a comparable bandwidth.

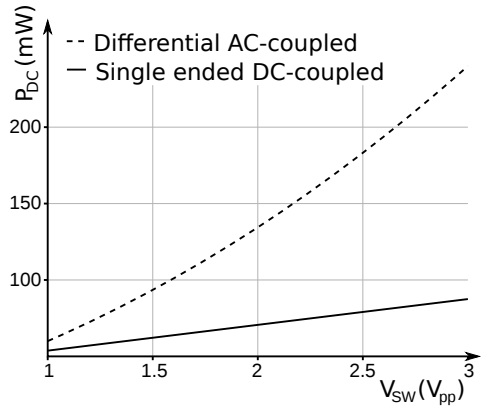


Figure 3.22: Comparison between single ended DC-coupled output and differential AC-coupled output for different V_{SW}

The approach with the active back termination does have a couple of advantages. Thanks to the emitter follower at the output, the output impedance is low in the range of a few tens of Ω. This gives a low impedance in parallel with the EAM capacitance, causing the bandwidth to be large even with a large R_L. Furthermore, the tail current of the differential pair can be chosen much lower than I_{MOD}, which is needed by the normal topology. Consequently the transistors can be smaller, reducing the input capacitance of the driver stage. This relaxes the constraints on the current of the predriver stage, reducing the total power consumption even further. However, for now we have assumed the I_{foll} current to be minimal, imposing the collector current of the emitter follower to be zero when the output is low. In reality this isn't feasible, forcing the current to be larger.

The normal single ended DC-coupled output topology, on the other hand, is the most simple approach, especially compared with the active back termination. As the power consumption can go below 100 mW, the active back

termination can only achieve a marginal gain in power reduction, while it holds a larger risk. So active back termination will not be pursued in this work.

3.4 Conclusion

In this chapter a number of output topologies were compared to reduce the power consumption. While in theory active back termination has some great potential of reducing the power consumption, in practice the power reduction will be minimal. As a result the conventional single ended DC-coupled output topology is favoured to minimize the power consumption. Next to its low dissipation, it is one of the simplest topologies, which holds the least risks.

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4

10 channel 11.3 Gb/s/ch low power EAM driver array

4.1 Introduction

As introduced in Chapter 1, dramatic increase of energy consumption owing to high bandwidth demands are becoming an issue and need to be addressed. Service providers are pursuing the deployment of WDM in next-generation PONs. At the OLT, which must support traffic from many ONUs, a major challenge is the lack of cost-effective, compact, low-power integrated WDM access components. A key enabling component for the OLT is a novel reflective multi-channel transmitter, which features a photonic integrated circuit (PIC) array of reflective EAMs (REAMs) integrated with an ultra-low power electronic driver array. This driver array, containing 10 channels, is one of the most challenging components to develop. As typically the power consumption of a single EAM driver is quite high, integrating 10 such EAM drivers into an array would require a costly, power hungry thermo-electric cooler (TEC). To the best of our knowledge such low power EAM driver arrays are not currently available on the open market, nor published in the literature by other authors.

4.2 Specifications

The aim was to minimize the power consumption of the modulator driver while keeping a sufficient voltage swing to drive the EAM. A small form factor was chosen, with a pitch of 500 μm between the channels. The target was an EAM driver array unit comprising 10 channels with each channel operating at 10 Gb/s. Introducing forward error correction (FEC) even calls for a data rate of at least 11.3 Gb/s. Moreover, the small form factor demands low power consumption for the driver channel array, certainly below 3 W in total or 300 mW per channel. The desired voltage swing was set to 2.5 V_{pp} with a 1.8 V reverse DC bias. A summary of the chip level design specifications can be found in Table 4.1

Parameter	**Unit**	**Min.**	**Typ.**	**Max.**
Operating temperature range	°C	0	25	70
Supply V_{cc2}/ current/ch	V/mA		4.5/43	
Supply V_{cc1}/ current/ch	V/mA		2.5/11	
Supply V_{cc3}/ current/ch	V/mA		1.8/30	
Output overshoot	%		10	
Crosspoint adjustment	%		12	
Driver jitter	ps_{pp}		12	
Single ended output swing	V_{pp}	1.5	2.5	3
Single ended input resistance	Ω		50	
RF return loss	dB	9	12	
Output edge speed (20%-80%)	ps		28	
Total power consumption/ch	mW		250	300
Die area (10 channels)	mm^2		1.2x5.5	

Table 4.1: 10-channel 113 Gb/s EAM driver array chip level design specifications

4.3 Technology

High speed modulator driver arrays are challenging broadband circuits to design, because they must deliver very large currents in combination with high voltage swings. 10 Gb/s modulator drivers have been designed in CMOS and more precisely in 0.18 μm CMOS [1]. However, complete switching of the CMOS driver stage imposes large input swings and/or wide transistors, both of which make the design of the predriver stage difficult [1]. Consequently substantial currents are needed in the predriver to

overcome these difficulties. Expensive GaAs and InP technologies are also often used in the driver design [2–8]. On the other hand, SiGe BiCMOS technology is an affordable option and drivers have been designed in 0.35 μm, 0.25 μm and 0.18 μm technologies [9–11].

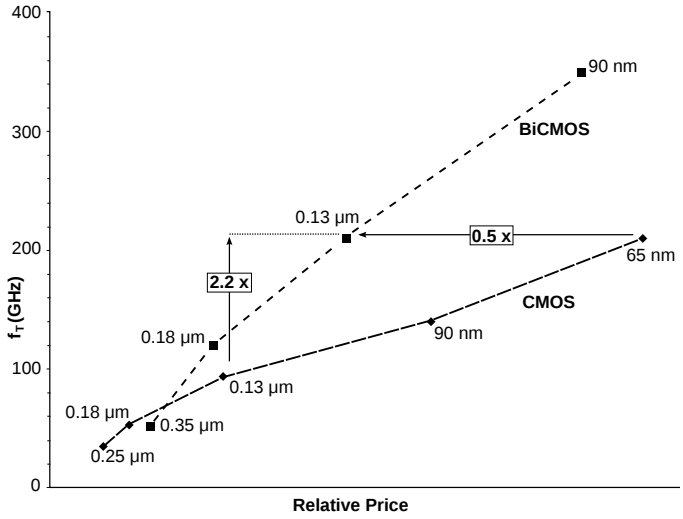


Figure 4.1: Comparison of price vs. performance of BiCMOS and CMOS

The price versus performance difference between BiCMOS and CMOS is illustrated in Figure 4.1 [12]. Even though the development of BiCMOS processes is typically one or two nodes behind, compared to state-of-the-art CMOS, the bipolar transistor is roughly twice as fast as the NMOS transistor of the same technology node. At the same time a BiCMOS process is only half as expensive (per area) as a pure CMOS process with similar speed. Therefore CMOS is mostly attractive when the design contains large digital blocks, which is definitely not the case for this driver array design [13]. Thanks to the analog performance, the price and the availability, the 11.3 Gb/s EAM driver array was realized in a 0.13 μm SiGe BiCMOS process from ST Microelectronics. The node of this technology might be more advanced than necessary, but it was chosen because of an excellent history of cooperation with ST Microelectronics and because no high performance CMOS technology nodes were available in the lab at that time.

4.4 Driver array architecture

Figure 4.2 depicts the top level diagram of the EAM driver array. It includes an input that is differentially matched to 100 Ω and a current divider pair to set the DC-level of the input to enable operation with an AC-coupled input. The first actual stage is a predriver block to amplify the input signal and to drive the large capacitive input of the actual driver. This predriver can also control the pulse width to compensate for the non-linearity of the EAM. The predriver is directly followed by the driver stage, which has a controllable bias and modulation current. The control was implemented using a serial peripheral interface (SPI) [14], which can set both the bias and modulation current with a 4-bit resolution. The bias and modulation current can be set separately for every channel to optimize the operating points of the EAMs according to the transmission wavelength. For testing purposes every channel can also be turned off.

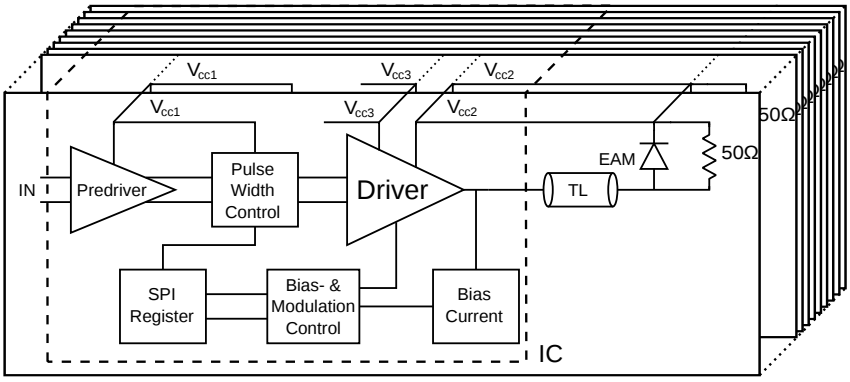


Figure 4.2: EAM driver array IC top level block diagram

To reduce the power consumption, several techniques were implemented in the driver array. First of all, the circuits were designed to operate with a low supply voltage and different supply voltages were used to operate the different circuits with minimum headroom. In this type of analog circuits, the power consumption scales approximately linear with the supply voltage. For this reason, a standard low supply voltage of 2.5 V (V_{cc1} in Figure 4.2) is fed to the predriver, the pulse width control block and all other building blocks outside the data path. The driver stage was supplied up to 4.8 V depending on the modulation and bias voltage required (V_{cc2} in Figure 4.2). The use of the 2.5 V in the predriver also has the advantage that there is no need for additional level shifters to correctly set the output level, as will

be elaborated in detail in Section 4.5. A third power supply of 1.8 V (V_{cc3} in Figure 4.2) was used as well to further reduce the power consumption. This power supply coincides with V_{dd} in Section 3.2.1 and is connected to the dummy arm of the differential pair, which is not used to produce an output signal, but to assure symmetry. Also broadband bias tees were avoided since they are too large to be used in a 10 channel array, both on- and off-chip. Finally, the total number of building blocks was limited. No power consuming retiming circuitry or extra amplifying stages were added, which keeps the architecture fairly simple.

4.5 Predriver stage

The predriver buffers the input ro the last stage, the current steering driver stage. It amplifies the input to a level of typically 500 mV differentially and drives the highly capacitive input of the driver. The circuit is portrayed in Figure 4.3 and consists of a differential pair (Q_1, Q'_1) succeeded by a pair of emitter followers (Q_f, Q'_f). The load of the differential pair contains 2 resistors: R_1 and R_2 (considering half the circuit for simplicity). The resistor R_2 is used to lower the output common mode level of the differential pair and, thus, of the predriver. Lowering the common mode (CM) output level reduces the emitter voltage of the bipolars of the succeeding current steering driver stage. This is necessary to maximize the collector-emitter voltage V_{CE}, which increases the transistor's speed. Considering this configuration, half-circuit analysis shows that the CM level of the differential pair output is set by R_1, while the output swing is determined by the parallel combination of R_1 and R_2. The swing must be restricted to reduce the power consumption, but also to keep the bipolar devices of the following stages out of saturation.

The emitter followers serve as level shifters and impedance transformers. To ensure a low drive impedance, a cascade of followers can be used [15, 16], with as disadvantage both a high supply voltage and current consumption. A follower cascade does give the possibility to integrate a differential active source follower circuit [17, 18], as depicted in Figure 4.4. During the signal transition this configuration temporarily changes the gate voltage of Q_3 through C, drawing extra charge or discharge currents for loading Q_2, speeding up the transition. This technique can improve the bandwidth by over 30%, without additional power dissipation compared to a conventional source follower [18].

Of course the technique can also be utilized for bipolar devices. However, for bipolars the principle of operation lies in the lower drive strength re-

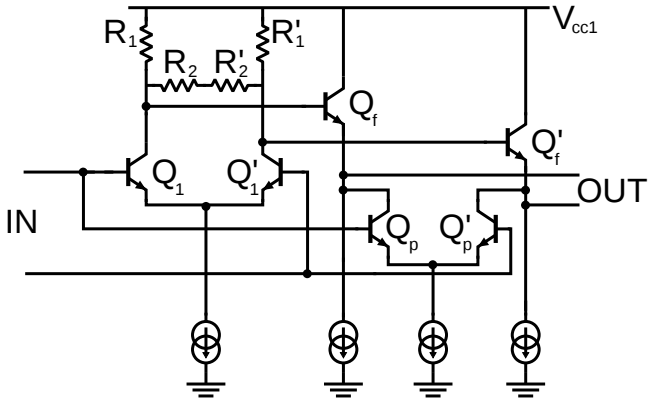


Figure 4.3: Predriver circuit

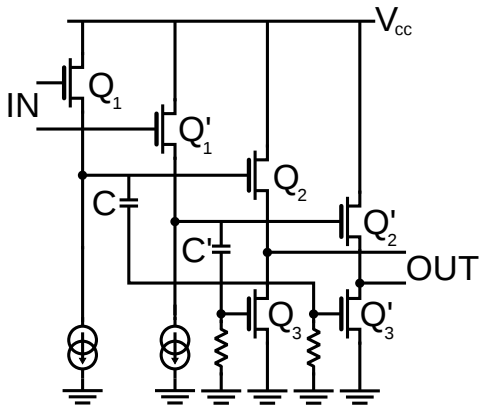


Figure 4.4: Follower cascade with differential active source followers

quired by a bipolar device when turning on than when turning off [19]. This can be understood by examining the base currents of the current steering driver stage transistors, as shown in Figure 4.5. When a bipolar device Q_d is turned off, the current surge out of the base is subtracted from the emitter current of the preceding emitter follower (Q_f, Q'_f). To compensate for this current reduction, the tail current of the follower should increase at every falling edge. In this respect, the emitter follower requires more current when the output data is low. By alternating a current between the pair of followers, sufficient current can be delivered at every falling edge and the current dissipation is reduced. The introduction of such an advanced push-pull configuration was done by a differential pair (Q_p, Q'_p) in Figure 4.3. The inputs of the push-pull differential pair Q_p are equal to the inputs of the predriver instead of being connected to the follower bases, as in Figure

4.4. This was primarily done for time considerations. Q_p needs to switch the current before the output of the follower has a transition, which is not true in case of a follower base connection. Secondly, the DC biasing is optimal when both differential pair (Q_1 and Q_p) inputs are the same. Another advantage of this technique is the reduction in capacitance at the output of the predriver. When a traditional current mirror would be used, a number of transistors are placed in parallel to reduce the reference current. This gives rise to more (parasitic) capacitance than the much smaller bipolars of the differential pair used for the push-pull configuration. A cascode mirror with a small cascode transistor also reduces the capacitance.

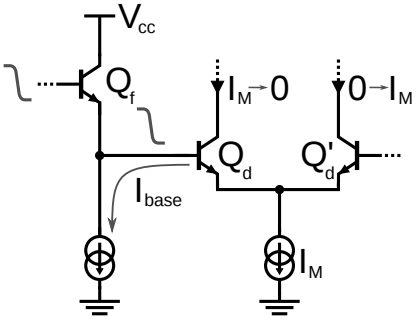


Figure 4.5: Base current at falling edge

Due to the current switching in the emitter followers, there is also an amplification in these followers. The base-emitter voltage V_{be} is dependent on the collector current, I_c:

$$V_{be} \;=\; V_T \, exp(\frac{I_c}{I_s}) \tag{4.1}$$

This leads to a positive correlation between V_{be} and I_c, causing a low input of the follower to give a greater V_{be} than at high input, thanks to the push-pull operation. In this manner the difference between low logic-level data and high logic-level data grows, which corresponds with amplification.

The PWC was also implemented in the predriver, with a simple current mirror according to the technique explained in Section 3.1.5.

4.6 Current steering driver stage

4.6.1 Model of the EAM combined with the interconnect

From an electrical point of view the EAM is mostly a capacitive device. Because the EAM and the driver were designed in parallel, the accurate equivalent capacitance of the EAM was not available. A value of 450 fF was estimated for the model. Due to the small dimensions of the EAM there is also a certain contact resistance in series with the capacitance. This was estimated at 10 Ω. The simple equivalent model of the EAM is represented in Figure 4.6(b).

As it is technologically not possible to directly bond the driver array to the EAM array, the length of the interconnection is not negligible compared to the electrical wavelength. Also, the capacitive nature of the EAM causes reflections at high frequencies and this would distort the eye diagram. As shown in Figure 4.6(a), a 3D model was developed through extensive simulations in CST (computer simulation technology) microwave studio [20]. The model includes the bonding wires, electrical parasitics and the electrical path or (short) transmission line between the driver array and the EAMs, to identify and reduce high-frequency signal distortion. The bondwires were predicted to be 400 μm, while the connection trace was set to 1.5 mm. A short interconnect was added to serve as a launch for the start port, as the port can't be directly connected to a bondwire.

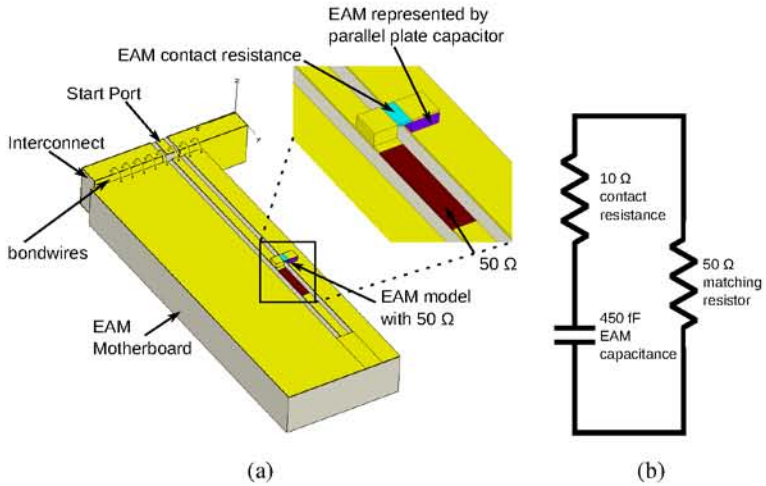


Figure 4.6: CST model (a) of a hybrid assembly with (b) the EAM equivalent circuit

4.6.2 Design of the driver stage

As stated earlier, the current steering driver stage consists of a differential pair (Q_1, Q_1') with two different power supplies to lower the power consumption (V_{cc2}, V_{cc3}), as shown in Figure 4.7. Simulations with the interconnect model showed that the back termination resistor R_{BT} could be much larger than 50 Ω, which led to a choice of 250 Ω. Even though it could be larger, it was kept at this value as higher values only give a marginal consumption reduction, while the design risk increases and the signal quality decreases. To achieve an output voltage swing of 2.5 Vpp, the chosen R_{BT} necessitates a modulation current I_{MOD} of at least 60 mA. Compared to an R_{BT} of 50 Ω, which requires 100 mA of modulation current, this is a reduction of 40%.

The extra supply voltage V_{cc3} was lowered from 4.5 V to 1.8 V, giving a power consumption reduction of 30%, without taking I_{BIAS} into consideration. To guarantee sufficient headroom for both transistors in the driver differential pair, the dummy load resistor R_D needs to be smaller than the parallel combination of R_{BT} and the external 50 Ω. It was set to 12.5 Ω, producing a swing of 750 mV. The reduced R_D lowers the amplification at the left dummy arm compared with the amplification at the actual output, which leads to an asymmetry. As a consequence the supply voltages need to be decoupled very well, with decoupling capacitances of at least 150 pF per driver. This is achievable as there is an abundance of space for on-chip decoupling thanks to the array configuration.

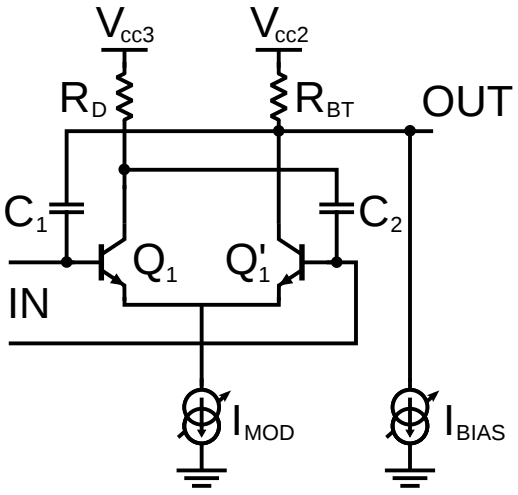


Figure 4.7: Driver circuit

To reduce the current dissipation of the preceding emitter followers, the input capacitance of the stage was lowered by introducing two cross-coupled capacitors (C_1, C_2). These become negative capacitances by exploiting the Miller effect [21]. The principle relies on a non-inverting gain that is larger than one: A > 1. By connecting a capacitance C across the non-inverting amplifier, the Miller capacitance becomes negative: $(1 - A) \cdot C$. In this respect, the collector-base Miller capacitance of the bipolar devices C_{bc} can be compensated. The asymmetry has to be taken into account and its effect is double. Firstly, the Miller effect has a minor influence on the base of Q_1, because the amplification A_s is smaller in this arm. Secondly, the amplification of the output A_l is larger, so C_1 can be small. For C_2 the inverse reasoning is valid. The Miller effect is more prominent in Q_1' and the amplification of the left arm is smaller, giving rise to a large capacitance. Both expressions are shown in Equations 4.2 and 4.3.

$$(1 + |A_s|).C_{bc} = (|A_l| - 1).C_1 \tag{4.2}$$

$$(1 + |A_l|).C_{bc} = (|A_s| - 1).C_2 \tag{4.3}$$

The ratio of C_2 and C_1 can be calculated by dividing both equations and becomes:

$$\frac{C_2}{C_1} = \frac{A_l^2 - 1}{A_s^2 - 1} \tag{4.4}$$

Considering full switching, this gives a ratio of approximately 12.5.

Simulations revealed that a simple differential pair was sufficient to withstand the large collector-emitter voltages produced. Although the BV_{CEO} was specified at 1.8 V, the small resistance seen by the base of the driver transistors increases the actual breakdown voltage considerably. Of course the simulations were only trusted because ST Microelectronics sufficiently documented the trustworthiness of their high current model (HiCuM) [22].

The transistor sizes were chosen such that the emitter's current density was 0.8 mA per μm of emitter length. This decision considers both transistor speed (f_T) and (parasitic) capacitances [23]. Larger devices would have low f_T and more parasitic capacitance, while smaller devices would give larger base capacitance and a decrease of f_T due to high-current effects (Kirk-effects [24]). It was also taken into account that the desired voltage swing, and with it the modulation current, could be smaller or larger. To accommodate all of the current, the transistors were split up into 4 parallel devices, each with 3 emitters. Also the resistors R_D and R_{BT} were split up in a number of parallel resistors not to exceed the maximum current density.

R_D was even divided into 6 parallel resistors of 75 Ω, each with a width of 16 μm to be able to withstand the large modulation current. In this respect also special attention was given to the widths of the traces, that conduct the massive amount of current.

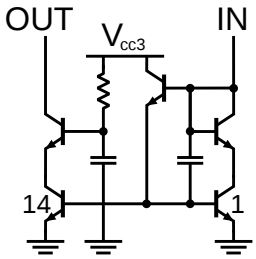


Figure 4.8: Bias current source made of a cascode mirror

Next to the current steering differential pair, also the bias current source is of great importance to set the reverse EAM bias voltage. The current source needs to sink a constant DC-current, while its output experiences a large voltage swing. As a result, a large output impedance is desired in combination with the ability to endure a substantial voltage across it. Furthermore it should add as little capacitance as possible to the output. Figure 4.8 shows the used cascoded mirror. It utilizes high-voltage transistors to sustain the large emitter-collector voltage and the cascode transistor was made as small as possible to limit the capacitance.

4.6.3 Higher power consumption driver approach

In the 10-channel array, only the first 5 channels were integrated as previously mentioned. As a back termination resistor of 250 Ω is much larger than the conventional 50 Ω, there is a risk of imperfect matching, despite the accurate interconnect model. For this reason the last 5 channels of the driver array incorporate a safe approach driver stage with a back termination resistor of 100 Ω. Due to the smaller R_{BT} both I_{MOD} and I_{BIAS} have to be increased by 25%. Consequently the current steering transistors are enlarged with the same ratio, which makes the input capacitance larger, despite a similar increase of the cross-coupled capacitors. To compensate this capacitive rise, the current steering differential pair was slightly degenerated with a resistance R_E of about 1.3 Ω, as illustrated in Figure 4.9. Even though this is a very small value, a current of 75 mA will still give a swing of 100 mV across the resistor. The topology of the predriver remained the same, apart from a slight rise in the emitter follower current.

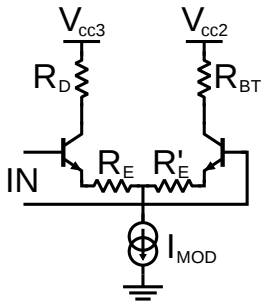


Figure 4.9: Degenerated driver circuit

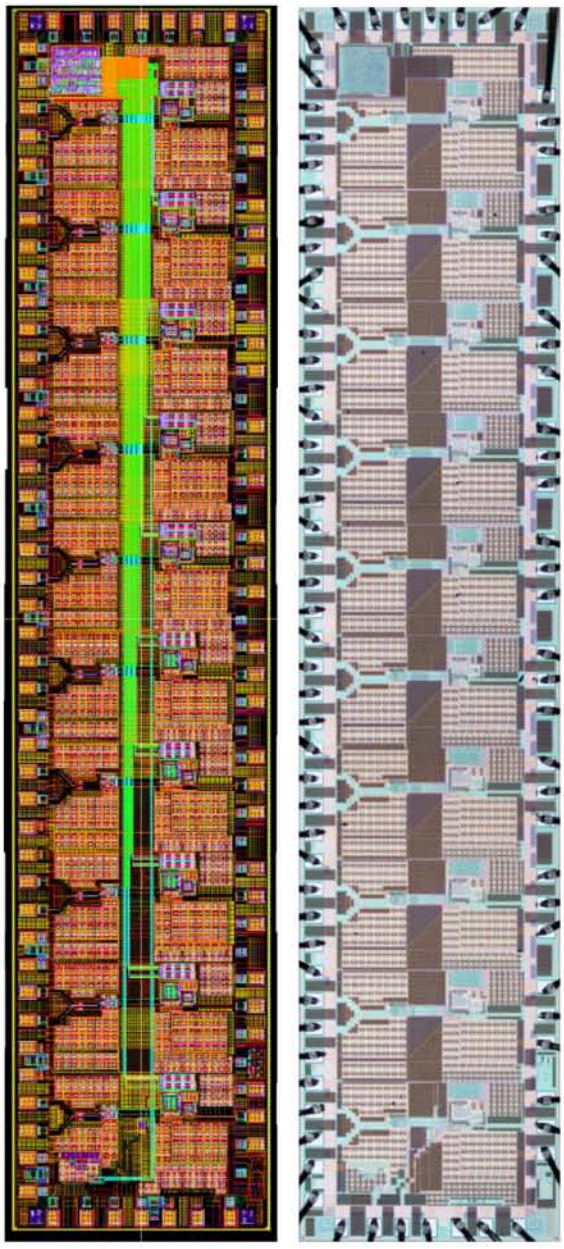
4.7 Realization of the 10-channel 11.3 Gb/s/ch EAM driver array

The measures taken to test the 10-channel 11.3 Gb/s per channel EAM driver array will be described next. Both the layout and pinout of the chip and the printed circuit boards (PCB) for testing will be examined in more detail.

4.7.1 Chip layout and pinout

Figure 4.10(a) shows a screenshot of the chip layout, while Figure 4.10(b) shows a micrograph of the manufactured die, which measures 5.5 mm by 1.2 mm. The array of 10 separate driver channels is clearly visible. The dimensions are mostly determined by the 500 μm pitch between the 10 EAM channels and the number of input/output (I/O) pads. This gives sufficient room for on-chip decoupling capacitances, 2.5 nF of decoupling is present for each supply.

The precise pinout and the bonding of the chip are depicted in Figure 4.11. Because of PCB manufacturing restrictions it was necessary to have a spacing of about 500 μm between the bondpads of the input and signal lines (lower side of the figure). This gives rise to longer wirebonds than anticipated, but this was not expected to affect the driver performance. The decoupling capacitors were placed as close as possible to the chip to minimize the effect of parasitic inductance between the IC and the capacitors.



(a) (b)

Figure 4.10: 10-channel EAM driver array: (a) layout and (b) micrograph

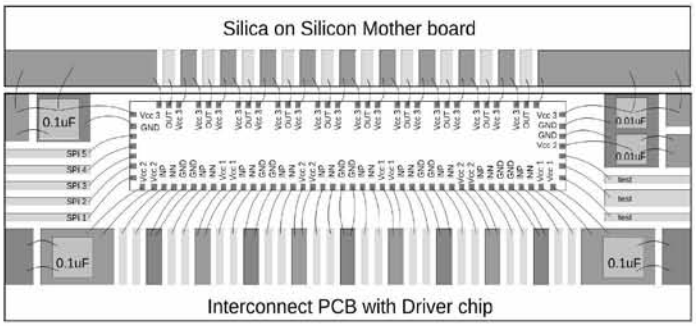


Figure 4.11: Pinout of the 10-channel EAM driver array with decoupling

4.7.2 Prototyping of the 10-channel 11.3 Gb/s/ch EAM driver array

As the die is tested both electrically, with an oscilloscope at the output, as optically, directly connected to a motherboard containing the EAMs, two test boards were developed. The optical test board is shown in Figure 4.12. It incorporates ten 100 Ω differential grounded coplanar waveguide (GCPW) transmission lines to connect the input. The electrical test board also holds 50 Ω single ended GCPW transmission lines for the output. To limit the test board's size and cost only four channels were tested: 2 low power consumption channels with 250 Ω back termination and 2 higher power consumption channels with 100 Ω back termination. The board is shown before and after assembly in Figure 4.13(a) and Figure 4.13(b) respectively. The transmission lines were designed by iterating between ADS Momentum, an EM field simulator and Mentor Graphics. The power supplies, the SPI-signals and the necessary external resistor are provided by an extra board that can be connected to both test boards. It is shown on the top of Figure 4.17.

The PCBs were finished in soft gold to have an optimal surface for bonding. Because the IC is directly bonded to the board, the pitch between the traces near the die needs to be extremely small. Figure 4.14 shows the small trace ends together with the die bonded to the PCB. The represented bondwires appear to be much longer than the initially estimated 400 μm.

To validate the correct design of the 100 Ω differential input transmission lines the return loss S11 was measured up to 67 GHz with a 4-port Agilent PNA-X. The results in Figure 4.15(a) show an S11 of less than -14 dB up to ∼7 GHz and below -10 dB up to ∼12 GHz.

Mentor Graphics' HyperLynx was used to convert the data into a time do-

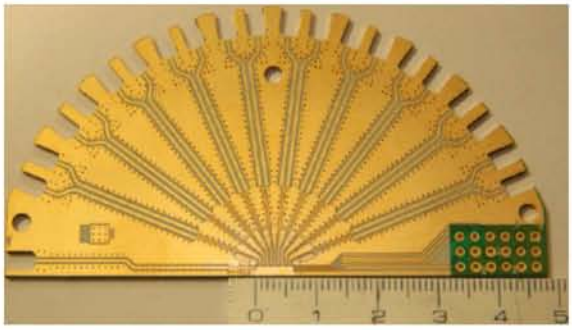
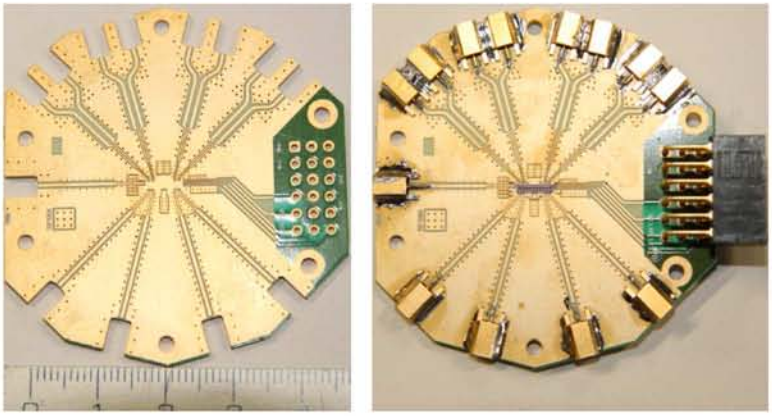


Figure 4.12: Unassembled optical test PCB board



(a) (b)

Figure 4.13: 10-channel EAM driver array electric test board: (a) before assembly and (b) after assembly

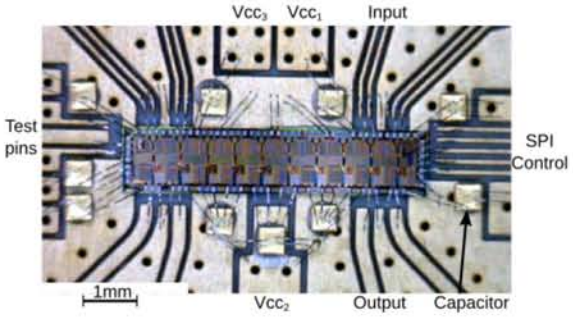
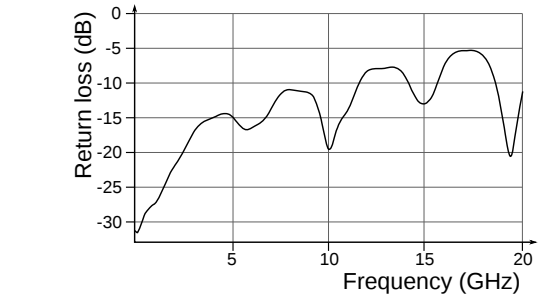
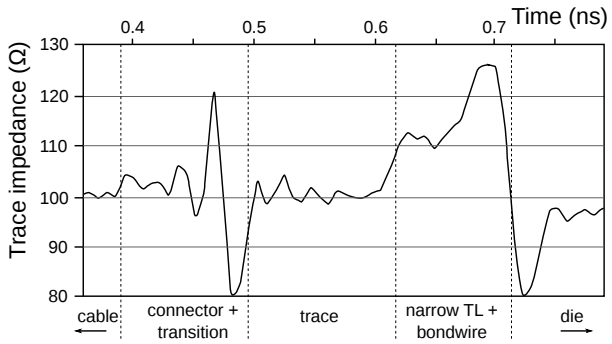


Figure 4.14: Bonded die of the 10-channel EAM driver array

main reflectometry (TDR) response [25]. Figure 4.15(b) clearly shows the different parts of the connection and their characteristic impedance. The employed mini-SMP connector is indicated by 3 small bumps followed by a large peak up to 120 Ω and a dip down to 80 Ω. The peak and dip can be attributed to the transition from connector to PCB. The peak is produced by the inductance of the connector pin without a PCB trace beneath it, as there is an air gap between the connector and the PCB. The dip is the result of the pin soldering and a slight misalignment of the pin on the trace due to fabrication deviations. Precise connector footprint design can resolve the issues [26].



(a)



(b)

Figure 4.15: Differential input transmission line measurement with a bonded die: (a) S11 (b) TDR

The first part of the trace appears to be correctly matched. Closer to the die the trace narrows down in two steps, resulting in two rises of the characteristic impedance. The deviation from 100 Ω can be attributed to fabrication tolerances, which become more critical as the trace becomes narrower. Also the bondwires will have a contribution to this inductive peak. The dip at the

beginning of the die can be assigned to the capacitive nature of the I/O pad and ESD-diodes. The die's input impedance seems to be quite close to 100 Ω, indicating little IC process variation.

4.8 Experimental test results

The electrical and optical evaluation of the 10-channel EAM driver array will be discussed next. Results obtained electrically with the oscilloscope as load and with a commercial EAM will be examined, together with the results of the integrated optical array.

4.8.1 Validation of the test setup

The measurement test setup for the electrical tests is shown in Figure 4.16. A bias-tee was placed at the output to emulate the same DC operating conditions as when the driver is connected to an EAM (with the cathode to V_{cc2}) shunted with a 50 Ω termination resistor. This was necessary because the load is a 50 Ω oscilloscope, which is DC-coupled to ground, while the EAM load would be connected to V_{cc2}. A 20-dB attenuator was added to avoid overloading the high-speed oscilloscope. Figure 4.17 shows a picture of these devices.

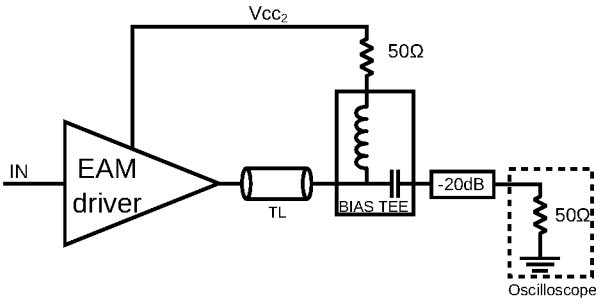


Figure 4.16: Experimental setup for the electrical testing

4.8.2 Electrical experiments

Measurement results of a standard 2.5 V_{pp} electrical eye diagram are shown in Figure 4.18(a), with the 50 Ω oscilloscope as load instead of the EAM [27, 28]. These were measured at the output of the driver with a data rate of 11.3 Gb/s and a 2^{31}-1 pseudo random bit sequence (PRBS). Multiple adjacent channels were measured to check the influence of crosstalk, which was

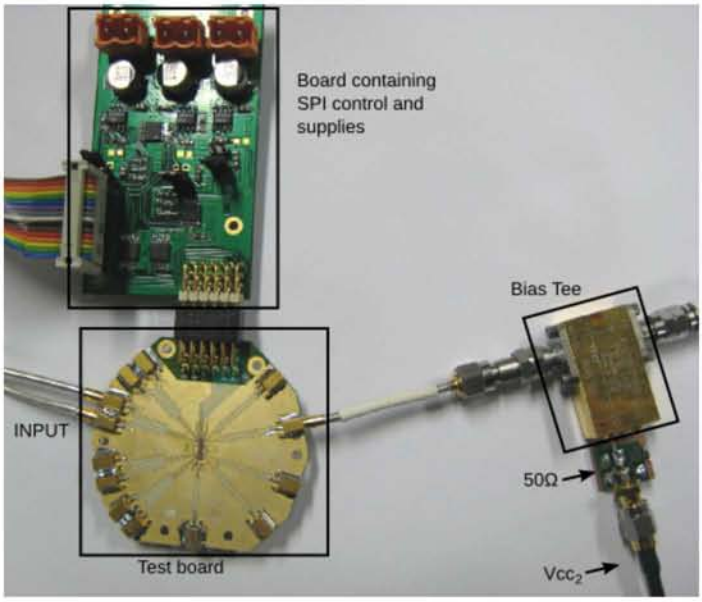
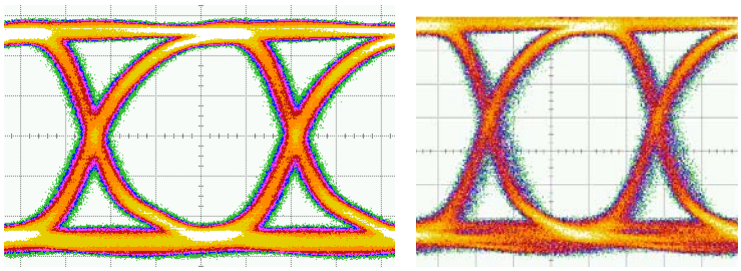


Figure 4.17: Picture of the devices used in the test setup for the electrical testing

negligible. With a differential input voltage of 600 mV_{pp} and a supply voltage of 4.5 V a swing of 2.5 V_{pp} is reached consuming only 188 mW on-chip and 31 mW in the external 50 Ω, resulting in a total power consumption of 219 mW per channel. The 20-80% rise/fall times are 24 and 31 ps respectively. The measured output jitter is 18.3 ps_{pp} and 2.45 ps_{rms}, using a data generator with a measured jitter of 14.6 ps_{pp} and 2.25 ps_{rms}. Even though the driver was designed for a swing of 2.5 V_{pp}, a maximal swing of 3 V_{pp} could be achieved, as shown in Figure 4.18(b). Also the pulse width control operates adequately and the programmable crossing point can be adjusted between 38.6% and 59.4% in 8 steps, as shown in Figure 4.19.

A comparison with the power consumption of previous works is shown in Table 4.2. (Note that it isn't always clear whether the papers only report the on-chip power consumption or also include the dissipation in the external resistor.) This table only contains single driver chips, except for our presented work. The lowest power consumption reported was 470 mW, which shows that this work is 50% below the state-of-the-art in power consumption. Even though [33] has twice the power consumption and the data rate is 10 times lower than the rate in this work, its output swing is considerably higher. By using the techniques reported here, a swing of 3.9 V_{pp} would



(a) (b)

Figure 4.18: Output signal at 11.3 Gb/s for a 2.5 V_{pp} (a) output and a 3 V_{pp} (b) (2^{31}-1 PRBS, 0.5 V/div, 20 ps/div)

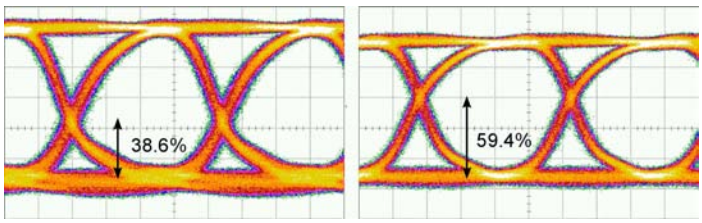


Figure 4.19: Pulse width control, (a) minimum, (b) maximum (2^{31}-1 PRBS, 0.5 V/div, 20 ps/div)

give a power consumption of 405 mW. In [33], however, no back termination resistor was used. Applying this to our work, would decrease the power consumption to 335 mW, which is almost 30% lower, but at 10 times the data rate. The power to data rate ratio of [30] is similar to our work, but only a swing of 1 V_{pp} is achieved. If this work would be designed for a swing of 1 V_{pp}, the power consumption would be below 90 mW. This gives a power to data rate ratio that is less than 40% of [30].

Ref.	Power (mW)	Freq. (Gb/s)	Output Swing (V_{pp})
[29]	980	10	2
[30]	850	40	1
[31]	800	10	4.5
[32]	675	10	2
[33]	470	1.25	3.9
this work	**220**	**11.3**	**2.5**

Table 4.2: Power consumption comparison

Figure 4.20 shows the range of output swings and output bias voltages together with their corresponding power consumption. It indicates a power consumption as low as 200 mW for a swing of 2.4 V_{pp} and below 300 mW for a swing of 3 V_{pp}. The power dissipation increases considerably when the bias voltage across the EAM goes up, even though the swing remains the same, especially at higher modulation voltages. This can partly be designated to the increase of the supply voltage, but it is mostly due to the increase of the bias current. Note that a great portion of this rise in power consumption is consumed in the external 50 Ω. In the case of a 3 V_{pp} output swing the power consumption grows from 288 mW to 401 mW for minimum to maximum bias, which corresponds to an increase of 113 mW or 40%. The power consumption in the external 50 Ω grows from 45 mW to 92.5 mW, which is a difference of 47.5 mW or 42% of the total increase. This points out that the on-chip power and heat generation isn't that profound, making a coolerless operation still possible.

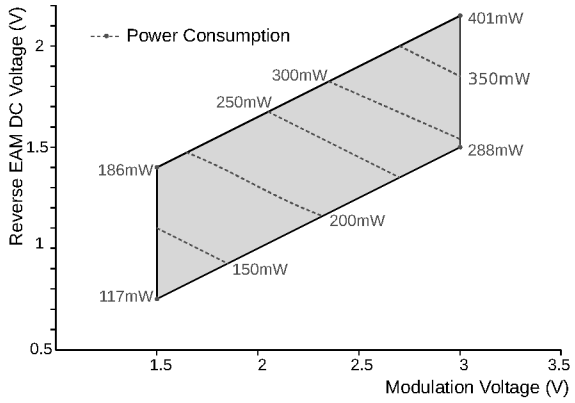


Figure 4.20: Reach of the modulation and bias voltage with the corresponding power consumptions

4.8.3 Optical experiments using a commercial component

Figure 4.21 shows the measured optical eye diagram at a data rate of 10 Gb/s using a commercially available 10 Gb/s EAM. An ER of 8 dB was measured with a 2^{31}-1 PRBS sequence, consuming as little as 173 mW on-chip, while reaching an output voltage swing of 2.5 V_{pp} with a bias voltage of 1.7 V, which was set by a bias-tee.

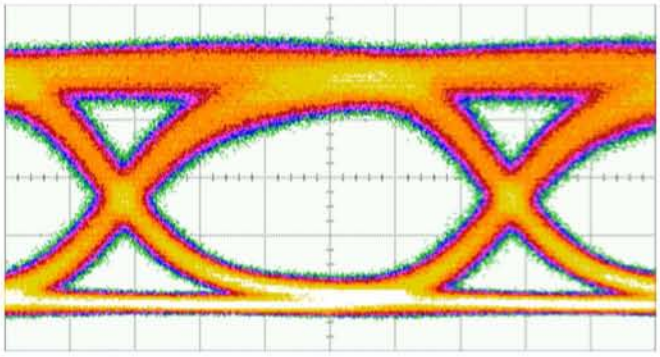


Figure 4.21: Optical eye diagram at 10 Gb/s (2^{31}-1 PRBS)

4.8.4 Integration and validation of the optical EAM array

The 10-channel EAM driver array was integrated into a multi-channel TX PIC by CIP (Ipswich, UK). The multi-channel transmitter assembly is composed of a single array of 10 ridge structure-based InP REAMs hybrid integrated with an AWG multiplexer, and the 10-channel EAM driver array [34]. Figure 4.22 shows a photograph of the main component blocks. The 10-channel AWG has 100-GHz spacing and is athermalized using polymer-filled slots to avoid wavelength drift with temperature. The REAM array is mounted on a silicon submount and aligned to the AWG silica planar motherboard. The integrated assembly features a single I/O fiber such that the transmitter operates in reflective mode.

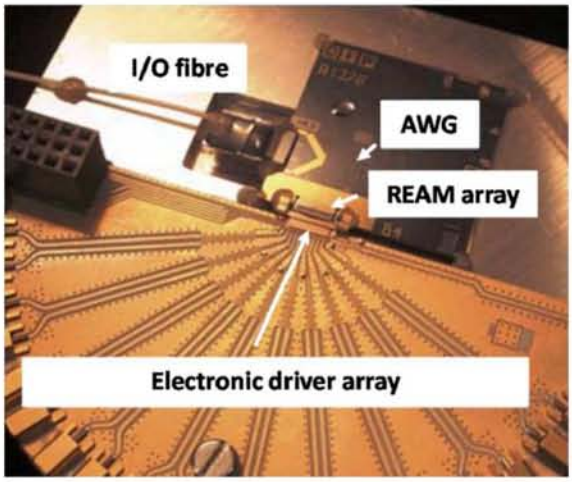


Figure 4.22: Photograph of the optical transmitter assembly

The naked die of the driver array is wire-bonded to an optical PCB with RF connectors and connected to the PIC motherboard. The bond wire lengths were minimized to reduce inductance. During packaging of the first prototype, three channels were damaged. As a result, the following experiment evaluates the 7 functional channels of this proof-of-concept assembly.

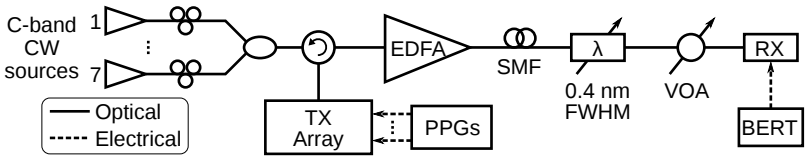


Figure 4.23: Testbed at Tyndall National Institute for evaluating the integrated transmitter array at 11.3 Gb/s

The test bed developed and operated by Tyndall National Institute (Cork, Ireland) is shown in Figure 4.23. Seven C-band CW carriers, aligned to the transmitter's 100-GHz AWG (λ = 1543.59-1548.37 nm), are generated. The optical carriers are passively combined and injected into the reflective TX via a circulator which is connected to the assembly's I/O fiber. The 11.3 Gb/s NRZ (2^{31}-1 PRBS) drive signals for the transmitter array are simultaneously generated by separate decorrelated pulse pattern generators (PPGs). Each channel is driven differentially by a 500 mV_{pp} signal. The transmitter's modulated signals emerge from the output port of the circulator. The dynamic insertion loss of the arrayed assembly is approximately 25 dB per channel, so the output signals are then amplified by an erbium-doped fiber amplifier (EDFA). This loss can be reduced by optimizing coupling losses between the REAM array and the silica waveguides, as well as monolithically integrating the REAMs with semiconductor optical amplifiers (SOAs). The array's transmission performance is evaluated using SMF lengths varying from 0 km (back-to-back (B2B)) to 96 km (a second EDFA was required at 96 km). The launch power into the SMF was kept below 6 dBm to mitigate non-linear effects. At the receiver side, a tunable wavelength filter with 0.4 nm full-width half-maximum (FWHM) emulates the bandwidth of a 100 GHz AWG and minimizes the ASE falling on the RX. The chosen wavelength channel is sent to a variable optical attenuator (VOA), then to a 10 Gb/s RX coupled to a bit-error rate tester (BERT) for BER analysis. The optical signal-to-noise ratio (OSNR) was kept sufficiently high ($>$28 dB) such that the receiver thermal noise floor provided the dominant impairment in the system.

Single channel B2B performance of the transmitter was evaluated first by turning on each channel separately, permitting individual assessment of the

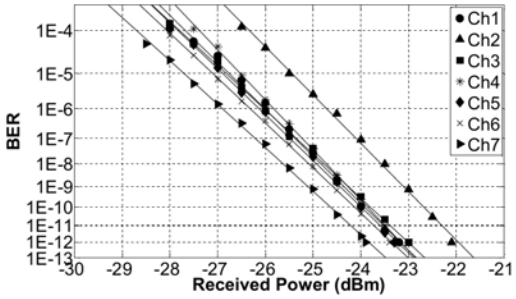


Figure 4.24: BER as a function of received power for Ch1-7 in B2B single-channel operation

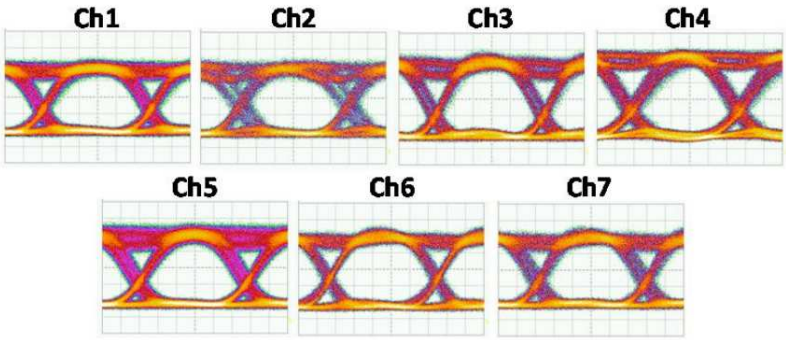


Figure 4.25: 11.3 Gb/s optical eye diagrams for Ch 1-7 in B2B single-channel operation (15.2 ps/div)

array's 7 operational channels (Ch1-7) at 11.3 Gb/s. The driver was set to a swing of 2.5 V_{pp} and a reverse EAM bias of 1.7 V. Error-free operation of each channel at 11.3 Gb/s was achieved with BERs below 1 x 10^{-12}, showing comparable sensitivity performance across all the channels. Figure 4.24 shows less than 2 dB difference in sensitivity between the 7 channels. Correspondingly, Figure 4.25 presents the single-channel B2B optical eye diagrams for the 7 channels, which show significant eye openings for all 7 channels. For the above REAM bias and modulation settings, the measured ERs range from 7.6 dB to 9.8 dB. Ch2 shows the worst sensitivity (by 1 dB), which can be observed from the slightly-degraded eye.

Subsequently, the arrayed transmitter's multi-channel performance was evaluated by operating all 7 channels simultaneously. The center channel in the functional set (Ch4 within Ch1-7) was chosen as the target channel, in order to provide a worst-case study of any possible electrical or optical crosstalk

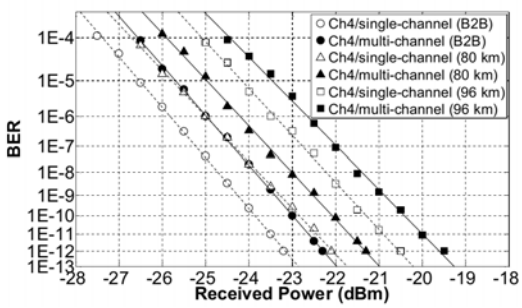


Figure 4.26: BER as a function of received power for Ch4 in single- and multi-channel operation

arising from the non-target channels in the array. Figure 4.26 provides the BER sensitivity curves for the single- and multi-channel operation cases. For B2B, a penalty of less than 1 dB (at a BER of 10^{-9}) is observed for Ch4 with all other channels turned on. No error floor resulted from multi-channel operation, indicating no discernible crosstalk effects in the array. Instead, the observed penalty was found to be due to a slight increase in REAM temperature resulting from heating by the driver when all channels were turned on. Such a temperature increase causes a red shift of the REAM band edge, which alters the bias and modulation operating point. In principle, this effect can be alleviated by mounting the TX assembly on a heat sink or TEC. By stabilizing the device's temperature, the TEC aims to restore the optimal bias and modulation operating point. However, in the current prototype, the REAM array is in poor thermal contact with the TEC (which sits under the assembly's evaluation board), thus the thermal effects cannot be completely mitigated. Operating the REAM at the driver's lowest possible bias and modulation settings compensates for this to some degree. However, this does have a decrease in ER as result (from 8.5 dB to 7.2 dB for Ch4). Ultimately, this ER reduction gave rise to a small residual penalty. In future versions of the TX, the penalty could be reduced by placing the optical devices in direct contact with the TEC or by blue-shifting the REAM band edge to achieve optimum modulation and biasing conditions at elevated temperatures. Of course the integration of 5 channels with a safe driver approach increased the total current dissipation and, thus, the heating. If all channels were integrated with a 250 Ω back termination resistor, the problem could be alleviated.

Lastly, the array's performance was analyzed after transmission over 80 km and 96 km of SMF, respectively (Figure 4.26). After 80 km (the intended reach for WDM-PON), a RX sensitivity penalty of approximately 1

dB was observed for the target channel. This 80 km transmission reach was consistent with prior results of EAMs at 10 Gb/s. Furthermore, error-free performance was maintained for distances up to 96 km for both the single- and multi-channel cases. At these distances, the performance degradation is due to chromatic dispersion, which leads to intersymbol interference and thus some eye closure. The extra $<$1 dB penalty that arises from concurrently operating several channels seen in B2B is preserved at both 80 and 96 km.

4.9 Conclusion

The measurements show that a driver array of 10 channels, each with an output voltage of 2.5 V_{pp}, can be achieved while consuming less than 2.2 W for the total 113 Gb/s transmitter. To the best of the author's knowledge such EAM driver arrays are not currently available on the open market, nor published in the literature. This is the first 10-channel EAM driver array and the lowest power consumption for an EAM driver so far reported, 50% below the state of the art in power consumption. The excellent signal quality revealed by the electrical eye diagrams gave the possibility to demonstrate a novel multi-channel REAM-based transmitter with integrated driver. The TX PIC showed error-free performance over 96 km, without significant crosstalk. A minor penalty of 1 dB is measured for multichannel operation, due to driver-induced heating of the REAM array. The co-optimization and integration of a PIC with an electronic driver offers a cost-effective solution for reflective OLT realizations in next-generation WDM-PONs.

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5 Duobinary modulation

In the previous chapter the realization of 11.3 Gb/s NRZ was reported. However, it is challenging to achieve 28 Gb/s with the same technology and a highly capacitive load, such as an EAM. Consequently, optical duobinary was chosen as the modulation format at this high speed. Not only does this modulation scheme reduce the bandwidth constraints, it also offers a number of advantages. The following chapter will discuss the scheme in more detail.

5.1 Introduction

The thirst for increased speed in today's information society results in a desire for higher transport capacities per fiber. In the thrust towards greater capacities, complex modulation formats have become key elements. Over the years dozens of formats have been investigated and compared [1], with the simplest and most commonly known format being non-return-to-zero on/off keying (NRZ-OOK). While this basic amplitude modulation (AM) scheme is easy to deploy in optical communication, it faces limitations at growing data rates and decreasing wavelength spacing in WDM based networks. Another easy-implementable modulation format that isn't as prone to these drawbacks is a duobinary (DB) scheme. It was developed in the 1960's and studied by A. Lender for transmitting binary data in an electric cable with high-frequency cutoff characteristics [2]. A DB signal con-

sists of 3 levels and it can simply be encoded from an NRZ binary input stream. The three-level signal can optically be translated into two intensity logic levels, but with a π phase difference between the 1-levels {-E, 0, +E}, which corresponds to amplitude modulation phase shift keying (AM-PSK), or optical duobinary (ODB). The ODB signal has the advantage that it can be demodulated by a common direct detection receiver.

5.2 Duobinary encoding

Duobinary modulation is the most common form of partial response signaling (PRS), which is an approach of encoding or decoding a signal in order to minimize the errors caused by inter symbol interference (ISI). PRS is based on the premise that since the ISI is known, its effects can be removed [3]. A PRS system is a cascade of a digital transversal filter, $F(\omega)$, and a pulse shaping filter, $G(\omega)$. The digital transversal filter is equivalent to a shift register with *N* taps. It gives the weighted sum of the input signal, b, and *N*-1 delayed versions of the signal, as shown in Figure 5.1.

$$d_n = \sum_{i=0}^{N-1} a_i.b_{n-i} \tag{5.1}$$

Here b_n is the nth bit of the original bit sequence, and a_i is the tap coefficient. In the time domain a binary signal $b(t)$ can be produced using a pulse shape, $p(t)$,

$$b(t) = \sum_n b_n.p(t - nT) \tag{5.2}$$

with T the bit period. This leads to the following analog transfer function in the frequency domain:

$$F(\omega) = \sum_{i=0}^{N-1} a_i.e^{-j\omega iT} \tag{5.3}$$

As the name says, $G(\omega)$ is used to shape the filter and is chosen according to the bandwidth preferences and other considerations, as explained in [3].

For duobinary encoding, $F(\omega)$ is a two-tap finite impulse response (FIR) filter, where both weights are equal, giving

$$d_n = b_n + b_{n-1} \tag{5.4}$$

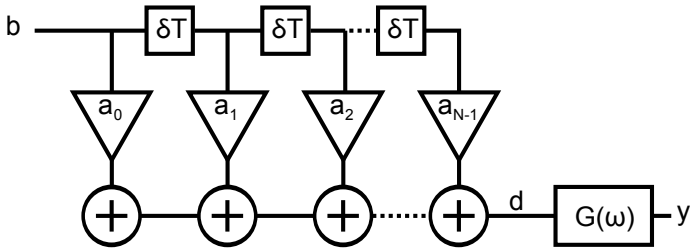


Figure 5.1: Schematical representation of a PRS system

This is also known as a delay-and-add filter (DAF) and it produces a signal with three levels $\{0,\ 1,\ 2\}$ as the bits of the binary sequence are '0' or '1'. The succeeding pulse shaping filter, $G(\omega)$, is an analog low pass filter (LPF) at half the bit rate R as shown in Figure 5.2 [4]. Due to the encoder implementation the three-level duobinary sequence is a correlated signal and hence it is not possible for all sequences to occur. Since it is impossible to have two rising edges that are a bit period T apart in an NRZ binary sequence, a '0' will never be followed by a '2' and vice versa a '2' will never be followed by a '0'. The DAF will also never generate the sequence '010' or '212'. What is more, a '0' followed by an odd number of '1's will always give a transition to a '2', while an even number of '1's will proceed a return to a '0' and vice versa.

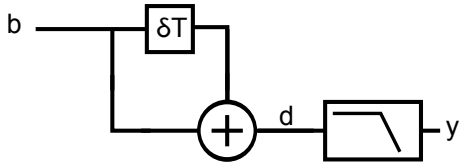


Figure 5.2: Schematical representation of a DB encoder

The DB encoder shown in Figure 5.2 can also be implemented differently. The DAF followed by a LPF can be replaced by a single analog LPF with a 3dB cutoff frequency at about a quarter of the bit rate. Typically, the ideal LPF for a system is a fifth order Bessel filter with a cutoff frequency at 0.28 R [5]. The similarity of both approaches is easily understood when looking at both the spectra, shown in Figure 5.3, where only half of the spectra are plotted. The main lobe has a 3dB cutoff frequency at a quarter of the bit rate, corresponding to the cutoff of the Bessel filter. For the DAF approach, the side lobes of the spectrum are suppressed by the LPF. Moreover the side lobes are suppressed but still present, which makes the single LPF approach

give better results for long reach transmission [6].

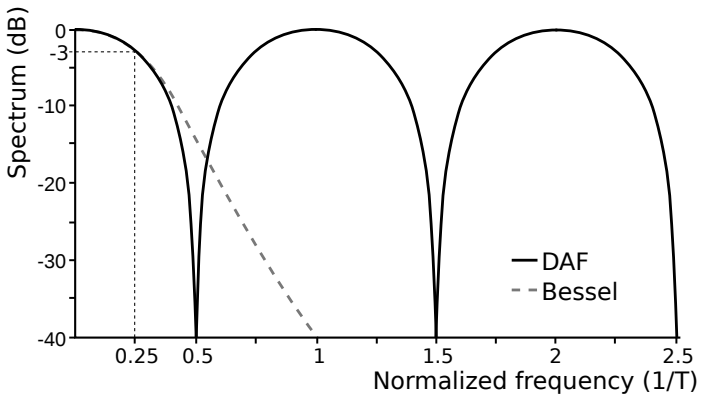


Figure 5.3: Spectrum of a delay-and-add filter compared to a 5th order Bessel LPF in function of the normalized frequency 1/T

Figure 5.4 compares both techniques in the time domain. Ideal block signals are used for simplicity. As an example the precoded data '0100' and '0110' are converted into '0110' and '0121' respectively, indicated by the gray dots. The precoding is explained in the next section. Note that there is a delay due to the encoding, which is not shown for clarity.

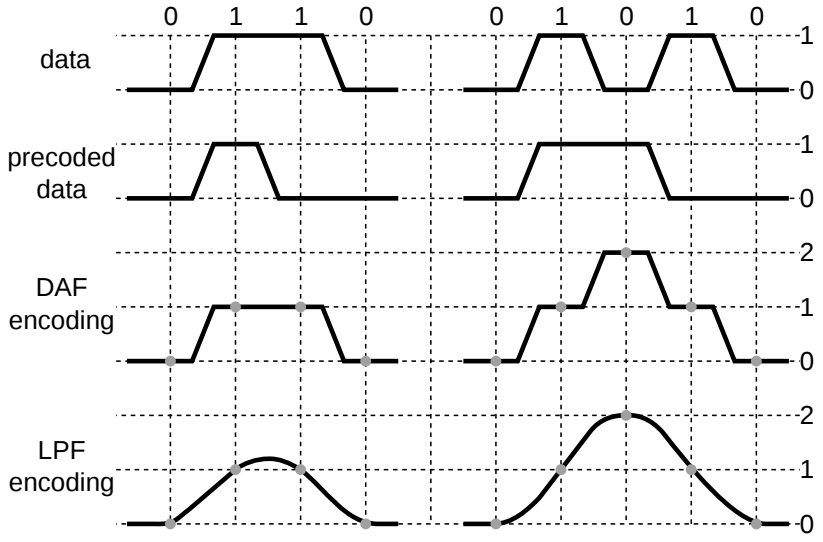


Figure 5.4: Comparison between DAF and LPF encoding

5.3 Duobinary precoding

At the RX side the duobinary sequence d has to be decoded in order to recreate the original bit sequence. As $b_n + b_{n-1}$ is sent, it is assumed that this will be perceived. In this way the RX can use the previously decoded bit, b_{n-1}, to decide on the current bit.

$$b_n = d_n - b_{n-1} \tag{5.5}$$

There are two problems with this type of decoding at the RX. First of all, when a single decision error occurs this error will propagate forever, causing a catastrophic decoding error. Another problem is the ambiguity due to the initial state. Since the decoding relies on the value of the previously decoded bit a problem emerges when the first bit arrives. Looking at expression (5.4), the modulated output is changed by the initial condition. Dependent on whether it is zero or one, the first duobinary symbol, d_0, is equal to b_0 or $b_0 + 1$ respectively, producing an entirely different data sequence.

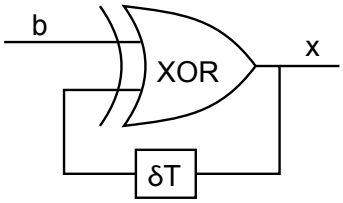


Figure 5.5: Precoder using a XOR-gate

Both problems can be solved by using a precoder at the TX side instead of a decoder at the RX. This precoder exists of a logic exclusive-OR-gate (XOR) that has the output fed back to the input with one bit period delay, as shown in Figure 5.5. The resulting precoded sequence is

$$x_n = b_n \oplus x_{n-1} \tag{5.6}$$

The XOR-gate performs the action of a modulo-2 adder, which results in the fact that the precoder can be implemented in a number of ways, as explained in Section 5.6.1.

The precoding eliminates the ambiguity of the initial conditions after one bit [7]. The truth table for the coding of b_1 is shown in Table 5.1, where x_{-1} corresponds to the initial condition. Now a '1' input always corresponds with a '1', while a zero corresponds with d_1 being '0' or '2'.

x_{-1}	b_0	b_1	$x_0(= x_{-1} \oplus b_0)$	$x_1(= x_0 \oplus b_1)$	$d_1(= x_0 + x_1)$
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	1	2
0	1	1	1	0	1
1	0	0	1	1	2
1	0	1	1	0	1
1	1	0	0	0	0
1	1	1	0	1	1

Table 5.1: Truth table for DB pre- and encoding

Of course the three-level signal still needs to be decoded into a two-level NRZ signal. In the early development of duobinary, the data conversion from duobinary to binary was performed by a simple full-wave rectifier [8]. However, the recent gigabit data rate would require a broad band full-wave rectifier with a flat response across the entire data bandwidth, which is extremely difficult to build. As an effect a more elaborate conversion method was devised [9]. The duobinary data has to be duplicated and then compared with two different thresholds, V_1 and V_2, which correspond to the crossing levels of the duobinary eye diagram, as shown in Figure 5.6. Figure 5.7 shows the duobinary decoding. A comparator compares the three-level DB signal to V_1 and transforms the '2' and '1' into a logic 1, while a '0' remains a logic 0. Another comparator compares the DB signal to V_2 and transforms the '2' into a logic 1 and the '1' and '0' into a logic 0. A XOR-gate then gives the decoded bit stream. Table 5.2 gives a truth table that confirms the correct decoding.

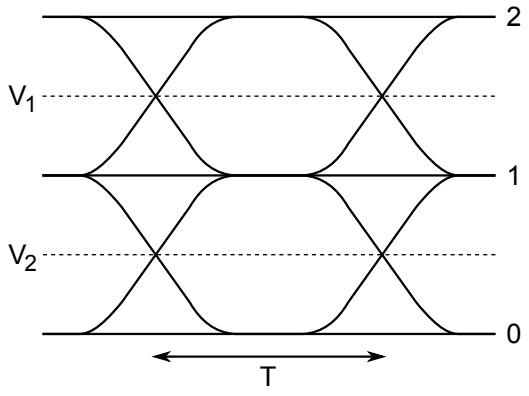


Figure 5.6: Duobinary eye diagram with thresholds V_1 and V_2

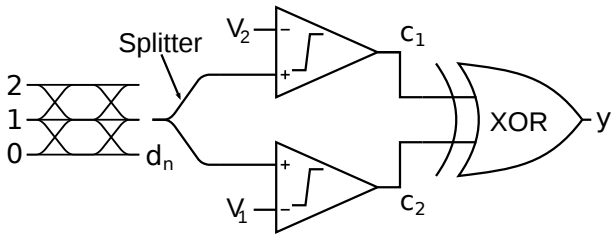


Figure 5.7: Schematic of duobinary to binary conversion

Condition	c_1	c_2	y
d_n = '2' $> V_2$	1	1	0
$V_2 > d_n$ = '1' $> V_1$	0	1	1
$V_1 > d_n$ = '0'	0	0	0

Table 5.2: Truth table for decoding

5.4 Optical duobinary

While it is possible to send a three-level optical duobinary signal through a fiber, the RX still has to convert the duobinary into a two level binary signal and needs to be completely linear, not to deform the signal. However, the duobinary technique can be combined with AM-PSK modulation. In AM-PSK modulation the carrier is amplitude modulated as well as phase modulated in a binary manner. Such a type of phase modulation is usually referred to as phase shift keying (PSK) to denote the discrete phase reversals of the light signal. Suppose the center level of the duobinary signal is represented by the absence of light and the outer levels by a constant-amplitude optical signal, but with a 180° phase difference. In this manner AM-PSK is completely analogous to duobinary but with phase modulation. Remembering the possible sequences of DB explained in Section 5.2, there is a 180° phase reversal if the number of intervening middle levels is odd; otherwise there is no reversal. Because in the AM-PSK system the presence of light, in either phase, represents a '1', at the RX there is no need to make a distinction between the phases, nor is there any need to decode the duobinary signal. As a result a conventional direct-detection (square-law) RX can be used, without any special features.

Typically, an MZM is used to generate the ODB signal. It is biased at its null-point, which causes no light to be transmitted by the center level. The

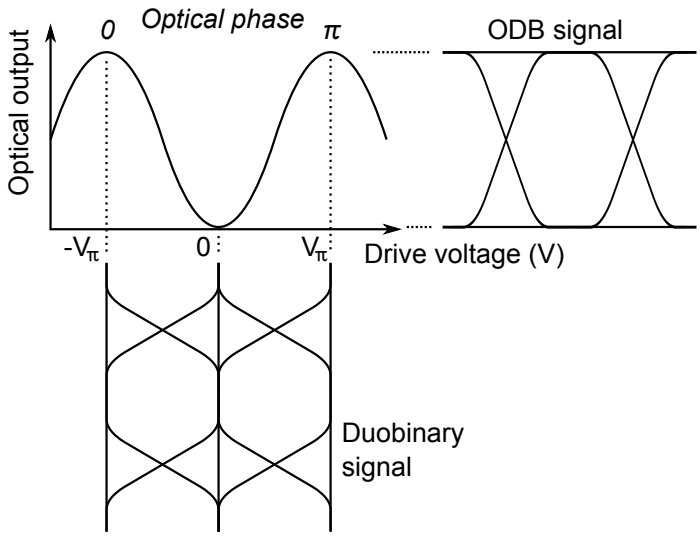


Figure 5.8: Conversion from electric DB into optical DB using an MZM

two outer levels, however, induce a complex optical field $\pm$ E, where the '$\pm$' denotes a 180° phase difference and |E| is the magnitude of the field. To achieve a high ER the MZM should be modulated with twice the half-wavelength voltage $V\pi$, which is generally done by driving it in push-pull. The optical conversion is illustrated in Figure 5.8.

Another option is to use 2 EAMs in a Mach-Zehnder (MZ) configuration. This configuration operates as follows: the positive and negative (three-level) data outputs from the DB encoder are fed to two separate EAMs, of which one is followed by a π-phase shifter, as shown in Figure 5.9(a). The electrical outer levels guarantee an output with a large optical intensity, as in this case one of both EAMs is transparent and thus turned on. Moreover, the 180° phase difference is ensured by the π-shifter. In case of the center level, both EAMs transmit a light signal with an equal optical intensity, which add destructively due to the π phase difference, ensuring a low optical intensity at the output. The advantage of this configuration is the smaller form factor of the EAMs in comparison to the MZM. As a surplus the typical drive voltage of an EAM is generally smaller, which gives possibilities to reduce the power consumption.

When reflective EAMs are employed the architecture is called a Michelson configuration as only 1 coupler is necessary and the arms are traversed twice [11]. This configuration is illustrated in Figure 5.9(b) [10].

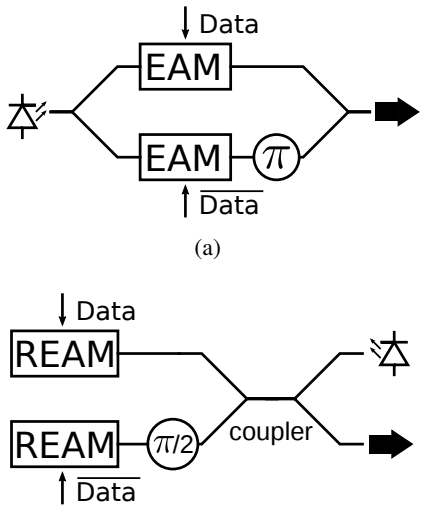


Figure 5.9: (a) EAMs in a MZ configuration and (b) REAMs in a Michelson configuration

5.5 Advantages of (O)DB

Even though the creation of a duobinary modulated signal seems to be more cumbersome than transmitting simple NRZ-OOK, it has a number of advantages. As stated before, duobinary modulation is a scheme that tries to minimize ISI caused by dispersion due to transmission. ISI can be defined as the spreading of symbol energy into adjacent symbols, in which case the tail of a pulse spills over into neighbouring signal intervals [12]. As a result the adjacent symbol shape is corrupted. Nyquist postulated that a channel with a minimum bandwidth of *R*/2 Hz is needed to transmit R symbols per second without ISI [13]. Consequently, *R*/2 is called the "Nyquist bandwidth". Unfortunately this bandwidth efficiency can only be achieved with the use of a brick wall filter, which is impossible to build in practice.

A logical extension of the NRZ binary transmission is the use of multilevel schemes, leading to higher data rates for the same channel bandwidth. In these schemes typically 2^k levels are transmitted, which results in k bits per symbol and thus k times the data rate capability of binary systems. A well-known example of this type of modulation is pulse amplitude modulation (PAM). While the increase in levels provides an extension of the bit rate, it requires a higher signal-to-noise ratio (SNR). This implies that smaller noise levels can now cause a signal level to be more easily confused with

an adjacent signal level. Moreover, the horizontal eye deteriorates rapidly with the increasing number of levels because of the increased number of possible transitions between the levels. This is shown in the PAM4 eye diagram of Figure 5.10, where the eye diagram exists of a stack of 3 'eyes'. Especially the outer eyes are closing horizontally, with the main contributors being the transitions between the extreme levels. All these factors make the performance of multilevel modulation more prone to errors.

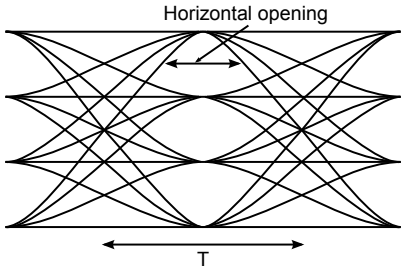


Figure 5.10: PAM4 eye diagram, with horizontal eye opening

Nyquist's work assumes that the transmitted pulse amplitudes are selected independently or, in other words, they are uncorrelated. The correlated PRS, of which duobinary is a part, can achieve a symbol rate of R across a channel with a bandwidth of $R/2$ Hz. Applying a DAF introduces ISI, but in a controlled amount: a symbol only experiences interference from the preceding symbol due to the summing. Since not all possible sequences can occur in duobinary, the problem of the horizontal closure of the eye disappears. Figure 5.11 shows the effect of dispersion for a bit pattern '101' in the time domain. For NRZ the two '1' pulses will broaden, spread into the '0'-bit in between them and add together, which can cause decision errors. When considering the same sequence in optical duobinary (the extension to normal DB is trivial), this is transformed into a sequence '+E 0 -E'. While the pulses will also broaden, they will interfere destructively in the middle due to the π phase difference and thus a clear '0'-bit level will be maintained [14].

In the optical field the tolerance to ISI is translated into a resilience to chromatic dispersion and narrowband optical filtering. This can also be explained in the frequency domain. Consider the data stream is made up of raised cosine pulses with a roll-off factor, β in between 0 and 1. Figure 5.12 plots the raised-cosine pulse shape with the rectangular pulse corresponding to a zero roll-off factor, $\beta = 0$ [15]. Figures 5.13 and 5.14 compare the spectra of NRZ and duobinary for different roll-off factors. It is clear that

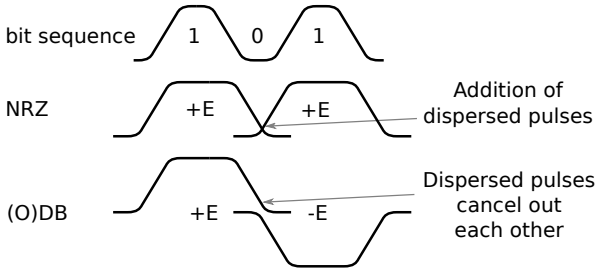


Figure 5.11: Effect of dispersion on NRZ and DB

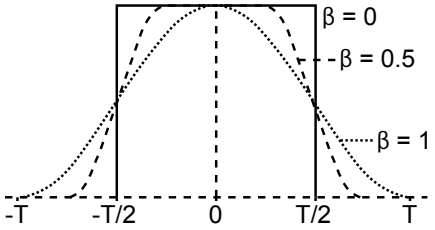


Figure 5.12: Raised cosine pulses with different roll-off β

the spectrum of DB is narrower than that of NRZ, which reduces dispersion induced signal distortions. For completeness the optical spectra of duobinary and NRZ at 10 Gb/s are shown in Figure 5.15 [16]. Additionally, a higher spectral density can be achieved as the channel spacing in DWDM systems can be reduced without additional channel crosstalk.

Of course, next to the resilience to ISI, another straightforward advantage is the reduced bandwidth needed at the transmitter. The possibility of only requiring a bandwidth of half of the data rate and below, can be of great importance when designing a driver that needs to modulate a large capacitive load, such as an EAM.

5.6 Implementation

5.6.1 Precoder implementation

As mentioned in Section 5.3 the precoder can be implemented in a number of ways. Using the XOR-gate with the feedback output of Figure 5.5 is a straightforward and elegant way of doing the precoding. However, at bit rates above 10 Gb/s it becomes difficult to implement [14]. This is due

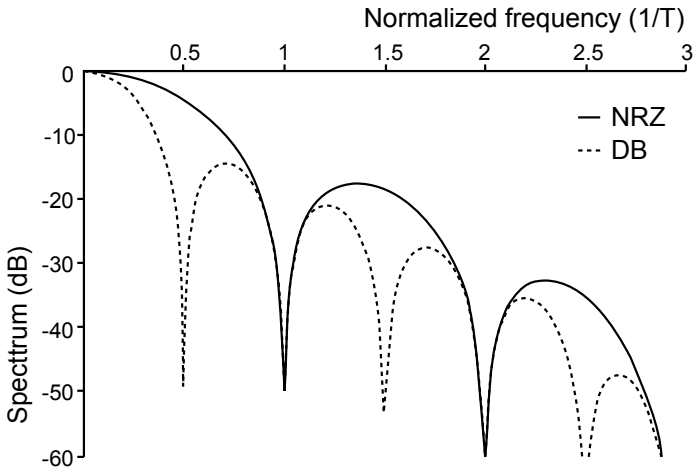


Figure 5.13: Spectrum of NRZ and DB with a raised cosine pulse with roll-off $\beta = 0.5$

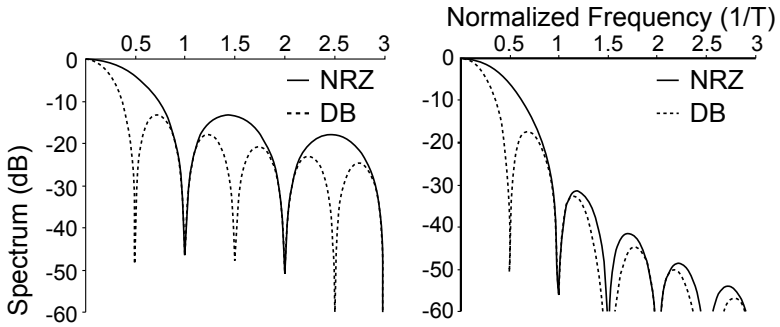


Figure 5.14: Spectrum of NRZ and DB with a raised cosine pulse with roll-off $\beta = 0$ (left) and $\beta = 1$ (right)

to the delay that needs to be exactly 1 bit period, which corresponds to less than 100 ps for rates exceeding 10 Gb/s. Considering process corners and temperature variations, an error of a few picoseconds in the delay is not without foundation. Such an error can cause glitches in the output, especially as at these speeds one uses fast technologies, which can output pulses of a few picoseconds. The glitch is shown in Figure 5.16 for a delay that is smaller than 1 bit period (UI). For a larger delay the result is similar. Note that in the figure it is assumed that the XOR-gate has no delay, which isn't true in reality.

On these grounds it is best to implement the precoder as a modulo-2 adder.

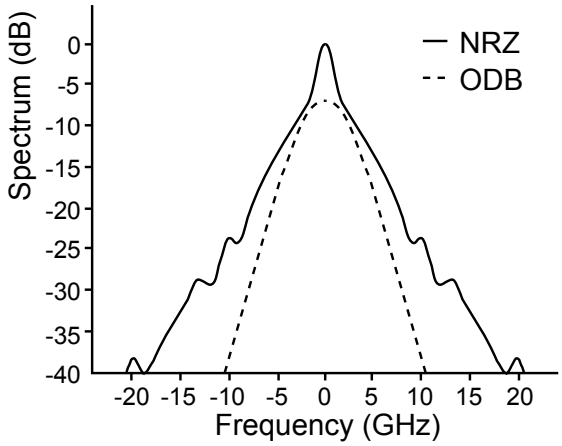


Figure 5.15: Optical spectrum of NRZ and ODB (10 Gb/s) [16]

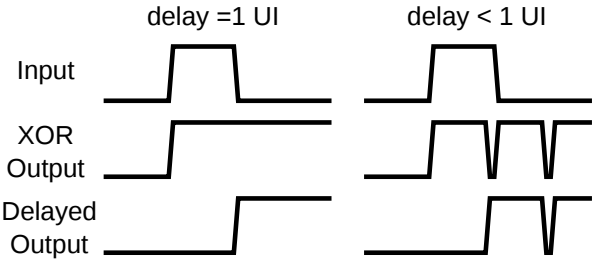


Figure 5.16: XOR-precoder output for exact and fast delay

A T-flip-flop is a possibility to achieve the required functionality. When the input of this component is high, the T-flip-flop changes state or "toggles" (as indicated by the name: "Toggle-flip-flop"). If the input is low, the flip-flop holds the previous value, as illustrated in Table 5.3.
Figure 5.17 shows the T-flip-flop built with an SR-latch and 3 AND-gates. The last two AND-gates and the SR-latch perform the toggling operation. When the input is low, both the R-input (Reset) and the S-input (Set) are low and nothing happens. When both the input and the output (Q) are high, the R-input becomes high and the output is reset to '0' or toggled. With a high input and low output ($\overline{Q}$ is high) the S-input becomes high, which sets the output to '1'.

The first AND-gate is necessary to transform the input into pulses. By performing an AND operation on the input and a clock with the same frequency as the input bit rate, every high input is converted into a pulse that

IN	OUT_{prev}	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Table 5.3: T-flip-flop truth table

is half the bit period wide. If this stage was omitted, a sequence of 1's at the input would cause the T-flip-flop to toggle constantly with a period equal to the combined delay of the AND-gate and the SR-latch. By introducing the clocked input this problem is avoided, as long as the delay is larger than the pulse period. The disadvantage of this approach is that lower bit rates can have too long a pulse period, using a normal clock with 50% mark density, causing the precoder to fail.

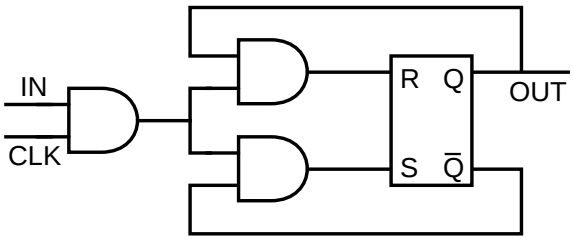


Figure 5.17: Precoder using a T-flip-flop

Notice that when the input is constantly high, the output is a square wave or sine at half the clock frequency and the T-flip-flop essentially becomes a frequency divider. This shows that a frequency divider can be used as precoder. A possible frequency divider configuration uses 2 D-latches that configure a D-flip-flop, as shown in Figure 5.18. A D-flip-flop (Delay-flip-flop) captures the data of the input typically at the rising edge of the clock-input. In Figure 5.18 the input of the D-flip-flop is the inverse of the output. This creates a component that toggles the output at every rising edge of the clk-input, which corresponds to the pulsed data input. This agrees with the precoder functionality. Figure 5.19 gives an example of the frequency divider working as a precoder with a high initial condition.

The main advantage of this configuration is its compliance to operate for a wide range of bit rates, from practically DC to the rate designed for. The circuit does demand accurate synchronization of the input and the clock to assure correct operation. In this case the rising edge of the clock should be

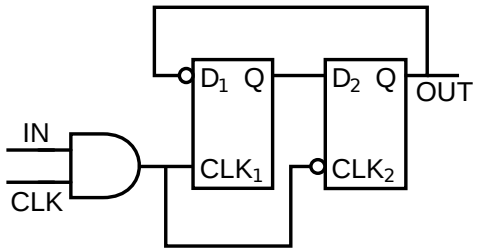


Figure 5.18: Frequency divider used as precoder

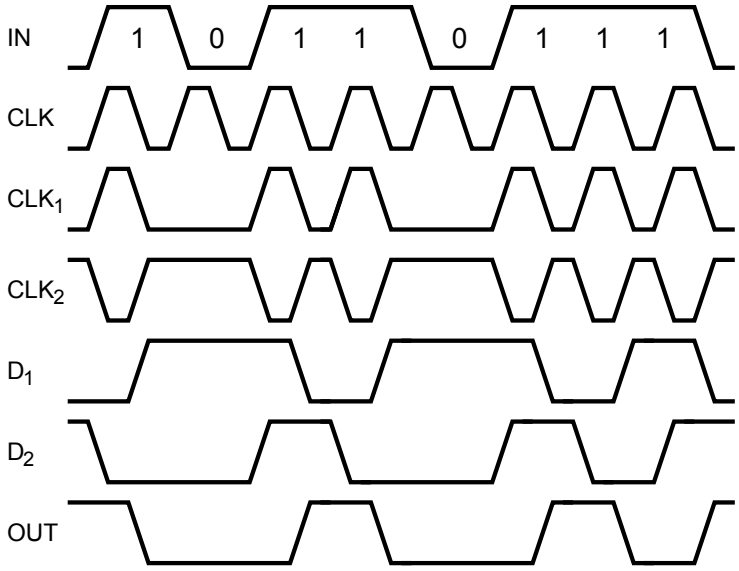


Figure 5.19: Frequency divider as precoder bit example

later then the rising edge of the data. If the input in Figure 5.19 would be delayed, the AND-operation would create two short pulses instead of one, which would lead to two transitions instead of the desired single transition.

5.6.2 Encoder implementation

The encoder is based on a 1 bit delay circuit and an adder. The 1 bit delay circuit can easily be implemented by using D-latches. A cascade of 2 D-latches will exploit the clock already present in the precoder. Because both inputs of the adder need to be synchronized with the clock to ensure an exact delay of one bit period, an extra D-latch will precede the encoder, as

shown in Figure 5.20.

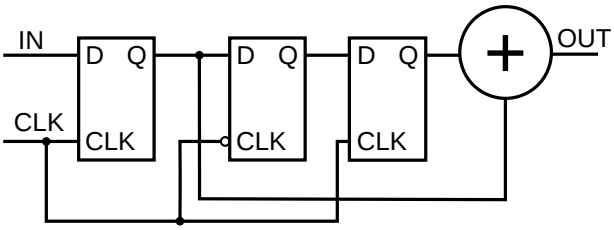


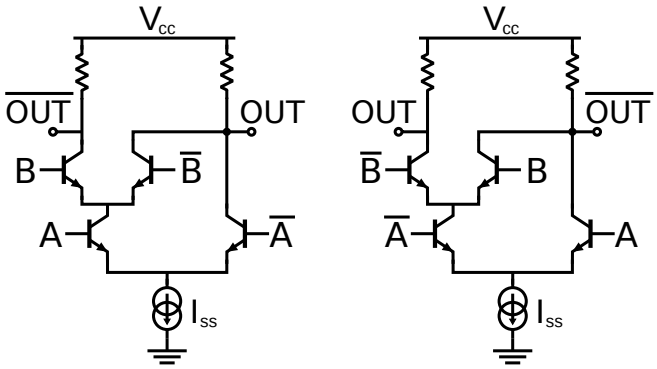
Figure 5.20: Encoder with D-latches

To delay the data correctly, it is important that it arrives before the triggering clock edge, which can be both the rising or falling edge. If this is not the case, the latch becomes transparent and no delay, other than the D-latch propagation delay, is introduced.

5.7 Circuits

Where the previous section focused on the logic level of the implementation, this section describes the circuit implementation of the different logic building blocks. Current mode logic (CML) is preferred as implementation because of its superior performance. Even though CML circuits suffer from a larger static power dissipation than CMOS circuits, they can handle low signal voltages and high operation frequencies [18, 19]. Migration towards emitter coupled logic (ECL) is possible by adding common collector stages also known as emitter followers. Without loss of speed the extra stage performs level shifting and an impedance transformation towards a lower output impedance.

The bipolar CML gate is based on the emitter coupled pair of npn transistors biased by a constant current source I_{ss} [20]. Typically, these circuits have a differential input and output. Their output swing is characterized by the load resistors and I_{ss}, as total current switching is achieved. By stacking multiple of these pairs AND-, OR- and XOR-gates can easily be obtained. Figure 5.21(a) shows an AND-gate, which can be easily reconfigured into an OR-gate by redistributing the inputs, as is represented in Figure 5.21(b). Of course it is also easy to transform the circuits into NAND-, NOR- and NXOR-gates by changing the positive and negative output, thanks to the differential implementation.
The D-latch is one of the most popular elements of CML and is shown in Figure 5.22. It has a clock (CLK) and a data input and basically performs



(a) CML AND-gate (b) CML OR-gate

Figure 5.21: Example of the simplicity of CML circuit transformation

two functions dependent on the clock signal. In case of rising clock edge triggering, when CLK is high it tracks the input data IN. When it is low the output is kept at the previous value, which is consistent with a hold operation that is performed by a cross-coupled pair. As mentioned before, cascading 2 such latches creates a D-flip-flop in master-slave configuration.

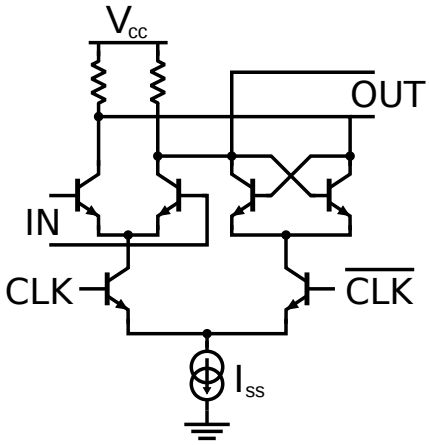


Figure 5.22: Conventional CML D-latch circuit

In Section 5.6.1 an SR-latch was used for the implementation of the pre-coder. This can simply be implemented by 2 cross-coupled NOR-gates as represented in Figure 5.23 [21]. It can be verified that this configuration works appropriate: a high S and low R will set the output Q high (and

$\overline{Q}$ low), a high R and low S will reset Q low and when both inputs are low, feedback will maintain the outputs in constant state. Of course the combination of both S and R high is a forbidden state, due to the inverse relationship between Q and $\overline{Q}$, but in the configuration of Figure 5.17 this state isn't possible.

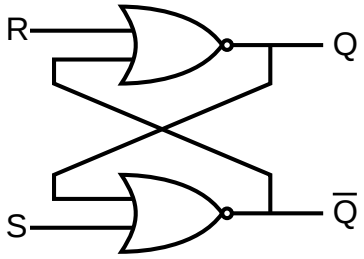


Figure 5.23: SR-latch buildup

The simple circuit that implements the adder necessary in the encoder is shown in Figure 5.24. This consists of 2 current steering blocks that add together the current, which is transformed into a voltage by a regular resistor.

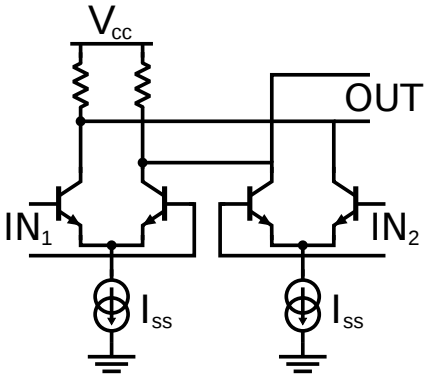


Figure 5.24: CML adder circuit

5.8 Conclusion

From the arguments in this Chapter it is clear that (O)DB has a number of advantages over other modulation schemes. Even though it requires some extra blocks compared with NRZ, these blocks are fairly simple to implement.

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6

Dual channel 28 Gb/s/ch low power optical duobinary EAM driver array

6.1 Introduction

In the C3PO-project 2-channel 28 Gb/s per channel TX arrays were realized for inter-data center communication. It was opted to introduce optical duobinary as a modulation scheme to soften the constraints on the TX bandwidth and to reduce WDM channel spacing with relaxed dispersion tolerance. A bandwidth of $\sim$14 GHz suffices to reach 28 Gb/s with ODB. Normally MZMs are employed for ODB generation, but due to the difficulty to decrease their form factor [1], the Michelson configuration with REAMs was chosen. Additionally, the Michelson arrangement is more suitable for the considered reflective architectures.

In what follows, two generations of 2-channel EAM driver arrays will be discussed. For the second generation the focus will be mainly on the improvements compared to the first generation.

6.2 Specifications

As was the case for the 10-channel 11.3 Gb/s/ch driver array, the principal aim of the design was the integration of multiple EAM drivers into an array. This necessitated the reduction of the power consumption per EAM

driver. The introduction of the ODB modulation scheme calls for the conversion of the conventional NRZ data signal to the three-level duobinary format scheme. The different possible implementations of the precoder and the encoder were examined, keeping in mind the low power requirements. Again the form factor had to be kept low, required by the array design. Even though an array of 4 driver channels was envisioned to reach a total of 100 Gb/s throughput (112 Gb/s including FEC), an array of 2 was designed to reduce prototyping costs for the demonstrator. The target for the desired voltage swing and reverse DC bias was 2.5 V_{pp} and 1.8 V respectively, the same as for the 10-channel EAM driver array. Due to the Michelson configuration both a positive and a negative data output need to be generated, with a pitch of 400 μm between the individual REAMs. As a consequence a differential driver was developed. The employed technology was again the 0.13 μm SiGe BiCMOS process from ST Microelectronics, the same as for the fabrication of the 113 Gb/s EAM driver array.

Parameter	**Unit**	**Min.**	**Typ.**	**Max.**
Operating temperature range	°C	0	25	70
Supply V_{cc2}	V/mA	4.8	6	6.6
Supply V_{cc1}	V/mA		2.5	
Input common-mode voltage	V		2.35	
Single ended input swing	mV_{pp}		300	
Clock common-mode voltage	V		1.5	
Single ended clock swing	mV_{pp}		400	
Output overshoot	%		6	10
3 dB bandwidth	GHz		14	
Driver jitter	ps_{pp}		10	
Single ended output swing	V_{pp}	1.5	2.5	3
Single ended input resistance	Ω		50	
RF return loss	dB		10	
Output edge speed (20%-80%)	ps		17	
Total power consumption/ch	mW	350	550	700
Die area (2 channels)	mm^2		1.2x2.2	

Table 6.1: 2-channel 56 Gb/s EAM driver array chip level design specifications

6.3 Driver array architecture

6.3.1 Duobinary precoding and encoding

As explained in Section 5.2, the three-level duobinary signal can be created in two ways: with an analog Bessel low pass filter (LPF) or with a delay-and-add filter (DAF) [2]. Due to the implementation of an array and the necessity of a DB precoder, the option of an external LPF is beyond consideration. Consequently, a Bessel LPF should be made on-chip, if this option was chosen. To minimize group delay variation across a passband of $\sim$8 GHz, an extremely accurate design is required. Considering layout parasitics, temperature and process variations, the probability of deviations is non-negligible. Therefore a DAF was chosen. Additionally, the DAF gives the possibility to adjust the bit rate as desired, whereas the LPF only gives good results at one particular data rate defined by its 3dB-cutoff frequency.

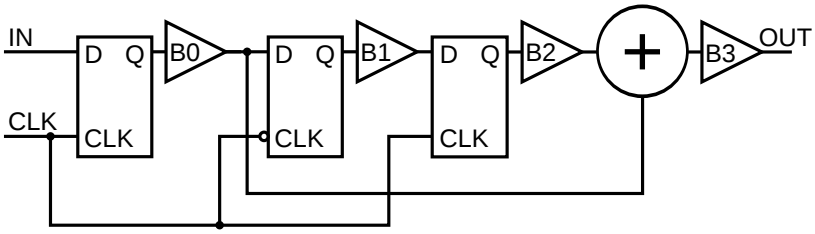


Figure 6.1: Implemented encoder with D-latches and buffers

The designed DB encoder is shown in Figure 6.1. Other than the simple encoder presented in Section 5.6.2, buffer structures were added to improve the signal quality. This is necessary to reduce clock feedthrough to the signal. The adder is also followed by a buffer B3, which is linear not to deform the three-level duobinary signal. Both inputs of the adder need to be synchronized with the clock to ensure an exact delay of one bit period. Because the outputs of the latches are synchronized, the encoder is preceded by a D-latch and a buffer B0. Not including B0 would cause an additional delay between the inputs of the adder, making the delay different from one bit period. To shape the signal the DAF encoder is generally followed by a LPF at half the bit rate. This LPF wasn't actually integrated, but its functionality is achieved by the limited bandwidth of the driver stage.

The precoder implementation is shown in Figure 6.2, which is practically the same as the T-flip-flop implementation of Section 5.6.1 apart from the extra buffer at the end. This was again added to ensure good signal quality. Figure 6.3 shows the implementation of the first AND-gate, which was

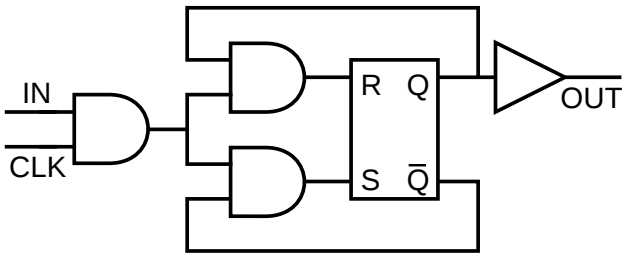


Figure 6.2: Implemented precoder as a T-flip-flop

altered from the classic design to minimize clock feedthrough. All stages have a differential output of 600 mV_{pp}. Typically, emitter followers are used between stages to perform level shifting.

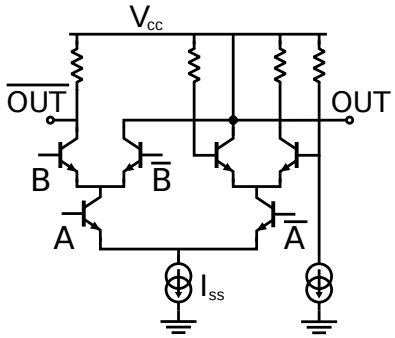


Figure 6.3: Implementation of the first AND-gate

6.3.2 Top level architecture

Figure 6.4 depicts the top level block diagram of the driver IC. The data input and clock input are both differentially matched to 100 Ω. First the NRZ data signal is converted by the aforementioned duobinary precoder and encoder. A predriver block amplifies the input signal and drives the large capacitive input of the current steering driver stage. The predriver is directly followed by the driver stage, which has a configurable modulation current and two configurable bias currents for both positive and negative outputs. Common mode feedback (CMFB) is used between the driver and the predriver, to keep the common mode level of the predriver constant at the optimal level.

The modulation and bias currents can be programmed through SPI with a

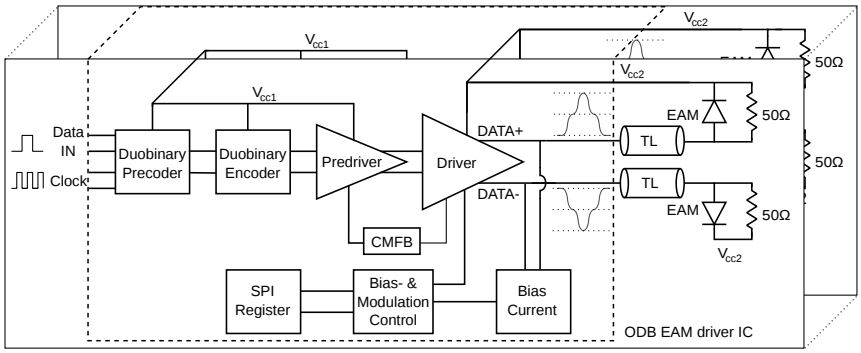


Figure 6.4: IC top level block diagram

4-bit resolution respectively. This can be done for each channel individually. The bias current can be set individually with an accuracy of less than 30 mV, to optimize the EAM operation points according to the transmitted wavelength. For testing purposes both channels can be powered down independently by nullifying all tail currents.

To reduce the power consumption, several techniques were implemented in the driver array. First of all, different supply voltages were used to operate the different circuits with minimum headroom. A standard low supply voltage of 2.5 V (V_{cc1} in Figure 6.4) was fed to the precoder and encoder, the predriver and all other building blocks outside the data path, whereas the driver stage can be supplied from 4.5 V up to 6 V (V_{cc2} in Figure 6.4).

6.4 Predriver stage

The predriver amplifies the duobinary input signal to a level of typically 600 mV_{pp} differentially and is followed by two buffers. The output swing needs to be quite high as the current steering driver stage is degenerated. The circuit is shown in Figure 6.5 and consists of a differential pair followed by a pair of emitter followers. Emitter degeneration (R_1, R_1') was used to make the predriver linear. This is necessary because of the 3-level duobinary signal, to ensure the crosspoints of the upper and lower eyes lie in the middle of the adjacent levels.

The emitter followers serve as level shifters and impedance transformers. The duobinary signal makes it difficult to employ the advanced push-pull operation indicated in Section 4.5. Instead, the current sources of the followers were implemented in a cascode configuration with the two gates

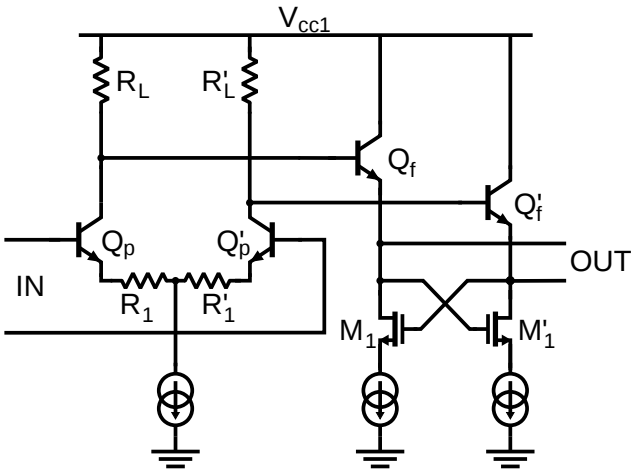


Figure 6.5: Predriver circuit of the 28 Gb/s duobinary driver

cross coupled for peaking. FETs were used to keep the bipolar devices of the current sources out of saturation. The followers have a relatively large collector current of over 7 mA each, which is necessary to provide a satisfactory low drive impedance of below 10 Ω.

The followers were designed with extreme care. The simplified small signal circuit model is portrayed in Figure 6.6(a) in which the base-collector capacitance and the Early effect are neglected and R_L is the load resistance of the predriver. The output impedance of this equivalent circuit was calculated to be

$$Z_{out} = \frac{r_\pi C_\pi R_L s + r_\pi + R_L}{r_\pi C_\pi s + \beta + 1} \tag{6.1}$$

where r_π and C_π are the base-emitter resistance and capacitance respectively and β is the common emitter current gain. The output impedance displays an inductive component as it increases with frequency from $(r_\pi + R_L)/(\beta + 1)$ at s = 0, to R_L at s = ∞. It is possible to construct an equivalent circuit from Equation 6.1, which is shown in Figure 6.6(b) [3]. The inductance and resistances formulas are given in Equation 6.2. The inductive nature of the output impedance in combination with the large capacitive input of the driver may yield considerable ringing, which would be devastating to the 3-level signal. To reduce the ringing, R_L was chosen relatively small at a value of 80 Ω.

$$
\begin{aligned}
L_1 &= \frac{r_\pi C_\pi(\beta R_L - r_\pi)}{(\beta+1)^2} \\
&\approx \frac{C_\pi}{g_m}(R_L - \frac{1}{g_m}) \\
R_1 &= \frac{r_\pi + R_L}{\beta+1} \\
R_2 &= \frac{\beta R_L - r_\pi}{\beta+1}
\end{aligned} \tag{6.2}
$$

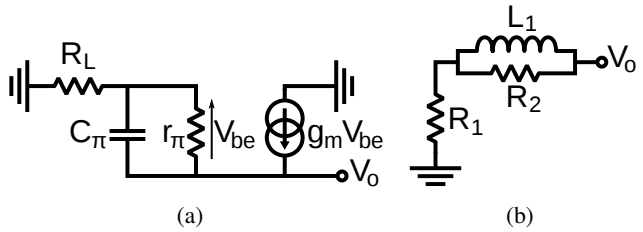


Figure 6.6: Emitter follower: (a) small signal circuit, (b) the equivalent output impedance model

6.5 Current steering driver stage

6.5.1 Model of the EAM combined with the interconnect

As was the case for the 10-channel 11.3 Gb/s per channel driver array, the EAM capacitance was again estimated, this time at a value of 260 fF. The contact resistance was assessed to be 10 Ω. Compared to the relatively simple interconnect of the 11.3 Gb/s driver array no 3D model was developed for the 28 Gb/s drivers. The first interconnect models were intricate with a daughterboard, containing the EAM array, that was flip chipped onto a motherboard. This not only gave a number of uncertainties, e.g. the solder thickness, but also inaccurate results regarding the transmission line at 28 Gb/s. As a result only the bondwire was modeled as a simple inductor of 0.5 nH. This simplification appeared to be a worst case assumption, as the transmission line of the 11.3 Gb/s model seemed to improve the signal quality.

6.5.2 Design of the driver stage

The current steering driver stage consists of a differential pair in a cascode configuration, as shown in Figure 6.7. The cascode not only reduces the capacitive loading of the predriver output, as the cascode input doesn't suffer from Miller multiplication, it also reduces the driver output capacitance. Series peaking L was introduced to increase the output bandwidth [4]. Additionally, emitter degeneration (R_1, R_1') was again used because of the duobinary signal and small negative capacitances were also added by employing two cross-coupled capacitors (C, C'), to further decrease the input capacitance. In analogy with the 11.3 Gb/s driver, the back termination resistors R_{BT} were chosen to be 250 Ω and the emitter's current density was set to 0.8 mA per μm of the emitter length.

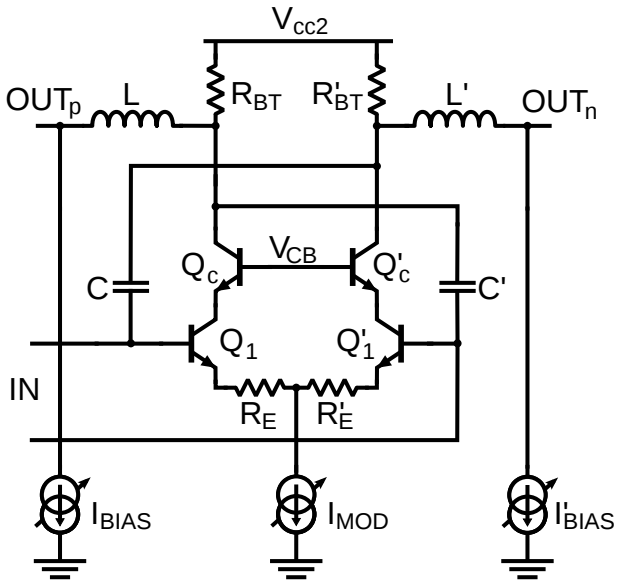


Figure 6.7: Driver output circuit

The V_{CE} of the differential pair was maximized. Since the collector voltage of Q_1 is set by the base voltage of the common base V_{CB}, the emitter voltage of Q_1 has to be set as low as possible to realize maximum V_{CE}. This was done by CMFB, in which a simple transconductor transforms the difference between the emitter voltage and a reference voltage into 2 equal currents. These are added to the load resistances of the predriver (R_L) to lower this stage CM output level [5]. Considering a large loop gain, the emitter voltage will be equal to the reference voltage of 350 mV. CMFB

was used, because it is insufficient to set the output of the predriver to a predefined CM level. This is due to the temperature dependence of V_{BE}, both in the emitter followers of the predriver and in the differential pair of the driver stage.

6.6 Realization of the dual channel 28 Gb/s/ch EAM driver array

The measures taken to test the 2 channel 28 Gb/s per channel driver array will be discussed next. Both the layout and pinout of the chip and the printed circuit boards (PCB) for testing will be examined in more detail.

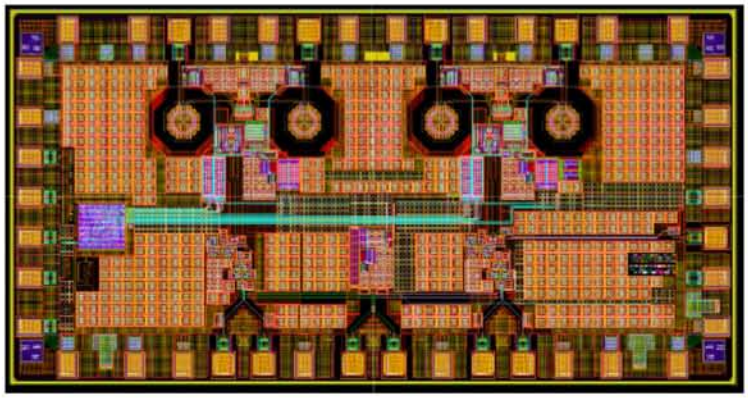
6.6.1 Chip layout and pinout

Figure 6.16(a) shows a screenshot of the chip layout, while Figure 6.16(b) shows a micrograph of the manufactured die, which measures 2.2 mm by 1.2 mm. The 2 channels can be distinguished and the 4 inductors are clearly visible. Again the dimensions are mostly determined by the 400 μm pitch between the EAMs and the number of I/O pads. The on-chip decoupling capacitance is 1.2 nF for each supply.

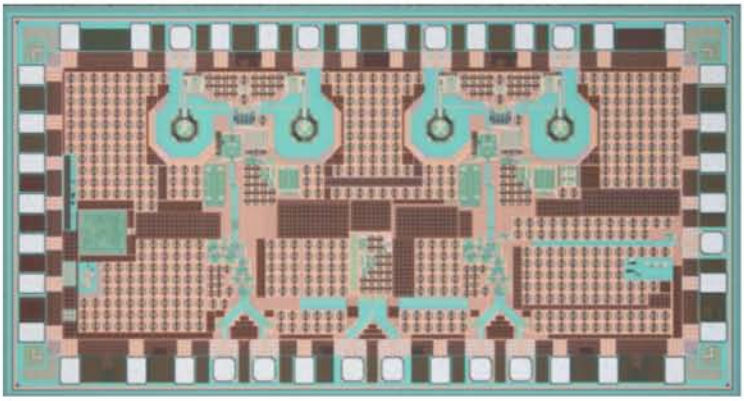
The precise pinout and the bonding of the chip are depicted in Figure 6.9. Due to PCB manufacturing restrictions it was necessary to have a spacing of about 400 μm between the bondpads of the input and signal lines (lower side of the figure). This gives rise to longer wirebonds than anticipated, but this does not affect the driver performance. The decoupling capacitors are placed as close as possible to the chip to minimize the effect of parasitic inductance between the IC and the capacitors.

6.6.2 Prototyping of the 2-channel 28 Gb/s/ch EAM driver array

Because the REAM array was not fabricated yet at the time of testing, the first generation driver array is only tested electrically, with an oscilloscope at the output. The test board incorporates 100 Ω differential grounded coplanar waveguide (GCPW) transmission lines for the inputs and also 50 Ω single ended GCPW transmission lines for the outputs. The outputs are single ended as the output pads are spaced 400 μm apart with supply pads in between, due to the EAM pitch. The board is shown before and after assembly in Figure 6.10(a) and Figure 6.10(b) respectively. As was the case for the 10-channel EAM driver array, the power supplies, SPI-signals



(a)



(b)

Figure 6.8: 2-channel EAM driver array: (a) layout and (b) micrograph

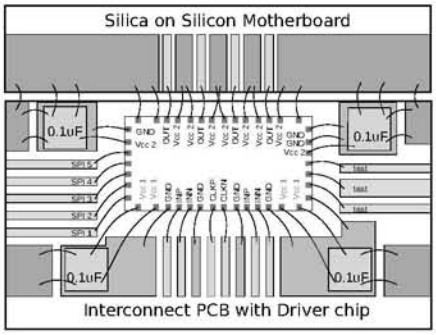
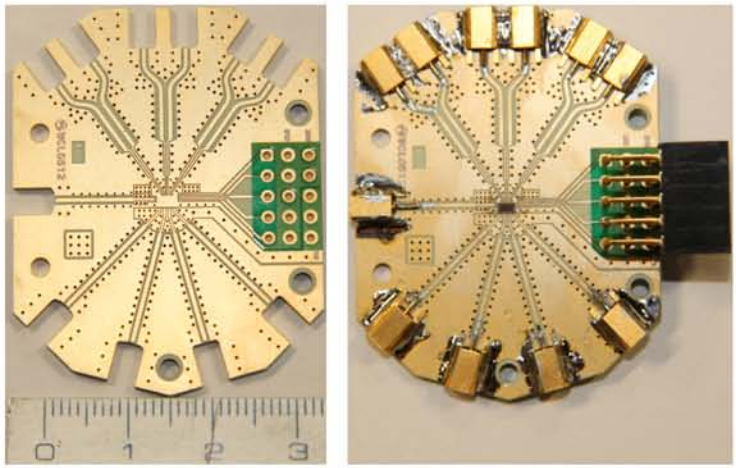


Figure 6.9: Pinout of the 2-channel EAM driver array with decoupling

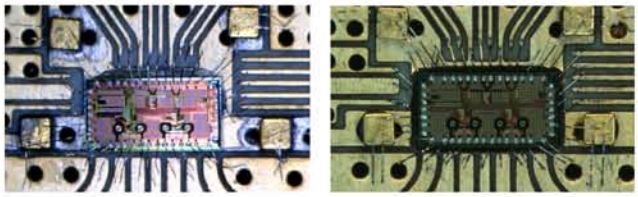
and necessary external resistor are provided by an extra board that can be connected to the test board.

Figure 6.11(a) shows the die bonded to the PCB. Again relatively long bondwires are used. To counter this a board was fabricated with a cavity, in which the die was placed. The cavity ensures proper height alignment of the traces and the I/O pads, which reduces the bondwire length, as shown in Figure 6.11(b). However, the reduction in bondwire length didn't improve the results, showing that the driver performance is robust against this variation.



(a) (b)

Figure 6.10: 2-channel EAM driver array test board: (a) before assembly and (b) after assembly

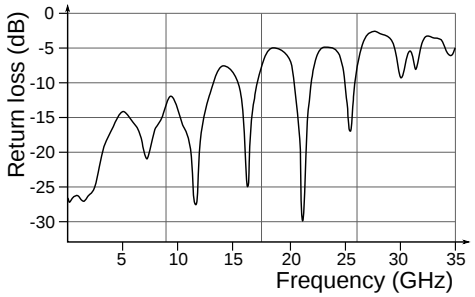


(a) (b)

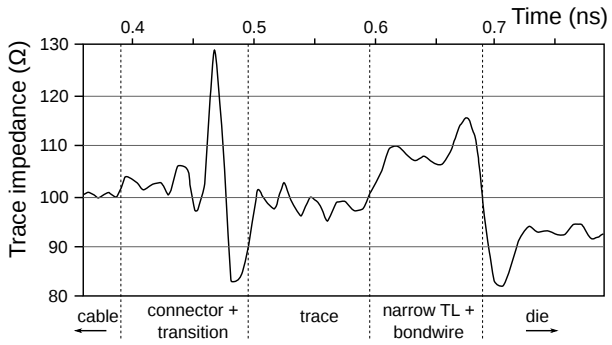
Figure 6.11: (a) The bonded die of the 2-channel EAM driver array, (b) bonded die inside a cavity with shorter bondwires

The return loss S11 of the 100 Ω differential input transmission lines was

measured up to 67 GHz with a 4-port Agilent PNA-X. The results in Figure 6.12(a) show an S11 of less than -10 dB up to ∼13 GHz and less than -7 up to ∼18 GHz. The return loss stays below -5 dB up to ∼26 GHz. The mismatch at higher frequencies is the result of the connector interface. After testing the boards, it was discovered that the mini-SMP connectors only give appropriate matching results up to ∼25 GHz, even though they specified a return loss of less than -14 dB up to 65 GHz [6]. The main reason is the connector footprint and the soldering. For higher frequencies screw-on 2.4 mm or 1.85 mm connectors should be used. However, the reduced matching did have little effect on the performance.



(a)



(b)

Figure 6.12: Differential input transmission line measurement with a bonded die: (a) S11 (b) TDR

Mentor Graphics' HyperLynx was used to convert the data into a time domain reflectometry (TDR) response. Figure 6.12(b) shows the different parts of the connection and their characteristic impedance. The 3 small bumps followed by a peak and a dip indicate the mini-SMP connector. The first part of the trace is matched correctly, while closer to the die the nar-

row trace and the bondwire result in a rise of the characteristic impedance. At the beginning of the die there is a dip caused by the capacitive I/O pads. The die's input impedance seems to be quite close to 100 Ω, indicating little IC process variation.

6.7 Experimental test results

6.7.1 Validation of the test setup

The measurement setup for the electrical tests is shown in Figure 6.13. At the input a 4:1 multiplexer is used to generate a 25 Gb/s NRZ signal. The multiplexer uses a clock signal at half the bit rate (12.5 GHz), while the duobinary coding blocks need a clock of the full bit rate (25 GHz). Consequently a clock doubler was used, followed by a ratrace coupler to transform the single-ended clock into a differential signal. As was the case for the 10-channel driver array testing, the operating conditions of driving an EAM were emulated by a bias-tee and a 20-dB attenuator was added to avoid overloading the oscilloscope. In this measurement the output was measured differentially, but for simplicity a single ended output structure is shown in Figure 6.13.

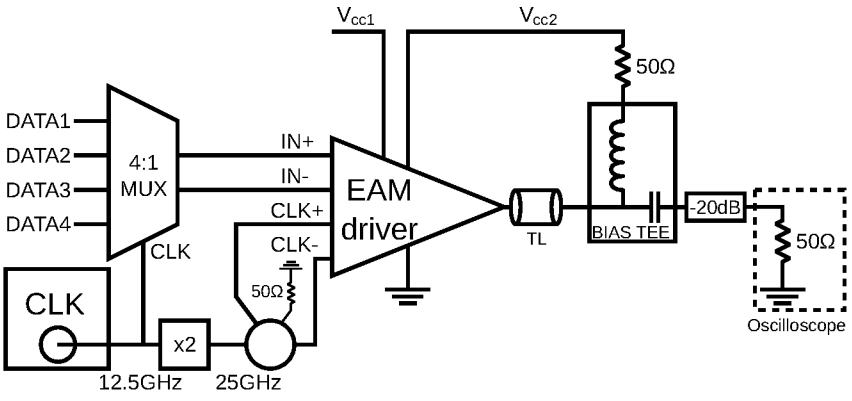
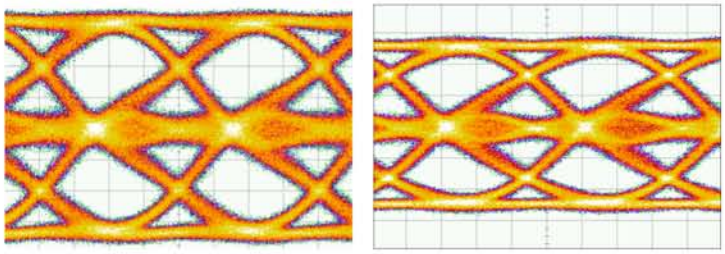


Figure 6.13: Experimental setup for the electrical testing with single ended output

6.7.2 Electrical experiments

The electrical duobinary eye diagram of one channel is shown in Figure 6.14(a), measured at a data rate of 25 Gb/s by multiplexing four 2^{31}-1 PRBS signals. Only 1 channel output is shown since both channels gave very similar results. With a supply of 5.6 V, a differential swing of 4.2 V_{pp} was reached, while both outputs were biased by the driver at a voltage of 1.5 V below Vcc2. The power consumption of the duobinary coding block was measured to be 186 mW/ch, while the driver consumption was only 485 mW/ch of which 90 mW was consumed externally in the 50 Ω resistors. Per channel this gives a power consumption of only 671 mW or a total of less than 1.35 W for the entire 50 Gb/s transmitter.



(a) (b)

Figure 6.14: Output signal at 25 Gb/s with a 4.2 V_{pp} differential output (a) and a 3 V_{pp} differential output (b) (2^{31}-1 PRBS, 0.6 V/div, 10 ps/div)

A smaller differential swing of 3 V_{pp}, is shown in Figure 6.14(b), with both outputs biased at 1.05 V. Due to the smaller swing, the corresponding modulation current is lower and the supply voltage can be reduced to 4.5 V, resulting in a reduction of the driver power consumption to 306 mW/ch excluding the 186 mW for the duobinary coding.

6.8 Second generation 2-channel 28 Gb/s/ch EAM driver array

While the first generation gave adequate results, its output swing could be improved and the power consumption could still be reduced. As a result, a second generation 2-channel EAM driver array was fabricated. Because of the acceptable performance of the first generation, no major changes were made. Again a 0.13 μm SiGe BiCMOS process from ST Microelectronics was used. However, it was a more advanced version of the technology

utilized in the first generation. In what follows the main differences with the first generation will be discussed.

6.8.1 Architecture changes

The second generation's blocks are the same as the first generation, with the exception of the CMFB block that was omitted to save power consumption. Instead a configurable current source was added to be able to change the predriver's output CM level via the SPI control. Similar to the previous generation, the duobinary driver also consists of a duobinary precoder and encoder, a predriver and a current steering driver stage. Also present are a bias current source and an SPI register to control the bias and modulation current settings. Even though the blocks are the same, the implementation of the precoder was adjusted to reduce its power consumption. The concept is still a divide-by-2 counter, but this time it was implemented as a frequency divider instead of a T-flip-flop. This reduces the power consumption of the coding blocks from 186 mW to 127 mW, which is almost a reduction of a third. The predriver was altered in a way such that its linearity can be controlled. The same techniques that are applied in the previous version are again used. Through the experience gained with the first version design and testing, the power consumption of the different blocks was optimized.

6.8.2 Circuit changes

The main changes were made to the current steering driver stage. The first generation didn't obtain full current switching, limiting the output swing. This was caused by the degeneration resistor (R_E in Figure 6.7), that was too large. The excess of resistance can be explained by temperature effects and parasitics. Process variations can also be a reason, but this is unlikely as the measured input and output resistors were smaller than the designed values (cfr. Section 6.6.2). To resolve the issue the degeneration resistance was reduced from 2.5 Ω to 1.1 Ω. Moreover, the degeneration was implemented differently. The modulation current source was split into 2 sources and the degeneration resistor was placed in between, as shown in Figure 6.15. In this way the headroom of the current sources was increased.

Additionally, the bias current source was connected to the emitters of the cascode transistors to reduce the capacitance at the output and to soften the constraints on the current source's output impedance. Also the inductor at the output, present in the first generation, could be omitted, thanks to the new technology and the different implementation of the bias current source.

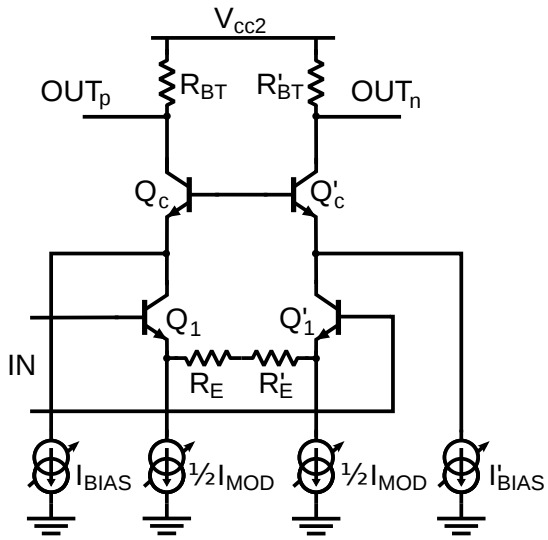


Figure 6.15: Second generation driver circuit

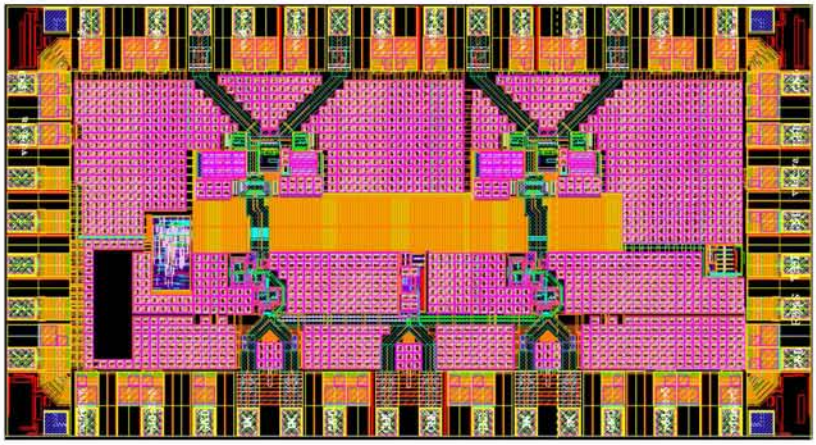
Only some small adjustments were made to the other circuits. The most important adjustment was made to the predriver's degeneration resistor, which was made configurable.

6.9 Realization of the second generation 2-channel 28 Gb/s/ch EAM driver array

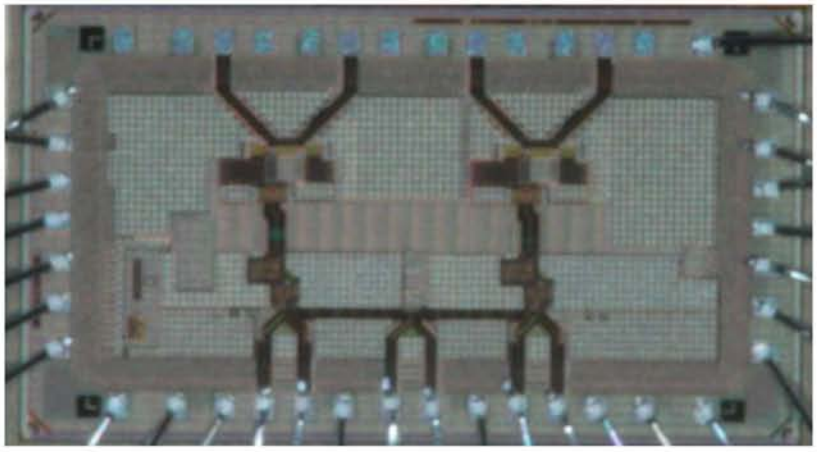
6.9.1 Chip layout and pinout

The die dimensions and the pinout have remained the same as the first generation, as a result the same test PCB's could be used. Also the test setup hasn't changed. The chip layout and a die micrograph are represented in Figure 6.16(a) and Figure 6.16(b) respectively.

Figure 6.17 represents a 3D view of the chip layout without the I/O pads. A more detailed representation of a single channel can be seen in Figure 6.18, which shows the different blocks. Figure 6.19 on the other hand shows the last stages from up close.



(a)



(b)

Figure 6.16: Second generation 2-channel driver array: (a) layout and (b) micrograph

6.10 Second generation experimental test results

The electrical and optical evaluation of the second generation 2-channel 28 Gb/s per channel EAM driver array will be discussed next. Results obtained electrically with the oscilloscope as load and with a commercial MZM will be examined.

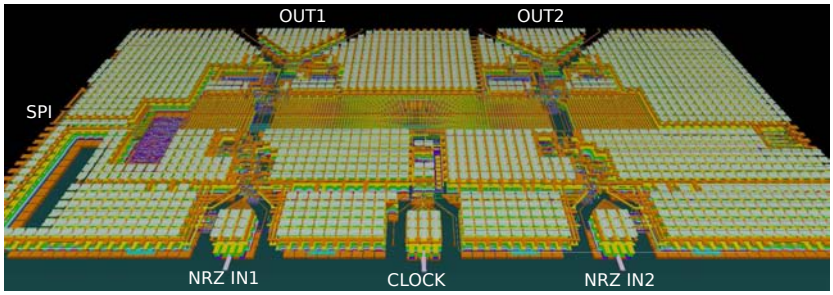


Figure 6.17: 3D view of the chip layout

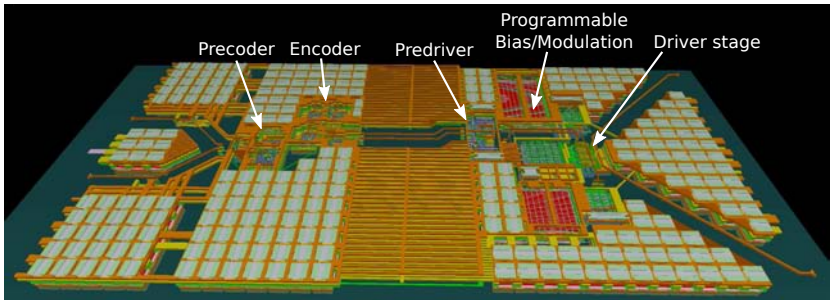


Figure 6.18: Detailed layout of a single channel

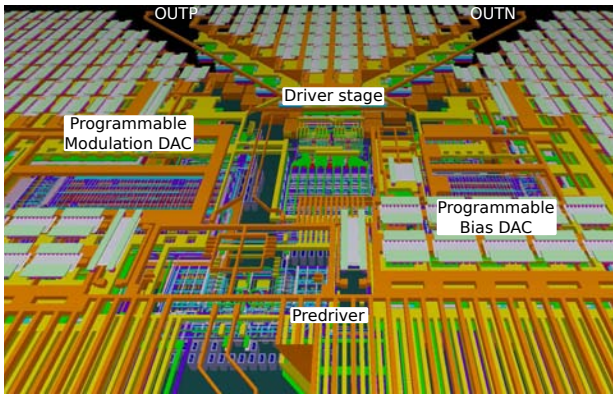


Figure 6.19: Detailed layout of the last stages

6.10.1 Electrical experiments

The duobinary eye diagram of Figure 6.20 shows more symmetry compared to the first generation and this at a data rate of 28 Gb/s. With a supply of 6.6 V, a differential swing of 6 V_{pp} was reached, corresponding to a gain

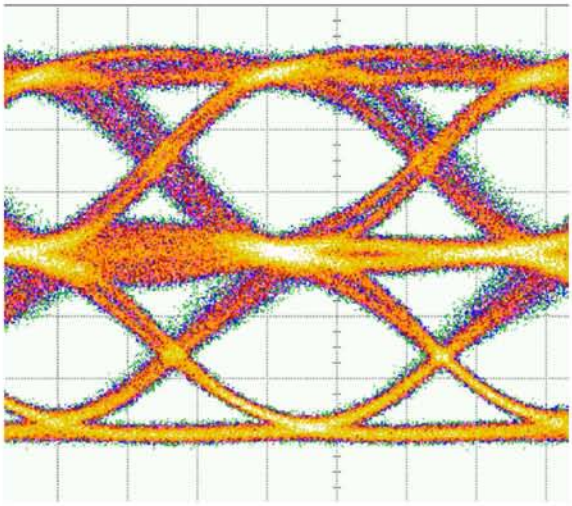
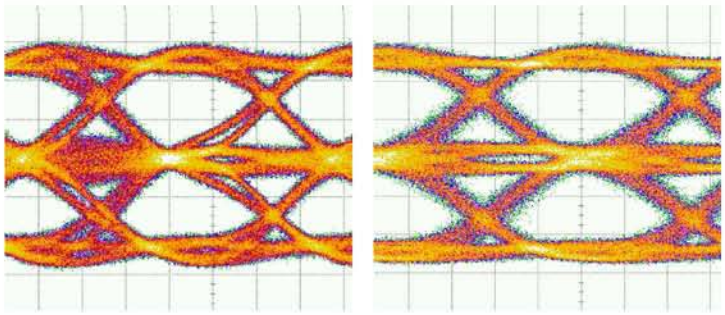


Figure 6.20: Output signal at 28 Gb/s with 6 V_{pp} differentially (2^{31}-1 PRBS, 1 V/div, 10 ps/div)

of 20 dB since the driver input is 600 mV_{pp} differentially. Both outputs were biased by the driver at a voltage of 1.5 V below V_{cc2}. The power consumption of the duobinary coding block was measured to be 127 mW/ch, while the driver consumption was only 525 mW/ch of which 90 mW was consumed externally in the 50 Ω resistors. Per channel this gives a power consumption of only 652 mW or a total of just over 1.3 W for the entire 56 Gb/s transmitter.

A smaller differential swing of 3 V_{pp}, is shown in Figure 6.21(a). Thanks to the smaller swing, the corresponding modulation current is lower and the supply voltage can be reduced to 4.8 V. This results in a reduction of the driver power consumption to 198 mW/ch excluding the 127 mW for the duobinary coding.

Because a DAF was used, the transmission speed can go as low as 21 Gb/s, as is shown in Figure 6.21(b). For lower speeds the delay of the precoder becomes too small with respect to the bit period. This causes the first D-latch to be transparent at the moment the data arrives. In other words, the data transmission comes just before the falling clock edge (assuming the rising clock edge is the triggering edge), which introduces a direct transmission of the output. As an effect the clock and data are not synchronized, leading to incorrect encoding. Adding an extra D-latch to the cascade could resolve this problem, but would increase the power consumption.



(a) (b)

Figure 6.21: Output signal with a 3 V_{pp} differential output at 28 Gb/s (a) and at 21 Gb/s (b)(2^{31}-1 PRBS, 0.6 V/div, 10 ps/div)

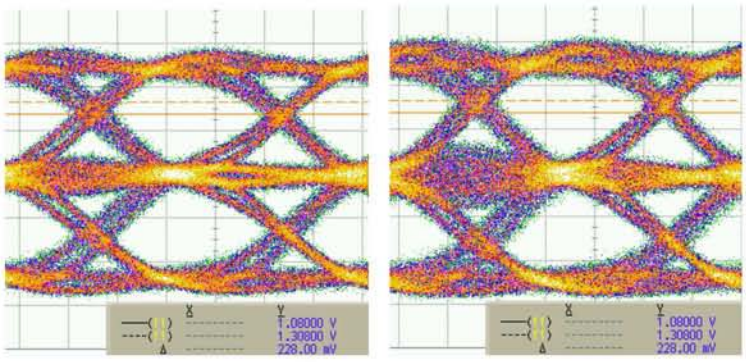


Figure 6.22: Crosspoint difference for an output of 4 V_{pp} at 28 Gb/s (0.8 V/div, 10 ps/div)

As mentioned earlier the linearity of the predriver can be controlled. For an output voltage of 4 V_{pp} this can make the crosspoint shift with 228 mV, which is more than 11%, as indicated in Figure 6.22. This feature can optimize the receiver sensitivity for optical duobinary according to the distance that is traversed. For back-to-back and short reach transmission little to no fiber dispersion is introduced, which gives optimal receiver sensitivity when the crosspoint is in the middle of the adjacent levels. For long reach transmission the eye quality and receiver sensitivity could improve when the crosspoint is shifted to the outer levels. Note that the adjustment doesn't work for output swings larger than 5 V_{pp}, as the predriver output needs to be maximal to have full current switching in the driver stage. To achieve this the predriver needs a minimal degeneration.

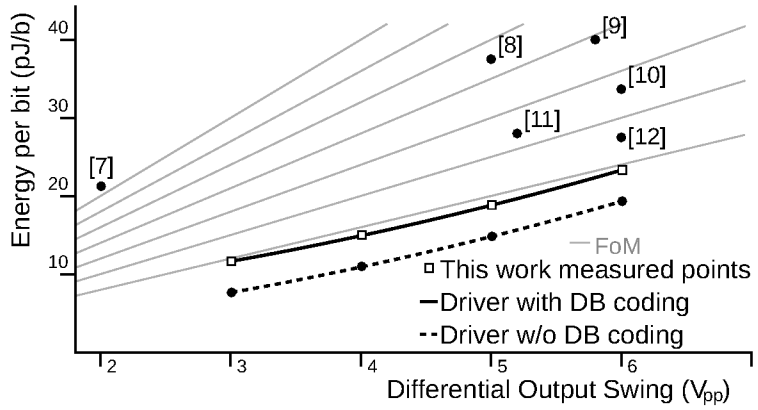


Figure 6.23: Energy per bit and output swing comparison

Reference	FoM (pJ/(b V_{pp}))	Freq. (Gb/s)	Power (W)	Output swing (V_{pp})
[7]	10.62	40	0.85	1
[8]	7.5	40	1.5	5
[9]	6.89	40	1.6	5.8
[10]	5.62	40	1.35	6
[11]	5.38	50	1.4	5.2
[12]	4.58	40	1.1	6
Driver w/ coding	**3.88**	**28**	**0.652**	**6**
Driver w/o coding	**3.13**	**28**	**0.525**	**6**

Table 6.2: Comparison state-of-the-art in low energy consumption

When comparing the power consumption to other papers it is important to keep in mind both bit rate and output swing. To make the comparison clearer, a figure of merit (FoM) is defined. The consumption per bit rate, which is equal to the energy per bit, is divided by the output swing. The resulting FoM and a comparison of the state-of-the-art with low energy consumption is given in Table 6.2.

Figure 6.23 shows a plot of the energy per bit in function of the differential output swing for different modulator driver circuits, together with equal FoM lines. At typical operation (6 V_{pp} output swing) the energy is 23.28 pJ/b, including the duobinary coding blocks consumption, and 18.75 pJ/b without. A plot of the energy per bit in function of the differential output swing for the different modulator driver circuits of Table 6.2 is shown in Figure 6.23.

In Figure 6.23, the black line represents the measured consumption of the complete modulator driver, including the duobinary precoder and encoder. The lower dotted black line only considers the driver (without DB coding), as this gives a better comparison with other papers, where NRZ is utilized and therefore no coding blocks are present. As the most desirable region is at the bottom right (high swing and low energy per bit), it is clear that this work gives the best performance, both with and without the coding blocks. The performance of [12] is the closest to this work, however, the used distributed amplifier with a single ended output occupies a total area of 6.7 mm^2, which is almost 4 times larger than the proposed array and thus far too large to be incorporated into an array.

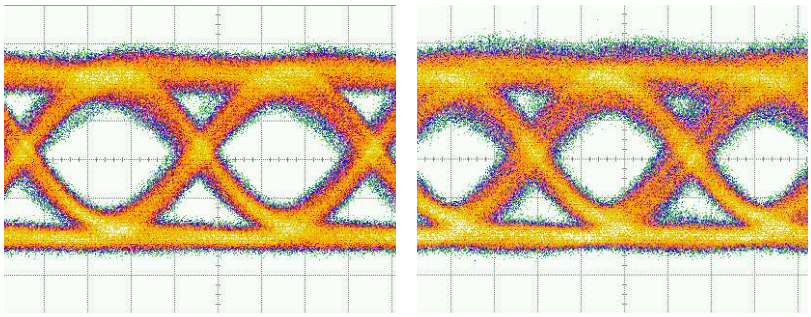
It should be noted that only modulator drivers with an energy per bit lower than 40 pJ/b are listed and that some papers reported the power consumption excluding the dissipation in the external load. Furthermore, not all designs did have a differential output, but their single ended swing was doubled in the figure to make this comparison possible. With [12] this is not done, as this is a distributed amplifier making the output differential is only possible by doubling the circuit, and thus the consumption. Note that except for this work no drivers at speeds lower than 40 Gb/s were included in this plot, as the energy per bit becomes too high at lower data rates. Moreover, only [10] and this work make use of SiGe BiCMOS, while the others utilise more expensive GaAs and InP technologies.

6.10.2 Optical experiments using a commercial component

Figure 6.24(a) and 6.24(b) show the measured optical eye diagram at a data rate of 25 Gb/s and 28 Gb/s respectively, using the Fujitsu FTM7937EZ 40 Gb/s MZM. An extinction ratio of over 10 dB was measured with a 2^{31}-1 PRBS sequence. A bit-error rate (BER) test was performed at both speeds with a commercial Sumitomo receiver and showed error free transmission, indicating the DB pre- and encoder work accordingly.

6.11 Conclusion

Both generation modulator driver arrays revealed excellent signal quality, while including duobinary coding. To the best of our knowledge, the proposed ICs are the fastest modulator driver chips including on-chip duobinary coding, reported so far. Next to that they achieve an improved power consumption in comparison with the state-of-the-art in energy consumption.



(a) (b)

Figure 6.24: Optically eye diagram (2^{31}-1 PRBS, 10 ps/div).: (a) at 25 Gb/s and (b) at 28 Gb/s

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7 Conclusion

7.1 Summary of the results

The main focus of the research described in this dissertation lies on the realization of 2 types of EAM driver arrays with record low power consumption. A 10-channel 11.3 Gb/s per channel EAM modulator driver array was designed to be employed both in metro and access networks, while a 2-channel 28 Gb/s per channel EAM driver array was developed for inter-data center communication with duobinary modulation. The research was performed under the framework of the FP7 project C3PO, which aimed to develop new colourless and coolerless technologies, whilst enabling bandwidth growth and constraining cost. The EAM driver integration into arrays requires a reduced driver power dissipation, which omits the need for power hungry thermo-electric coolers. Consequently costs are lowered and the WDM-PON access architecture benefits from the integrated driver development. The necessity of greener network electronics due to the immense power consumption of the global network that makes up the internet is illustrated in Chapter 1.

Electroabsorption modulators appear to be the best candidate for the applications considered in this thesis. This is apparent from Chapter 2, which gives a brief overview of different optical transmitters. Thanks to the low chirp, high speed and high signal quality, external modulation is the best choice for the transmission over tens of kilometers at line rates beyond 10

Gb/s. Furthermore, the EAM attributes lower drive voltage and smaller form factor, compared to MZMs. These two advantages are crucial to achieve a low power consumption and array integration respectively. Moreover, the use of new reflective EAMs together with SOAs realizes the colourless approach pursued in C3PO.

In Chapter 3 the driver topologies were examined. Considering the power consumption, 4 different output configurations were compared. Different techniques in reducing power consumption were analyzed and weighed. Also a driver stage with an active back termination was discussed in short. As a result of the comparison, a current steering driver with a single ended DC-coupled output was chosen as the best solution, taking into consideration bandwidth, signal quality and potential design risk.

The realization of a 10-channel 113 Gb/s (including FEC overheads) EAM driver array was reported in Chapter 4. A single channel power consumption of 219 mW was measured at a throughput of 11.3 Gb/s for an output swing of 2.5 V_{pp}. The jitter was measured to be 18.3 ps_{pp} and 2.45 ps_{rms}. To the best of the author's knowledge such EAM driver arrays are not currently available on the open market, nor published in the literature. This is the first 10-channel 113 Gb/s EAM driver array and the lowest power consumption for an EAM driver so far reported, 50% below the state of the art in power consumption.

Subsequently, the 10-channel EAM driver array was integrated into a multi-channel TX PIC together with the newly designed REAM array. Even though 3 channels were damaged during packaging, the remaining 7 channels showed good B2B performance with clearly open eye diagrams. Less than 2 dB difference in RX sensitivity between 7 channels was measured for error-free operation at ERs ranging from 7.6 dB to 9.8 dB. Multi-channel operation showed little crosstalk, with a RX sensitivity penalty of less than 1 dB. Also a RX sensitivity penalty of approximately 1 dB was observed after transmission over 80 km of SMF. Furthermore, error-free performance was maintained for distances up to 96 km for both the single- and multi-channel cases. The research into this 10-channel EAM driver array resulted in several journal papers [1–3].

Chapter 5 described the advantages and generation of the duobinary modulation scheme. Two generations of a 2-channel duobinary EAM driver array at 25 and 28 Gb/s per channel were reported in Chapter 6. Since two REAMs had to be driven in push-pull, required by the duobinary approach, each driver had a differential DC-coupled output. The first generation gave acceptable results with a driver dissipation of 485 mW per channel for a 4.2

V_{pp} differential output at 25 Gb/s and a power consumption of 186 mW for the duobinary coding. A second generation 2-channel 56 Gb/s EAM driver array provided a greater output swing. With a differential swing of 6 V_{pp} a power consumption of 525 mW was achieved at 28 Gb/s, while the duobinary coding only consumed 127 mW. Moreover, the achieved eye diagram showed more symmetry compared to the results of the first generation. To the best of the author's knowledge, the proposed IC is the fastest modulator driver including on-chip duobinary coding reported so far. It also demonstrates array integration and state-of-the-art power consumption. This work resulted in publications [4, 5].

Both driver array designs showed excellent performance at low power consumption. The ultra low dissipation of the 10-channel 113 Gb/s EAM driver array shows potential to operate the transmitter without TEC, even though the power consumption induced temperature rise has an effect on the REAM performance, a simple heatsink would alleviate this problem. Also the 2-channel 56 Gb/s EAM driver array would work fine without a TEC.

7.2 Further research

To ultimately minimize the power consumption of the modulator driver a number of optimizations can be performed. The main possibilities of further reductions were discussed in Chapter 3. Even though most techniques were employed in the discussed designs, they can be pushed even further, eventually in a trade-off with the signal quality.

The active back termination design should be examined in more detail and different approaches of this design need to be fabricated and tested. The low output impedance of this type of driver could give astonishing low power consumption, achieving the required bandwidth, resulting in excellent signal quality.

Extremely close integration of the EAMs and the drivers could omit the need for an off-chip parallel 50 Ω. This provides the opportunity to optimize the total load resistance with respect to power and bandwidth.

Next to the optimization of the driver, further research in photonic modulators now allows to operate modulators with lower drive voltage. As stated in Chapter 3, a reduction in desired voltage swing will have the most influence on the power consumption. In this respect Mach-Zehnder devices have achieved lower drive voltages, such as 0.63 V_{pp} at 20 Gb/s [6] and 0.5 V_{pp} at 26 Gb/s [7], while EAMs have been developed at drive voltages as low as

0.5 V_{pp} at 13 GHz bandwidth [8] and even 0.2 V_{pp} at 25 Gb/s [9]. Of course these devices suffered from high insertion losses and/or low ERs and should be examined further from a system and circuit perspective. However, it is clear that a lot of research effort is devoted to design more efficient modulators, requiring appropriate driver chips to benefit better telecom systems.

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