Karakterisering van elektrostatische ontladingsgolfvormen op chip
met sub-nanoseconderesolutie:
ontwerp van een differentiële hoogspanningsprobe met hoge bandbreedte

Characterisation of On-Chip Electrostatic Discharge Waveforms
with Sub-Nanosecond Resolution:
Design of a Differential High Voltage Probe with High Bandwidth

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Dankwoord

Een doctoraat is veel meer dan vier jaar doctoraal onderzoek. Het is een logische verderzetting van de leercurve die je sinds geboorte doormaakt, en is terzelfdertijd ook een engagement om die leercurve in de toekomst verder te zetten. Zo'n evolutie is enkel maar mogelijk dankzij goede begeleiding. Ik wil dan ook iedereen bedanken die mij sinds geboorte, hetzij op wetenschappelijk, hetzij op persoonlijk vlak, mee heeft helpen vormen. Uit deze groep mensen zijn er een paar aan wie ik hier expliciet mijn dankbaarheid wens uit te drukken.

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Lembeke, 26 maart 2012

Guus Colman

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Glossary

A

AM   Amplitude Modulation

C

CBM   Charged Body Model
CDM   Charged Device Model
CMRR   Common-Mode Rejection Ratio

D

DUT   Device-under-test

E

EM   Electromagnetic
EMC   Electromagnetic Compatibility
EOT   Equivalent Oxide Thickness
ESD   Electrostatic Discharge
ESDS   Electrostatic Discharge Sensitive

F

FC   Fixed Connector

FFT	Fast Fourier Transform
FM	Frequency Modulation
FR4	Flame Retardant 4

G

GSps	Giga-samples per second

H

HBM	Human Body Model
HMM	Human Metal Model

I

IC	Integrated Circuit
IEC	International Electrotechnical Commission
IIP2	Input-referred Second-order Intercept Point
IIP3	Input-referred Third-order Intercept Point
IO	Input-Output
IP2	Second-order Intercept Point
IP3	Third-order Intercept Point

M

MAP	Maximum A Posteriori
ML	Maximum Likelihood
MM	Machine Model
MMSE	Minimum Mean Square Error

N

NF	Noise Figure

O

OIP2   Output-referred Second-order Intercept Point
OIP3   Output-referred Third-order Intercept Point

P

PCB   Printed Circuit Board

R

rms   Root mean square

S

SMA   SubMiniature version A
SNR   Signal-to-Noise Ratio

T

TLP   Transmission Line Pulse

V

VCSEL   Vertical-Cavity Surface-Emitting Laser
VNA   Vector Network Analyzer

Nederlandstalige samenvatting
–Dutch Summary–

Gedurende de laatste decennia is het aantal op chip geïntegreerde ESD-protecties met rasse schreden toegenomen. Dit heeft tot gevolg dat het aantal door ESD veroorzaakte falingen in elektronische schakelingen enorm werd teruggeschroefd. Toch blijft een gestage evolutie in nieuwe en betere ESD-protectietechnieken noodzakelijk om het hoofd te kunnen bieden aan toekomstige ESD-problemen. Een noodzakelijke voorwaarde hiervoor is het remediëren van de nog steeds te beperkte kennis van de werkelijke ESD-problematiek. Een belangrijke stap voorwaarts kan worden gezet door het rechtstreeks opmeten van de elektrische golfvormen aan de ingang van de ESD-protectie. Hierbij moet extra aandacht worden besteed aan de overgangsverschijnselen ten gevolge van het inschakelgedrag van de geïntegreerde ESD-protecties. Aangezien parasitairen in het meetsysteem (bvb. bonddraden,...) de gemeten golfvormen ter hoogte van deze overgangsverschijnselen sterk kunnen beïnvloeden, kan de hoogste nauwkeurigheid enkel verkregen worden door rechtstreekse meting op de ingangspads van de ESD-protectie. Op deze wijze kan het gedrag van het circuit rechtstreeks gelinkt worden aan de gemeten golfvormen. In dit proefschrift wordt een goedkope meettechniek beschreven die door haar lage gevoeligheid aan elektromagnetische interferentie gebruikt kan worden voor de karakterisering van ESD-golfvormen op chip. De verstrekte in situ informatie kan dan ook als leidraad fungeren in de zoektocht naar nieuwe, robuuste elektronische ontwerpen.

Een system-ESD puls bevat informatie in een frequentieband tot 5 GHz en een dynamisch bereik van 35 dB [1]. Zo een puls zou rechtstreeks kunnen worden gedigitaliseerd met behulp van een op de testchip toegevoegde bemonsteringsschakeling. De eisen die aan een dergelijke schakeling gesteld zouden worden, zijn gelijkaardig aan deze van de bemonsteringsschakelingen in de front-end van de commerciële snelle bemonsteringsoscilloscopen. Ook genereert een ESD puls een sterk interfererend elektromagnetisch veld

dat binnen hetzelfde frequentiebereik ligt als de gemeten puls. Dit veld zal de digitaliseringsperformantie gaan begrenzen, bvb. door overspraak en grond- of voedingsstuiter. In plaats van een rechtstreekse bemonsteringstechniek te gebruiken in een door EMC verstoorde omgeving, wordt in dit werk een architectuur die gebaseerd is op 'verdeel en heers' voorgesteld. Hierbij wordt het in situ digitaliseringsprobleem opgedeeld in een transport- en een digitaliseringsprobleem. Hierbij zijn de resulterende problemen van een lagere complexiteit. De meetprobe meet de ESD-golfvorm ter hoogte van het testobject in een door EMC verstoorde omgeving en transporteert het naar een EMC-veilige omgeving. Hier kan het dan door een snel bemonsteringsinstrument, zoals bvb. een oscilloscoop, inferentievrij gedigitaliseerd worden. Er bestaan verschillende manieren om een breedbandig signaal doorheen een EMC-onveilige omgeving te loodsen. In dit werk werd er gekozen voor een optische link, aangezien een dergelijke link inherent immuun is voor elektromagnetische interferentie [2]. Een extra, nuttige eigenschap van een optische link is dat het een galvanische scheiding vormt tussen de ESD-puls en het dure bemonsteringssysteem. De meetprobe bestaat uit een circuit waarin het opgemeten ESD-signaal herschaald wordt tot het zich in het lineaire bereik van de laser bevindt. Hierbij staat de laser in voor de optische modulatie. Tegenwoordig zijn kleine, goedkope, hogesnelheidslasers commercieel beschikbaar. Nadien wordt dit optische signaal gedemoduleerd met behulp van een foto-ontvanger en gedigitaliseerd. Aangezien ESD-pulsen een heel hoog ogenblikkelijk vermogen bezitten, waarvan een heel kleine fractie gebruikt wordt voor laseraansturing, kan een breedbandige verzwakker gebruikt worden om de laser aan te sturen. Die verzwakker zal de ingangsspanning dan omzetten naar een laserstroom. Weerstanden zijn heel lineare, en dus heel voorspelbare componenten. Sommige weerstanden kunnen opereren bij heel hoge spanningen (in de orde van 100 V) en aan heel hoge snelheden (een aantal GHz). Dit maakt hen dan ook heel geschikt voor deze toepassing. Hoewel de ogenblikkelijke dissipatie in de weerstanden tijdens een ESD-puls kan oplopen tot een paar Watt, is dit geen begrenzende selectiefactor, aangezien de ESD-pulsduur te kort is om destructieve gevolgen te hebben voor de attenuatieweerstanden. De uiteindelijke meetprobe wordt dan verkregen door connectorpinnen aan de ingang van de attenuator te verbinden. Hiermee kunnen de spannings- en stroomgolfvormen dan gemeten worden op de IO-bondpaden van een op chip geïntegreerde ESD-protectie. Om zo een spanningsmeting tot een goed einde te kunnen brengen is er nood aan een referentie. Aangezien een stabiele, laagimpedante referentie niet altijd voor

handen is in de nabijheid van een ESD-puls en aangezien de gegenereerde elektromagnetische velden meten met behulp van een externe referentie kan bemoeilijken, is een differentiële meting over twee nabijgelegen bondpaden de beste keuze. De stroomlussen in een dergelijke miniatuur differentiële meetprobe zijn dan ook heel wat kleiner. Wanneer deze probe dan nog eens goed afgeschermd is, heeft dit een heel lage elektromagnetische susceptibiliteit tot gevolg. Op deze wijze kan zo een differentiële meetprobe accuraat de spanningsgolfvorm ten gevolge van een ESD-puls opmeten. De stroomgolfvorm kan, indien de impedantie tussen twee punten gekend is, uit een opgemeten spanningsgolfvorm berekend worden.

Dit voorgestelde meetsysteem werd gebruikt om de respons van een, in een 0,25 μm BCD ON Semiconductor proces geïmplementeerde, thyristor, op een 100 V, 2 A transmissie lijn puls (TLP, [3]) met een stijgtijd van 0,6 ns en een pulslengte van 50 ns, op te meten. Hiervoor werden een testbord en een meetopstelling met een bandbreedte van meer dan 5 GHz en een dynamisch bereik van meer dan 40 dB ontwikkeld. Dit werd in detail beschreven in dit proefschrift, waarbij de nadruk werd gelegd op alle relevante aspecten en afwegingen uitgaande van de systeemvereisten, en in het bijzonder op de architectuurexploratie, het systeemontwerp, circuitontwerp, componentselectie, optimalisatie van het dynamisch meetbereik, EM-simulaties, experimentele karakterisering en studie van kalibratietechnieken. De opgemeten spanningsgolfvorm is voorgesteld in Figuur 1.

Uit zo een verkregen spanningsgolfvorm kan de werkelijke golfvorm, zoals die er op chip uitziet, berekend worden. Dit proefschrift bevat een beschrijving van een kalibratieprocedure die de opgemeten golfvorm compenseert aan de hand van het frequentieantwoord van het meetsysteem. Deze kalibratieprocedure maakt gebruik van op niet-uniforme wijze bemonsterde S-parameters om de spanningstransfertfunctie te berekenen. Het gebruikte compensatiefilter is gebaseerd op een maximum a posteriori (MAP)-schatter, waaraan een extra vrijheidsgraad werd toegevoegd om de ruisversterking door het filter te minimaliseren.

De laatste stap in het ontwerp van een meetprobe is miniaturisatie. In dit werk wordt extra aandacht besteed aan laseralignatie, elektromagnetische koppeling en afscherming. Elektromagnetische veldsimulaties van de meetstructuur in CST microwave studio tonen aan dat een mutuele koppeling in de orde van enkele tientallen pH verwacht kunnen worden. Dit is een enorme verbetering ten opzichte van reeds bestaande contact-karakteriseer-systemen, aangezien elektrisch geconnecteerde opstellingen grotere stroom-
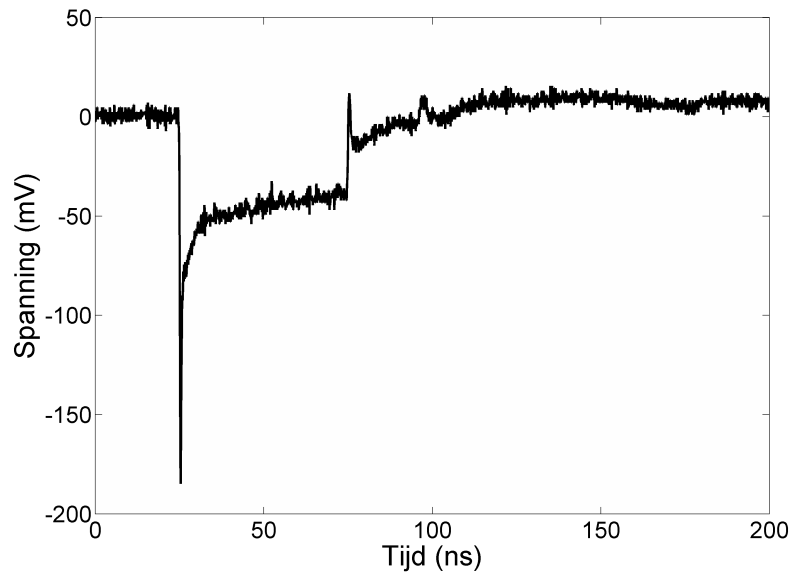
Figuur 1: Opgemeten spanningsgolfvorm

lussen bevatten, wat een grotere mutuele koppeling tot gevolg heeft, en aangezien de zelfinductie van de bonddraden van de testchip zich in de grootteorde van nH bevinden [4].

Dit proefschrift eindigt met een overzicht van de voordelen van de voorgestelde meetarchitectuur en van mogelijke toekomstige aanpassingen en verbeteringen. Het werd in dit werk bewezen dat het mogelijk is om herbruikbare, goedkope, laag vermogen, optische meetprobes met een hoge bandbreedte, een groot meetbereik en een voldoend lage susceptibiliteit, te realiseren, onafhankelijk van de technologie van het testobject. Deze probes kunnen nauwkeurige informatie verschaffen over de respons van bestaande testobjecten, zullen tot waardevolle inzichten leiden in toekomstige ESD-problemen en zijn misschien een kleine stap in de richting van de langverwachte ESD-ontwerpssoftware.

Referenties

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English summary

The level of on-chip ESD protection has been steadily increasing over the past couple of decades. This greatly reduced the number of ESD caused circuit failures, especially during handling for testing or mounting on a board or module. To cope with the ever growing demand for new ESD protection techniques, a better understanding of the real threats is essential. To this end, ESD waveforms will need to be measured with extra attention to the transient response. This measurement needs to be performed at the on-chip ESD protection itself to minimize transient measurement errors due to parasitics (e.g. bondwires,...). This way, the behaviour of the protection circuit can be directly linked to the measured waveforms. In this work, a low cost measurement probe is presented, which, due to its low sensitivity to electromagnetic interference, can be used for on-chip ESD-waveform characterization. This provides invaluable in situ information to the ESD protection development process in the search for robust electronic designs.

A system-ESD pulse contains information in a frequency band up to 5 GHz considering a dynamic range of 35 dB [1]. A way to digitize such a pulse would be by adding an on-chip sampling circuit to the chip-under-test. This circuit would require specifications similar to those of the sampling circuits that can be found inside a commercial high speed sampling oscilloscope front-end. Also, an ESD-pulse generates a strong, interfering electromagnetic field with the same frequency range as the digitized pulse. This interfering field limits the digitization performance of such a system, e.g. due to crosstalk or power/ground bounce. Instead of using a direct sampling technique in an EMC hostile environments, the main idea of the architecture presented in this work is 'divide and conquer'. The in situ digitization problem is divided into a transport and a digitization problem. The probe captures the ESD-waveform at the device-under-test (DUT) in the EMC hostile environment and transports it to an EMC-clean environment, where the waveform can be digitized by a high speed sampling device (e.g. oscilloscope) without interference. There are a few methods to transport a wideband signal through an EMC-hostile environment. In this work, an

optical link is used because of its inherent immunity to electromagnetic signals [2]. The measurement probe consists of a circuit in which the measured ESD-signal is rescaled until it is situated in the linear range of a laser, which performs the optical modulation. Nowadays, small, high speed lasers are commercially available at low cost. Afterwards, the optical signal is demodulated by a photoreceiver and digitized. The optical link provides a galvanic isolation between the ESD-pulse and the high speed sampling device. Still, this laser needs to be driven. As ESD-pulses have a very high instantaneous power of which only a fraction is to be used in the laser, the laser driver can be implemented as a broadband attenuator, converting the measured voltage signal into a laser current. Resistors are very linear, which gives them a very predictable behaviour. Some of these can be found operating at very high voltage levels (order 100 V) and very high speeds (several GHz). These characteristics make them suitable for this ESD measurement application. Although the instantaneous power dissipation in the resistors can become in the order of Watts during ESD-pulse measurements, this is not a limiting resistor requirement as the pulse duration is too short to have a destructive effect on these attenuation resistors. The probe is finalized by connecting probe tips at the input of the attenuator. An on-chip ESD protection device is connected to several IO-pads which can be probed to measure the voltage level at these points. This voltage measurement requires a reference. As a stable, low impedance voltage reference can hardly be found near an ESD-pulse and external references are hindered by large magnetic fields, a differential probe should be used across two nearby bondpads. Bondpads are placed very close together, this way it is possible to make a miniature differential probe with very small current loops. If this probe is well-shielded, this results in a very low electromagnetic coupling. This way, this measurement probe can characterize the ESD voltage waveform. The ESD current waveform can be calculated out of a measured voltage waveform if the impedance is known.

The presented measurement system was used to obtain the (scaled) response of a silicon-controlled rectifier implemented in a 0.25 μm BCD process of ON Semiconductor, to a 100 V, 2 A transmission line pulse (TLP, [3]) with a rise time of 0.6 ns and a pulse length of 50 ns. To this end, a testboard and a measurement setup with a measurement bandwidth of more than 5 GHz and a dynamic range of more than 40 dB were developed. This research is thoroughly described in this work, focusing on all relevant aspects and trade-offs starting from the system requirements and focusing on the architecture exploration, system design, circuit design,

component selection, optimization of the dynamic range, EM simulations, experimental characterization and study of calibration procedures. The resulting measurement voltage waveform is presented in Figure 2.
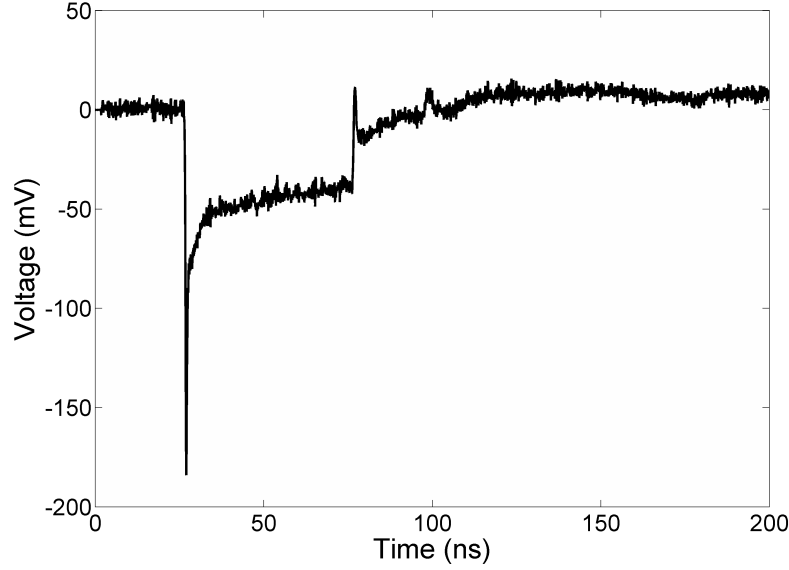
Figure 2: Measured voltage pulse

To obtain the correct on-chip voltage waveform, the measured voltage waveform needs to be compensated for the frequency response of the measurement device. To this end, a calibration procedure is presented in this thesis. This calibration procedure uses non-uniformly sampled S-parameters to calculate the voltage-to-voltage transfer function. The selected compensation filter is based on a maximum a posteriori (MAP)-estimate. A degree of freedom is added to reduce the noise amplification in the filter.

The final step in measurement probe design is miniaturisation. In this work, extra attention is paid to laser alignment, electromagnetic coupling and shielding. Full 3D electromagnetic field simulations of the measurement structure in CST microwave studio indicate that a mutual coupling in the order of tens of pH can be expected. This is a vast improvement over the commonly known off-chip contact characterisation systems as electrically connected setups contain larger current loops, resulting in a larger mutual coupling and DUT bondwire inductances are in the order of nH [4].

This dissertation concludes with an overview of the advantages of the presented measurement architecture and of several improvements that can be made in the future. In this work, it was proven that reusable, low cost, low power, optical measurement probes can be realised with a high enough bandwidth and dynamic range and a sufficiently low susceptibility to successfully reproduce an ESD-signal in an EMC-clean environment, independent of the used technology of the device-under-test. These probes will provide more accurate information on the response of the protection device, bring invaluable insights in future ESD problems and can perhaps even be a small step towards the eagerly awaited ESD design software.

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- **G. Colman**, J. Bauwelinck, R. Gillon, A. Wieers and J. Vandewege, *Wideband measurement system for on-chip ESD waveform characterisation*, IET Electronics Letters, Vol. 48, No. 3, pp. 150-152, February 2012

- **G. Colman**, J. Bauwelinck and J. Vandewege, *Waveform measurement system for on-chip ESD-pulses*, 12th UGent FEA PhD Symposium, Gent, Belgium, December 2011

- **G. Colman**, J. Bauwelinck and J. Vandewege, *DC-coupled directional bridge front-end for vector network analyzer receiver in GHz-range*, IEICE Electron. Express, Vol. 8, No. 11, pp. 814-818, 2011

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- **G. Colman**, J. Gillis, J. Bauwelinck and J. Vandewege, *Low-cost kHz-to-GHz harmonic vector network analyzer for embedded applications*, 9e UGent - FirW Doctoraatssymposium, Gent, Belgium, pp. 206-207, December 2008

- **G. Colman**, G. Torfs, J. Bauwelinck and J. Vandewege, *Low-cost circuit incorporates mixing and amplifying functions*, EDN, Vol. 53, July 2008

Preface

This thesis is based on the research performed during my doctoral time at INTEC_design. The INTEC_design laboratory [1] is a research group within the department of Information Technology (INTEC) of the engineering faculty of Ghent University. INTEC_design offers graduates a PhD training in advanced electronics, including the specification and design of innovative electronic hardware, firmware and embedded software. The main applications concern RF and broadband communication, including fiber optics.

The author worked on two different research projects in the domain of instrumentation. The first project was the Vector Network Analyzer project or VNA-project. It was an academic research project, meaning that no external industrial partner was involved. In this project low cost vector network analyzer architectures, which would allow for easy system integration, were studied. This is a challenging, but very interesting topic for a junior design engineer in the field of instrumentation. The author worked in a frequency range between 300 kHz and 2.5 GHz. This resulted in a low cost harmonic vector network analyzer architecture [2].

A Vector Network Analyzer characterizes a device under test (DUT) by means of Scattering- or S-parameters in the frequency domain. An S-parameter describes the relationship between an incident wave at an input port of the DUT and the reflected or transmitted wave at respectively the same or another port at the same frequency, when all ports are terminated by a known impedance Z_0 (usually 50 or 75 Ω). To this end, commercial vector network analyzers use a transmitter that can generate sine waves (single frequency) with a very broad frequency range. As S-parameters are small-signal parameters, the DUT has to behave in a linear way when stimulated by the incident wave. This imposes a restriction on the power of this incident wave. Often the output power of the VNA-transmitter can be changed over tens of dB.

In the harmonic vector network analyzer architecture, another type of narrow-band signals is used: the square wave. A square wave consists of strong harmonics, of which each harmonic is a narrow-band signal. This means that each harmonic contains amplitude and phase information at a single frequency point. The frequency points corresponding to different harmonics have a known ratio. This makes it possible to isolate the information carried by each harmonic if the system remains linear. Advantages of this technique are that measurements at different frequencies can be performed in parallel and that the use of a square wave allows for easy integration of the generator . Also the fundamental frequency of these square waves can be low, as long as the harmonic at the target frequency is strong enough. During this research, a methodology for selection of the harmonics for each frequency range was presented and a transmitter and receiver proof-of-concept were designed. More research on VNA-testsets resulted in integration of directional bridges in the VNA receiver front-end [3]. This is performed by replacing the broadband transformers in commercial VNA directional bridges by the differential mixers in the first receiver stage. This also allows the directional bridge to work near DC.

After this first project, the author was enlisted in a second research project. This was the IWT-ProSE-project in which ProSE stands for Protections for System level ESD (Electrostratic discharge) [4]. This project was partly funded by the agency for Innovation by Science and Technology. Next to Ghent University, there were three industrial partners involved, i.e. ON Semiconductor Belgium [5], Sofics [6] and NMDG [7]. The ProSE-project deals with the research for new and improved protection techniques against System level ESD-pulses in various applications (e.g. automotive, industrial,...). To this end, new ESD-measurement technique was required for test and verification purposes. This measurement technique would be able to perform accurate measurements of on-chip voltage and current waveforms, both at the I/O-pins and inside an ESD-protection, caused by an ESD-pulse, in various circuits and applications, without itself being influenced by this ESD-pulse or influencing the behaviour of the circuit. In this work, an electro-optical probing technique, researched by Ghent University in direct cooperation with ON Semiconductor Belgium, is presented. For the first time, accurate, high-impedance, differential, in-situ ESD-voltage and -current waveform measurements with a high bandwidth and low electromagnetic susceptibility, due to a low coupling and high common-mode rejection ratio, are made possible. This will lead to new insights in current and future System level ESD protection devices. Due to the high level of

innovation, this work has been chosen as the main subject of this dissertation.

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1

ESD-protection: not a free lunch

Although the phenomenon of Electrostatic Discharge (ESD) itself is not commonly known to the general public, it has various appearances which are widespread, e.g. as a lightning strike or sparks that emerge when touching a car door in winter, etc. The Oxford English Dictionary [1] defines electrostatic discharge as: 'the action of allowing a stationary electric charge to flow out from where it has been confined.' Another definition could be: 'the transfer of electrostatic charges between two objects with different electrostatic potentials.' This is already known for a very long time. In this chapter, a short historical overview of ESD is provided (section 1.1) and more information is given on the ESD problem and ESD-protections in Integrated Circuit (IC)- design (section 1.2). Section 1.3 deals with methods to test ESD-protection devices. It gives an overview of the different models, the state of the art test equipment and a situation of this work in the field of ESD-tests. For this introductory chapter, the author mainly relied on three works dealing with on-chip ESD protection devices: [2], [3] and [4].

1.1   A short history of ESD

The history of ESD starts near 600 BC, when the Greeks observed attraction of lightweight objects to a piece of amber, after rubbing this piece with a piece of fur. This may not be the first observation of static electricity generation, however, it was believed to be the first documented experiment, and consequently the discovery of static electricity.

In the 15th century, sudden explosions of munition depots due to electrostatic discharge, led to the first implementations of static control procedures and devices. These procedures, introduced by European military agencies, were to prevent the ignition of gun powder during storage.

The understandings of modern concepts of static electricity were only established after a few more centuries of research activities conducted by Gauss, Coulomb, Faraday, etc. One of these research activities was the famous Benjamin Franklin experiment, when he flew a kite during a storm and observed the Leyden jar placed close to one end of the kite's wire being charged up. This experiment led to the invention of one of the most significant ESD protection devices in scientific history: the lightning rod.

After World War II, ESD became a real issue as highly insulating polymeric materials found widespread usage in industry. These materials made static charge accumulation possible, which could cause machinery shutdowns.

The devastating ESD damage problem was not taken into serious consideration until the modern microelectronics technologies took the role in everyday life. With the invention of the semiconductor transistor in 1947 and the development of metal-oxide semiconductor technologies in the sixties, the impact of the invisible ESD phenomena became materialized. The number of electronic system failures due to ESD-events escalated exponentially in the seventies. Statistics indicated that up to 30% of all IC failures might be attributed to ESD [5]. This resulted in a semiconductor industry cost of billions of U.S. dollars annually. Consequently, the military began to develop standards to govern ESD immunity of electronic products.

Today ESD is a buzzing line of research, as with the semiconductor IC technologies advancing to the very-deep-sub-micron regime comes a higher ESD vulnerability. This makes research for new ESD-protections and measurement systems increasingly important.

1.2 ESD-protection

1.2.1 The ESD problem

In a typical work environment, a charge of about 0.6 μC can be induced on a worker with a body capacitance of about 150 pF. This charges the worker's body to electrostatic potentials of 4000 V or greater. Any contact by the charged worker with a grounded object, such as an IC-pin, will then result in an electrostatic discharge with peak currents of multiple amperes for a duration of about 100 ns. The energy associated with this discharge could cause failure to electronic devices and components, or in this case destruction of the manipulated IC. This example clearly illustrates the large voltage and current ranges that need to be dealt with. Where normal transistor operation is in the voltage range up to 5 V and the current range up to 100 mV in high speed applications, ESD-pulses span voltage and current ranges up to thousands of volts and tens of amperes.

ESD-damage can be thermally initiated as device or interconnect burnout. The high currents could also lead to on-chip voltages that are high enough to cause oxide breakdown in thin gate MOS processes. This voltage level does not necessarily result in destruction of the device. Sometimes the damage is too weak to be detected easily, as the device seems to work well, but does not meet its specifications, or as the damage only becomes visible over time. Where a decade ago ESD-damage was typically caused by the first reason, nowadays the second cause has gained in importance. This can be explained by the enormous technological evolution in chip design which has been occurring over the last couple of years. This technological evolution resulted in a reduction of feature size to obtain an increase of transistor speed, indicated by the ft-value of the transistors (Figure 1.1), and a higher level of on-chip integration. As a result, the gate oxide thickness was decreased, as indicated by the Equivalent Oxide Thickness (EOT)-curve in Figure 1.2. This resulted in a rapid decrease of the gate oxide breakdown voltage, as indicated in Figure 1.3. This makes protection against high voltage peaks increasingly important.
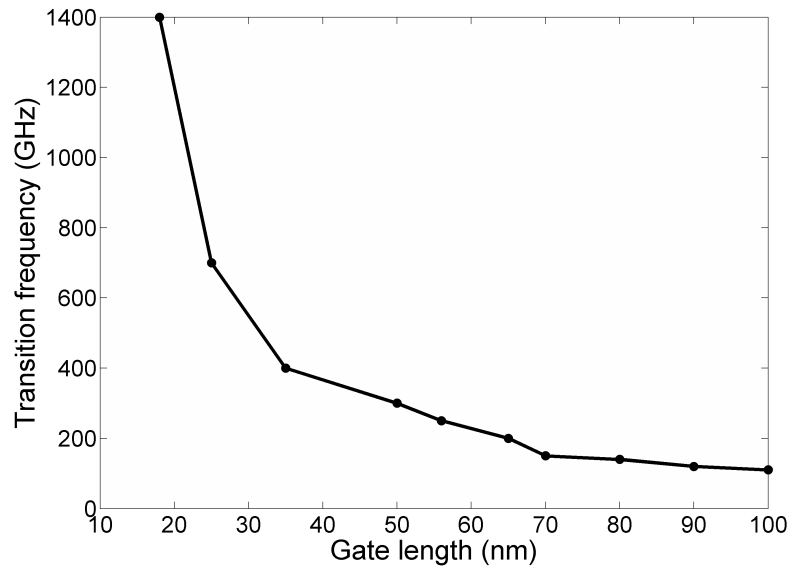
Figure 1.1: Transition frequency in different IC-technologies [6]
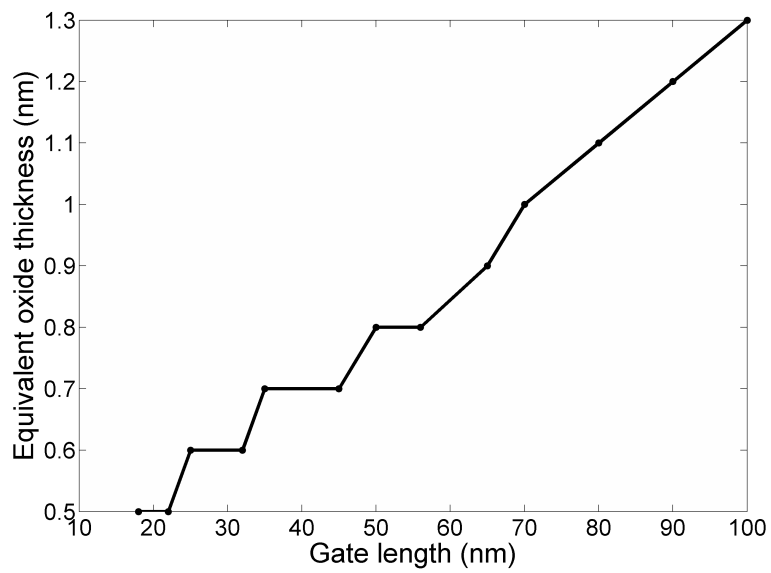
Figure 1.2: EOT in different IC-technologies [6]
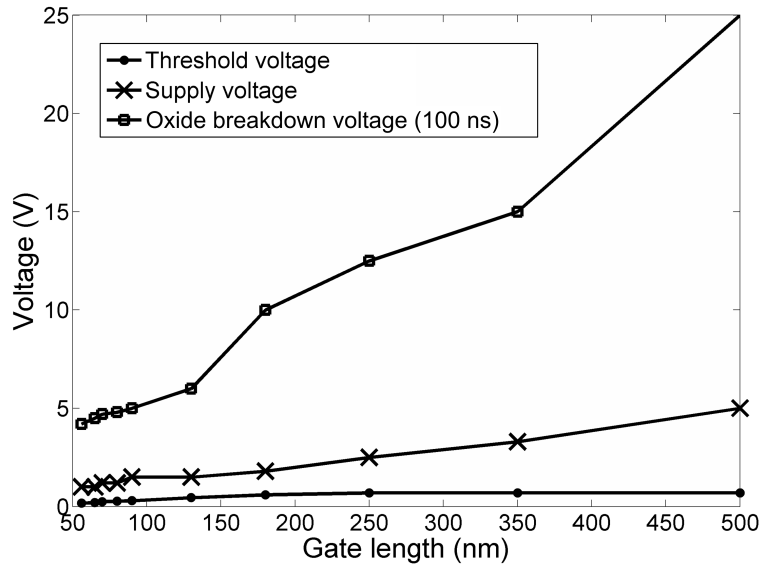
Figure 1.3: Threshold, supply and oxide breakdown voltages in different IC-technologies [6]

1.2.2 ESD-protections

In the past decades, profound progress was made in understanding the ESD fundamentals that are relevant to semiconductors. This resulted in a long list of methods to protect electronic components against ESD strikes at different levels. At the top level, a systematic ESD control program should be established, preventing static charge generation and providing a safe way for static discharging in work environments. Efficient measures include using well-grounded static protective work areas and an ESD protective floor, preventing human body induced electrostatic generation by using ESD protective shoes, clothing and wrist straps, using antistatic materials to prevent charging and static dissipating materials to safely discharge the accumulated static electricity, and promoting the use of ESD symbols. Nonetheless it is important to keep in mind that no matter how good such an ESD control program could be, electrostatic discharge will still occur, although at a much lower occurrence rate. The effects can be countered by integrating ESD protection circuits on chip.

If an ESD pulse finds its way to an unprotected IC, this pulse follows the current path with the lowest impedance to ground, potentially damaging or destroying the IC. The basic operation principle of an on-chip ESD protec-

tion circuit is to direct the ESD-pulse to a pre-defined current path around the sensitive core circuit of the IC. Therefore, a full chip ESD-protection consists of a combination of current limiting devices and voltage sensitive switches or clamps directed to the power supply or ground. By adding a parallel current path with a controlled resistance, the voltage level on the chip can be kept low, irrespective of the magnitude of the externally applied current pulse. Although this principle is easy to understand, the implementation is often a challenge due to the high complexity of current paths and resistances.

A good ESD-protection needs to comply with four requirements: robustness, effectiveness, speed and transparency.

- Robustness describes the ability of the ESD clamp to handle ESD current by itself. The robustness level is defined as the ESD level at which the clamp, taken on its own, fails. A clamp is robust to a certain ESD pulse when the standalone clamp is not damaged by this pulse.

- Effectiveness describes the ability of the clamp network to limit the voltage to a safe level, such that circuits in parallel with the ESD-protection do not fail. If, for example, an ESD-clamp protecting an Input-Output (IO)-port is robust to a certain ESD level, but other elements of the IO-circuit, such as the output driver or some parasitic path, activate and fail at a lower ESD level, the ESD-clamp is only effective to this lower level for this particular IO-network. To achieve higher protection levels, the voltage sustained across the ESD-clamp must decrease or the turn-on voltage of the failing elements must increase. A powerful tool to aid in defining the effectiveness of a protection device is an I-V(current-voltage)-characteristic. This shows the pulsed high voltage and high current behaviour of the device. It can be used to distinguish several device characteristics, e.g. the trigger voltage level, i.e. the voltage level at which the device starts to conduct and at which the I-V characteristic leaves the voltage axis; the failure point; the conductance of the device, i.e. the instantaneous slope of the I-V-curve; etc. The I-V-characteristics of three examples, illustrating the effectiveness of the ESD protection system displayed in Figure 1.4, are presented in Figures 1.5, 1.6 and 1.7.
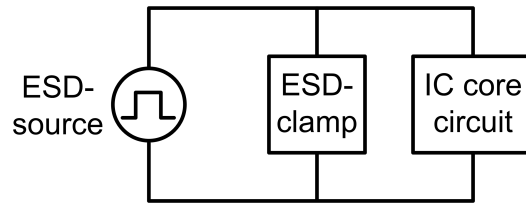
Figure 1.4: ESD-protection system

In these three cases a robust ESD-protection is assumed, together with a non-robust IC core circuit that includes parasitic parallel paths. The reader can easily verify that this is indeed possible, as in all cases the breakdown current level of the ESD-protection is larger than the breakdown level of the core circuit. The point where breakdown occurs is indicated in the figures by the failure point.
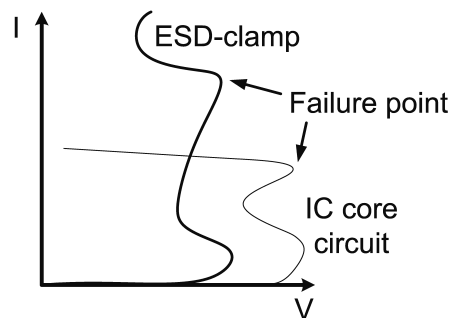
Figure 1.5: I-V characteristics first example: effective protection

The first example shows an I-V characteristic of an effective ESD-protection (Figure 1.5). The ESD protection device triggers and conducts at a lower voltage than the core circuit. Up to its failure current, the ESD-clamp limits the voltage to less than voltage needed for conduction (and failure) of the core circuit. Therefore, the ESD protection device is effective.
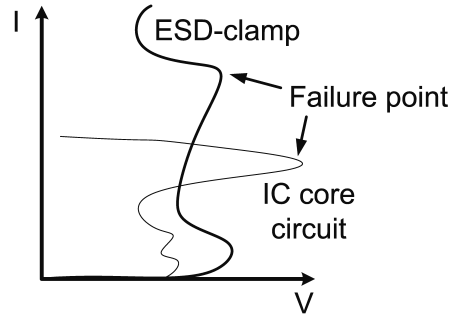
Figure 1.6: I-V characteristics second example: effective protection

Figure 1.6 also presents an effective ESD-protection. Although the parallel paths in the core circuit of the IC, trigger and conduct below the trigger voltage of the ESD-protection, these paths are sufficiently resistive so that the ESD-protection can still trigger below the failure voltage of the IC core circuit.
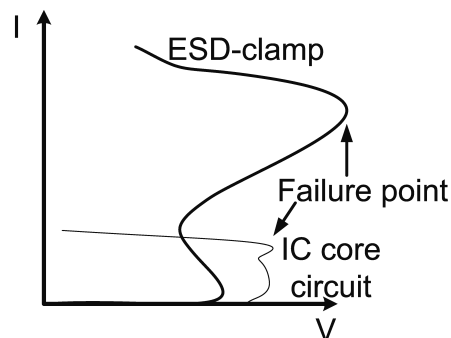
Figure 1.7: I-V characteristics third example: ineffective protection

In figure 1.7, an ESD-protection is shown that is ineffective in protecting the particular core circuit. The parallel paths in the core circuit trigger and conduct at a lower voltage than the ESD-clamp. This means that the core circuit consumes all the ESD-current, failing before the ESD-clamp can trigger.

These examples give an illustration of the effectiveness requirement. More examples and information on this requirement can be found in [7].

- Speed: Even robust and effective ESD networks must activate sufficiently fast to clamp the ESD event at a safe level. Although this is inherent to nearly all protection schemes, some clamps have such a slow triggering speed that the pad voltage exceeds safe levels, causing failure in parallel circuits.

- Transparency: An ESD-protection is transparent if it does not interfere with the normal operation of the chip itself. This includes the impact of the protection on parameters and specifications, e.g. input capacitance, leakage, power sequencing, etc. Transparency becomes particularly important for high-frequency signal pins and low-leakage power supplies.

Although the principle for on-chip ESD-protection is to create a shunting path for safe discharge of static electricity, the design of these circuits becomes much more challenging as IC-technologies continue to shrink. The first issue is the complex interaction between the protection and the core circuit. A working standalone ESD protection device does not warrant chip level ESD protection, because any parasitic device in the core circuit of the IC or surrounding the protection can become an unexpected shunting path. Such a path is usually unable to handle incoming ESD-pulses. This is why ESD protection solutions are not only geometry and technology dependent, but also product-specific. This makes them non-portable. The second issue is situated in the ESD design methodology. While CAD-oriented design is common practice in mainstream IC-design, the first CAD-tools are just emerging in today's ESD protection design practices [8]. These simulators combine a circuit simulator with extracted data from technology CAD-tools [9]. The reason for this gap between circuit simulators and ESD-simulators was the lack of accurate device models and accountable CAD-tools. During an ESD-event, the on-chip components operate outside their normal operating range. The behaviour of semiconductor circuit elements in this region is not covered by standard texts on semiconductor device physics. Nowadays, the first ESD-simulators, able to predict the system response to an incoming ESD-pulse, are emerging. Still, there is a long way to go before these ESD-simulators are sufficiently widespread.

The previous paragraphs illustrated the measures that are taken to reduce the number of ESD casualties, and the difficult specifications and challenges the ESD design engineer needs to face to design on-chip protection circuits. As the actual design of ESD protection circuits is not within the scope of this work, more information on this subject can be found in works as [2] or [3].

1.3   ESD test methods

Although significant progress has been made in the field of ESD protection research and design, it is clear that a continuous evolution in ESD measurement techniques is needed to support ESD designers in coping with the future ESD-challenges. In this section, more information is provided on the currently used test methods, starting with the most important ESD pulse models. Then, a short overview of the state-of-the-art ESD measurement systems is provided, to end with a short introduction of this work, and a situation in the field of ESD-measurements.

1.3.1   ESD-models

An easy way to test the quality of an on-chip ESD protection device, protecting an input pin of a chip, is to use a stress test. This means that a high current pulse is fired to the selected input pin of the chip, and a comparison is made between the system functionality before and after the test to see if damage occurred to the IC. As there is a large difference between the system response on different pulses, this resulted in a standardisation of different pulses. These standards were chosen to resemble interesting real-life cases. Three of these models are: the Human Body Model (HBM), the Machine Model (MM) and the Charged Device Model (CDM). These models are presented in the paragraphs below.

1.3.1.1   Human body model

The human body model is the traditional ESD testing standard. A HBM ESD-event describes a discharge procedure where a charged human body makes direct contact with a grounded device, and electrostatic charges transfer from the human body into the device. It is easy to understand that absolutely repeatable HBM ESD-events are impossible, because every human body has different electrical characteristics, as does each Device-under-test (DUT). One of the earliest and most widely accepted HBM test model is the military standard, MIL-STD-883, published in 1989 [10]. This model uses the simplified equivalent lumped element circuit, illustrated in Figure 1.8, to describe the ESD-event.
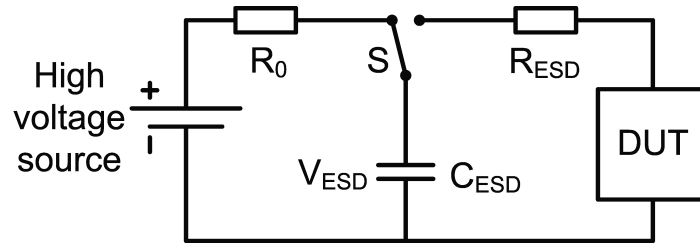
Figure 1.8: Simplified equivalent lumped element circuit human body model (MIL-STD-883)

The charged human body is modelled by a charged human body capacitor C_{ESD} of 100 pF, and the human body discharging resistance R_{ESD} is specified as 1500 Ω. This results in a discharge time constant of about 150 ns and a peak current of 0.67 A for each kV of initial voltage across the charged capacitor. Also, a short-circuit output discharge current waveform is defined in the standard to make pulse reproduction easier. The test device needs to comply with this defined waveform and not with the described circuit model. The described model is certainly over-simplified as it delivers an instant discharge current waveform and does not produce the waveform defined in the same text. The HBM-model circuit needed modification as there is parasitic inductance in the discharge path, resulting in a finite current rise time. Over time, improved HBM ESD test standards were proposed by several organisations to account for parasitic effects in real ESD measurements, e.g. [11], [12] and [13].

1.3.1.2 Machine model

ESD-events are not only caused by a charged human body. Any charged object can discharge into an Electrostatic Discharge Sensitive (ESDS) device if mechanical contact is made between the two objects. The most common ESD-events of such kind, concerning IC-parts, occur when charged metallic tools or machinery make contact with IC components in an IC manufacturing environment. The big difference with the HBM ESD-case is that the parasitic resistance is very low for metallic machinery. This required a new ESD test model for ESD events arising out of large charged objects, discharging through zero resistance. In Japan, the machine model was initially developed as a worst-case scenario for the human body model [14]. The MM-pulse has a much higher current peak and is oscillatory in nature due to parasitic inductances in test systems. Due to its sensitivity to DUT parasitics, it is very hard for testers to comply with the standards.

Nowadays this model is mostly used in the automotive industry. Different versions of the MM-standard can be found in [15], [16] and [17].

1.3.1.3 Charged device model

A third model depicts an ESD-event where a charged IC-part discharges when a pin contacts a grounded object or conductive surface. Such a discharge occurs often in automated manufacturing lines with an insufficient level of grounding or shielding for the IC-devices, or e.g. when devices from a tape reel are dropped on a metal table surface. Although charges are stored in the very small parasitic capacitance of the IC itself, a CDM discharge is very fast (timeconstant of a few ns) and produces very large ESD-currents (up to tens of amperes) because of the very low discharge resistance and inductance. Again it is extremely difficult to build a CDM ESD test device as the waveform highly depends on the parasitics in the discharge path, e.g. the package type. Nowadays, the CDM ESD-events are getting more attention as the thinner dielectric films in the latest CMOS-technologies are much more prone to this type of ESD-event. Different versions of the CDM-standard can be found in [18], [19] and [20].

1.3.1.4 Model overview

In the previous paragraphs, three models for different cases of ESD-events were presented. The current waveforms of a 5 kV HBM, a 500 V MM and a 500 V CDM ESD-event are presented in figure 1.9. The reader should pay attention to the fact that the voltage level indicated before the model type is not the peak voltage on the IC-under-test, but the initial voltage on the capacitor before the discharge event.
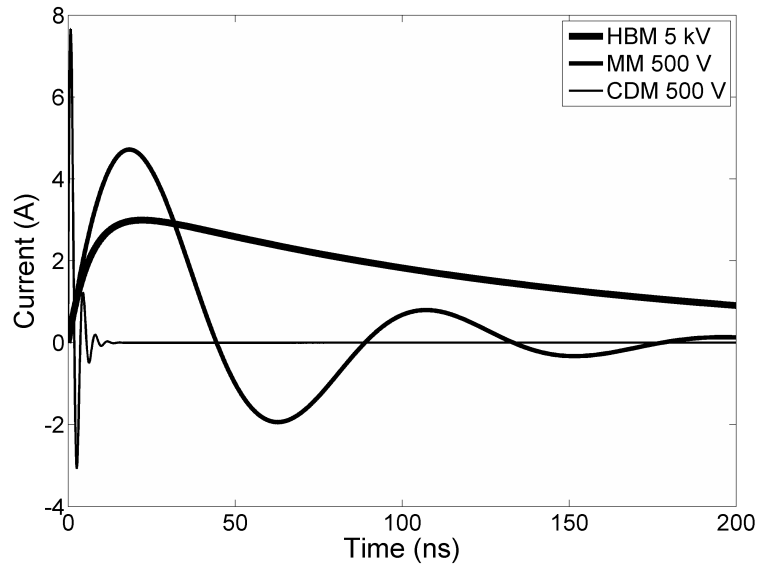
Figure 1.9: HBM, MM and CDM pulse

The question remains to which specifications a system-under-test needs to comply to be ESD-safe. The Industry council on ESD Target Levels [21] is an independent body of ESD experts with the mission to review these ESD robustness requirements of modern IC-products for allowing safe handling and mounting in an ESD protected area.

For more than 20 years, IC component-level ESD target levels for both HBM (2 kV) and MM (200 V) have essentially stayed constant, with no focus on data to change these levels. In the past, arbitrary CDM protection levels have been specified as IC qualification goals with little background information available on actual/realistic CDM event levels and the protection methods available in controls and device design for safe production of IC components. The rapid advancement of IC technology scaling, coupled with the increased demand for high speed circuit performance, are making it increasingly difficult to guarantee the commonly customer specified 500 V CDM specification.

To provide a realistic view of the required ESD levels for modern IC production, the Industry council on ESD Target Levels produced two key white papers on HBM/MM [22] and CDM [23] in 2007 and 2008. The major conclusions of these papers were:

- HBM levels between 500 V to 2 kV are equally safe for qualification.

- CDM levels of minimum 250 V are safe. Lower than this requires
  more detailed control implementation at the production sites.

- MM is a redundant test. Meeting the HBM/CDM test provides suffi-
  cient protection for IC handling and productions.

Both of these papers have been accepted by the ESDA Board and the JEDEC
Board and are now available as public documents.

Other ESD test standards are Charged Body Model (CBM), Human Metal
Model (HMM) and International Electrotechnical Commission (IEC) stan-
dards for system level ESD tests.

1.3.2   Transmission line pulse test

An easy way to test the functionality of ESD protections is to do an ESD
zapping test: An ESD pulse corresponding to a certain ESD test model is
fired at a protection device or system. The possible survival or destruction
of the device or system provide information about the failure threshold cor-
responding to the pulse type. This does not, however, offer insights into
the mechanisms that caused this failure, which are critical to ESD protec-
tion circuit design. More information would be obtained if the voltage and
current characteristics on the IC could be measured. A simple realisation
would be to apply a DC-current to the DUT and to measure the voltage
level. The problem is that such DC-measurements would lead to DUT-
failure at much lower current levels than the normal ESD current range due
to heating. This problem is solved by using current pulses with an ESD-
like time duration. The principle for a Transmission Line Pulse (TLP)-test
is that a piece of transmission line cable is used to produce a stable square
wave pulse to stress an ESDS device. Such a pulse is easier to control
than the pulses defined by the standards mentioned above. Many types of
TLP-systems exist. A piece of transmission line is precharged to a specified
voltage level. It then discharges through a constant matching resistor and
put into another transmission line with a characteristic impedance of 50 Ω
into the DUT. Instantaneous voltage and current data are obtained by prob-
ing the current and voltage of the DUT, e.g. by means of an oscilloscope.
The DC leakage current is measured after each ESD-test. By incrementing
the TLP pulse height and measuring the steady state voltage and current
level of the pulse, one can obtain an instantaneous I-V curve of the DUT
under stress. This I-V curve and the leakage current information are essen-
tial for a designer to debug and optimize a design. One key point in using
TLP-tests is to correlate the results to those obtained using other models.

This can be done by setting TLP parameters, such as pulse duration and rise time, accordingly. As shown in [24], TLP is not the only means of to acquire the I-V curve. In this article the author uses an HBM-pulse, a pulse which is much closer to the ESD events occurring in nature, to derive this information.

1.3.3   State of the art

As ESD is a hot topic in electronics nowadays, there is a large variety in ESD measurement equipment available. The first type focuses on direct ESD-prevention on the work floor. This varies from a basic wrist strap and footwear, ESD quality checking devices to high voltage measurement instruments and field monitors [25] [26] [27]. The high voltage measurement devices are used to locate regions with large electrostatic charge accumulation, as these regions are prone to cause ESD-events. These ESD-events can be detected, and also located, by field monitors. Multiple ESD-detections indicate a possible breach in the ESD-protection measures, e.g. a wrist strap ceasing to function.

Another type of ESD measurement equipment helps the ESD-engineer in his search for new ESD-devices. This type consists of ESD guns and complete pulse generator and ESD voltage and current waveform measurement solutions. These complete solutions are able to generate multiple standard waveforms with a large peak current range, different rise times and pulse widths and perform voltage and in- and outcoming current measurements at the same or at other test ports. Some of these solutions have options to perform simultaneous zapping tests at multiple test ports or do automatic destructive judging e.g. by measuring the leakage current of the device under test after each pulse. Also compact, portable versions of these systems are available. The main applications are: ESD robustness characterisation on wafer-, chip- or board-level; Safe-Operating-Area (SOA) measurements of active and passive devices; reverse and forward recovery measurements of diodes; determination of breakdown and turn on/off characteristics of devices and measurement of the impulse response. Some manufacturers of these complete solutions are [28], [29] and [30]. To be able to perform on-wafer measurements, these systems are combined with wafer probers, RF-probes and probe cards. Some manufacturers are [31] and [32]. There are RF-probes available in different frequency ranges with a very high bandwidth (e.g. DC to 26 GHz) at a fixed characteristic impedance (e.g. 50 Ω) or high input impedance, with and without grounding point. Also dual probes are available and probes can be mounted on a probe card with a fixed pitch.

In the academic world, ESD measurements have also become a hot topic; next to articles dealing with verification of simulation models [33] [34], publications on measurements of radiated fields caused by ESD-events [35] [36] [37] or on the used tools themselves [38] are widespread. These results have been obtained by using adequate measurement methods and devices, which have been improving over the years. Two main types of ESD-pulse measurement techniques are used to obtain information on the ESD-events and the ESD protection devices: contact and non-contact techniques. In non-contact techniques, electromagnetic fields near ESD-events are measured to obtain information about coupling, or further processed into voltage or current information on a nearby surface [39]. Contact measurement techniques directly measure the voltage and current waveforms on a specific point, e.g. by means of a voltage or current probe and an oscilloscope [40].

The main problem with contact measurement techniques is the location of the measurement point. The most interesting measurement point, from the point of view of the ESD design engineer, is directly where the voltage or current of interest occurs. For the voltage waveforms, this is on the IO-pads of the on-chip ESD-protection. The measured current waveforms are the ones going to or coming out of the DUT via the IO-pads. The straightforward measurement technique would be to use measurement probes directly on the IO-pads of the DUT to obtain the in-situ waveforms. As ESD-pulses have a very high instantaneous power, there is a large amount of interference with the probe, which highly reduces the measurement accuracy. This is why the actual measurements are always performed on the coaxial connection between the pulse generator and the device-under-test, resulting in different waveforms. This difference is caused by the parasitics of the DUT and the test setup. To obtain a better estimation of the exact waveforms on the IO-pad of the on-chip ESD-protection, several calibration techniques have been researched to cancel out the influence of these parasitics. In [24] the measured current waveform is compensated by means of an extra voltage measurement and a known DUT. In [41] and [42], linear calibration techniques are presented to correct the measured waveform transients. In [43] this is improved by means of a large-signal calibration technique. In [44] an open-short-load calibration technique is used to de-embed probe needles and system parasitics in a VFTLP-measurement, enabling the use of non-RF-probes for VFTLP-measurements.

1.3.4 This work

In the ProSE-project, a measurement device was needed to perform accurate on-chip voltage and current measurements, both at the IO-pins of the protection and inside the ESD-protection, caused by an ESD-pulse, without influencing or being influenced by this pulse, in various circuits and applications. To perform a correct voltage measurement, a voltage measurement reference or grounding point needs to be set. In a hostile EMC-environment it is not always possible to find an absolute reference point near the measurement point of interest, therefore a full differential measurement probe is best used. Also such a probe should have a high input impedance to minimize the amount of interference with normal protection operation and a very high Common-Mode Rejection Ratio (CMRR). A second problem with the measurement sprecifications is the current measurements. In this project it was requested to be able to perform current measurements on each conductive path of an ESD-protection. The presented systems in the previous section measure in- or outcoming current or the current density on a conductive surface via non-contact techniques. This can be done by combining a high impedance differential probe and a calibration technique. It needs to be possible to perform measurements As the current in each conductive path is to be measured, it must be possible to measure a smaller current signal lying next to a high current signal. Therefore the coupling between the probe and the DUT needs to be minimized. Some commonly known manufacturers of high impedance differential probes are [45] and [46]. These differential probes have a limited bandwidth (< 200 MHz) or low measurement voltage specifications (< 25 V) and can't be used in this ESD-measurement application. In this work, a broadband, differential, voltage and current ESD waveform measurement probe with high input impedance, CMRR and low coupling is presented to meet these specifications. Chapter 2 deals with the architecture exploration, which resulted in a new concept, and the first high voltage waveform measurement tests, proving that the proposed architecture can indeed be used. Also, a current measurement probing technique was presented based on the same architecture. In chapter 3, this measurement architecture is used to perform waveform measurements on real ESD protection structures. Chapter 4 describes a calibration procedure, which operates on the measured waveform based on the S-parameters of the measurement probe. In chapter 5 the probe miniaturisation is addressed. In the final chapter of this dissertation (chapter 6) the author concludes this work and suggests some future research topics to improve the presented measurement probing technique.

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2

ESD-pulse characterisation system

In chapter 1 it was illustrated that, in order to cope with the ever growing demand for ESD protection devices, issues related to a limited understanding of the real ESD-threats need to be encountered. To this end, an on-chip high voltage and current waveform characterisation method needs to be researched. This will provide invaluable insights to the ESD design engineer, in the end improving reliability of electronic systems. This work will focus on the reconstruction of the following waveforms:

- Voltage waveform of a System-ESD pulse on a protected IO-pad

- Current waveform of a System-ESD pulse within the low impedance path of the ESD-protection

Application specifications often require ICs to be able to withstand such pulses during normal operation, hence the need to accurately characterize their shape.

In this chapter a characterisation system for ESD pulses is presented. In section 2.1 the measurement specifications are derived. Section 2.2 presents several measurement system architectures, out of which one is selected. A test setup based on this architecture for the characterisation of voltage waveforms is then presented in section 2.3, of which the test results are shown in section 2.4 and evaluated in section 2.5. Finally, a current waveform characterisation method is presented in section 2.6.

2.1   Measurement system specifications

Before a suitable architecture can be chosen, minimum measurement device specifications have to be derived. As this device measures the internal chip response of an ESD-pulse, the questions "What does an ESD-pulse look like?" and "How much information does it contain?" have to be answered.

There are different ESD-models for various situations. Some popular ones are HBM, MM and CDM [1] [2]. The ESD pulse of interest in this work is the one defined in [3]. This pulse can be generated by a standardized ESD-pulse generator. The external response on a TLP-pulse of the ESD-protection on the chip was measured by On Semiconductor [4]. As no System-ESD response data is at hand, this data, depicted in Figures 2.1 and 2.2, can be used to define the expected amount of information in a System-ESD pulse and to derive the measurement device system requirements.
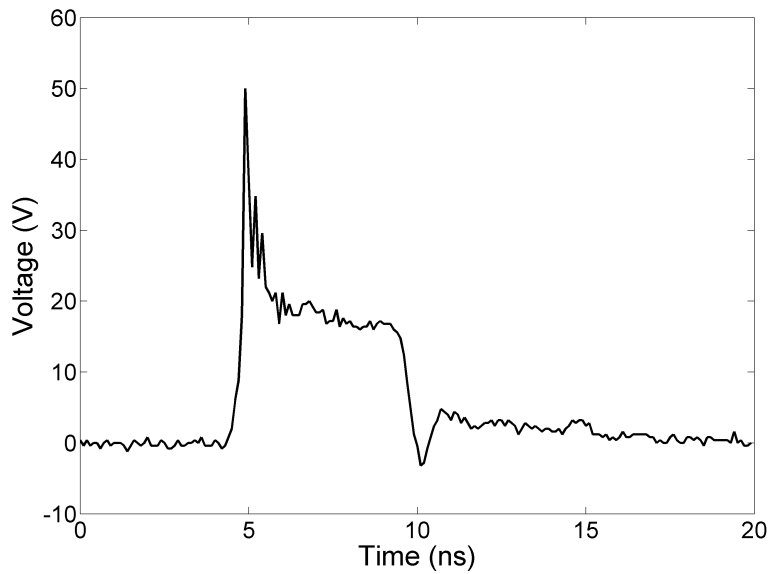
Figure 2.1: Voltage measurement of an incoming ESD-pulse on an ESD-protection device
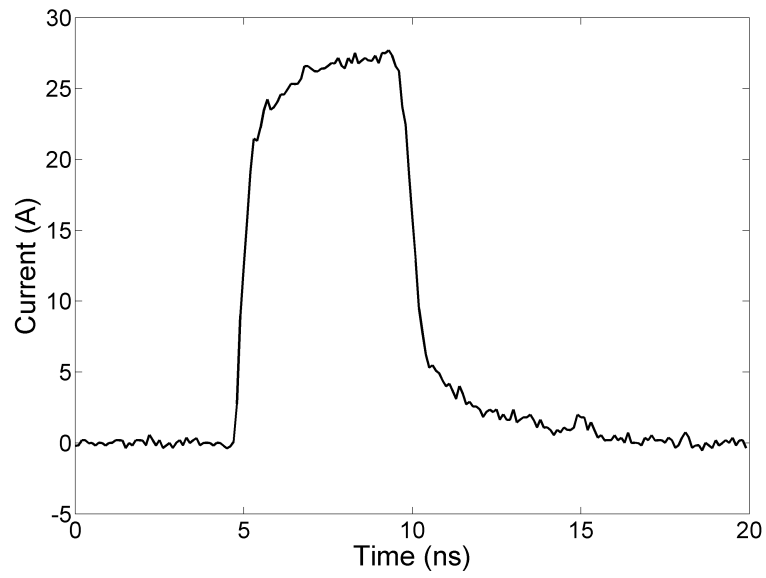
Figure 2.2: Current measurement of an incoming ESD-pulse on an ESD-protection device
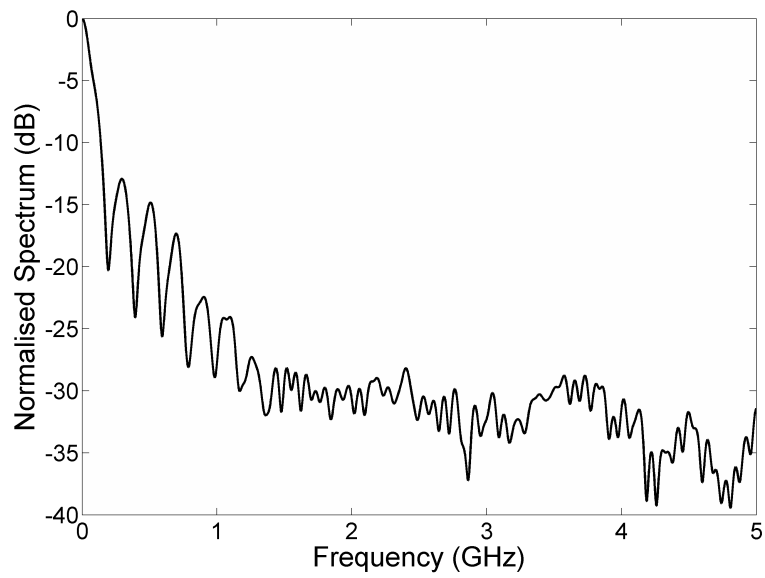
Figure 2.3: Spectrum of the incoming voltage signal

As some signal properties can be defined easier in the frequency domain, a Fast Fourier Transform (FFT) is used to transform the expected voltage signal. The normalized result of the FFT of the voltage waveform in Figure 2.1 is presented in Figure 2.3. Because of the limited amount of FFT processing gain, the FFT noise floor is too high. This processing gain can be increased by increasing the number of samples. Therefore the signal data has been concatenated with zeroes, until the signal rises out of the FFT noise floor [5].

2.1.1   Bandwidth and dynamic range

First, it has to be determined how many information the signal contains and in which frequency range this information is located. This information is enclosed in two important figures: the bandwidth and dynamic range. In Figure 2.3, the data has been collected with a 10 Giga-samples per second (GSps) high speed sampling oscilloscope. If aliasing is not taken into account, the maximum frequency that can be displayed on this frequency spectrum is 5 GHz. Although most of the energy of the pulse is located at the lower frequencies (less than 1 GHz), the signal also contains a non negligible higher frequency part up to about 4 GHz. This higher frequency part contains information on the fast ESD-peak and ringing. In this work both information on the peak and lower frequency information need to be captured. As the power spectrum at the lower frequencies is about 30 dB higher than the power spectrum in the higher frequencies, the target measurement dynamic range is set at 35 dB. This puts an upper bound to the total received noise compared to the input level. To obtain some frequency margin, the target measurement bandwidth is set at 5 GHz. As this bandwidth was derived from a 10 Gbps measurement and aliasing can occur, an extra measurement with higher sample rate was used, showing that there is indeed no relevant information at higher frequencies.

2.1.2   Measurement voltage and current levels

During the waveform analysis in the previous paragraph, no absolute voltage or current levels were mentioned. Still these are important system specifications. The ESD-protections that have been used in this research, clamp the voltage at 80 V. This puts a limitation on the voltage across the DUT. Although the reaction time of ESD-protections is very short, some overshoot can be expected. If 50% overshoot is taken into account, the maximum voltage specification of the measurement device is set at 120 V. To enhance the use of this solution, the design must be able to work with lower voltages

as well, once a minimal number of components is adjusted.

The maximum input current rate passing through the ESD-protection is chosen at 50 A. Although this is mostly a design parameter for the ESD-protection itself, it also provides a maximum limit on the current scale and the generated magnetic field. ESD signals have a very high peak voltage and current, which are far above the input range of any high speed digitizer. Therefore, the input ESD signal is attenuated to a level where it can be digitized. Electromagnetic fields have a very large role to play in this work, as the fields that are generated by the ESD signal can distort the attenuated signal at high attenuation levels due to Electromagnetic (EM)-coupling.

2.1.3   Linearity

An ideal signal measurement device works in a linear way. This means that any linear combination of input signals will result in the same linear combination of the corresponding output signals at the output. A real device is assumed to be linear in a certain range. In this paragraph the linearity requirements are derived.

Any non-linear transfer function of a system without memory, can be written as a series expansion of power terms. In most cases, only three power terms are required to obtain a good idea of the linearity. This results in the transfer function in equation 2.1, where x(t) represents the input signal and y(t) represents the output signal:

$$y\left(t\right) = a_1 x\left(t\right) + a_2 x^2\left(t\right) + a_3 x^3\left(t\right) \tag{2.1}$$

In this equation, the linear contribution is given by the first term, while the second and third term contribute in a non-linear way. It is clear that the linear behaviour of a such a system can be described by the ratio of a_2 and a_1, and the ratio of a_3 and a_1. For simplicity, a_1 is chosen equal to 1. This way the linearity specifications can be set by choosing limiting values for a_2 and a_3. As the non-linear terms in equation 2.1 become more important with rising input signal magnitude, the system linearity is best defined at maximum input magnitude. There are many ways to define 'acceptable' a_2 and a_3 values. In this work, a_2 and a_3 are chosen in such a way that the spectra of the second- and third-order term are 20 dB below the spectrum of the pulse at each frequency. This way the pulse will not be disturbed by non-linear effects. This results in a_2 and a_3 values of respectively $7 \; 10^{-4}$ and $5 \; 10^{-6}$. For these values, the spectra of the terms in equation 2.1 are depicted in Figure 2.4.
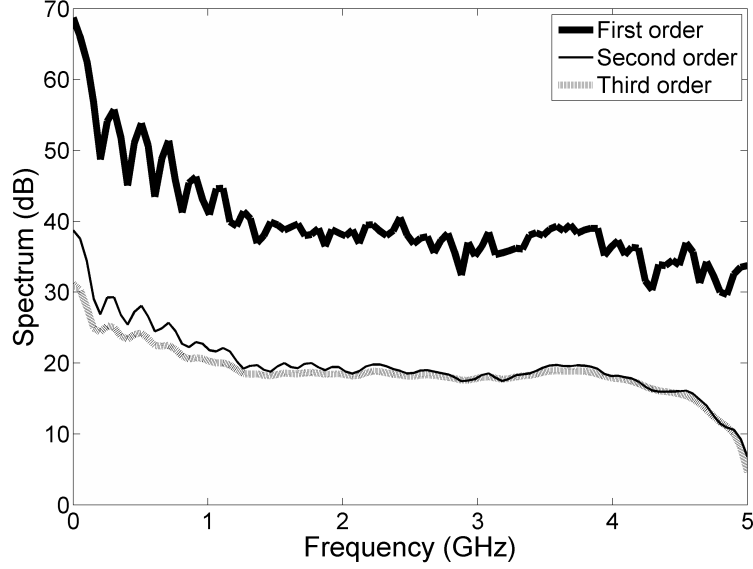
Figure 2.4: Spectra of the linear, second- and third-order terms in equation 2.1

To define the linearity of a device, multiple definitions can be used. Throughout this work the linearity of a system will be characterized by its Second-order Intercept Point (IP2) and Third-order Intercept Point (IP3). These are the theoretical, extrapolated points in a two-tone test where the amplitudes of respectively the second and third order intermodulation products are equal to the amplitudes of the fundamental tones [6].

With these limits for a_2 and a_3 known, the input signal amplitudes, for which the amplitude of the linear terms in a two-tone test is equal to the amplitude of the second- (IM2) or third-order intermodulation product (IM3), can be calculated. The amplitudes of IM2 and IM3 are given by [7]

$$IM2 = a_2 A^2 \tag{2.2}$$

and

$$IM3 = \frac{3}{4} a_3 A^3 \tag{2.3}$$

This results in an Input-referred Second-order Intercept Point (IIP2) and Input-referred Third-order Intercept Point (IIP3) of respectively 1.4 kV and 520 V. These seem very large IIP values, but as the maximum input voltage is 120 V, a significant attenuation is needed anyhow. For example, assume this 120 V signal is attenuated to 200 mV, which is a normal digitizer input value, at 50 Ω by a resistive, and thus very linear, voltage divider of 1/800. Assume this voltage divider is perfectly linear, then the Output-referred Second-order Intercept Point (OIP2) and Output-referred Third-order Intercept Point (OIP3) are equal to the IIP2 and IIP3 multiplied by the gain. This provides the following values at the input of the measurement system after 1/800 attenuation: IP2 = 17 dBm and IP3 = 9 dBm. These are realistic linearity values for standard components. If linearity needs to be improved, a larger attenuation could be used, however resulting in a lower Signal-to-Noise Ratio (SNR).

2.1.4 Clock jitter

In each high frequency sampling system, clock jitter has to be taken into account. For a 35 dB signal-to-noise ratio and a maximum frequency f_{max} of 5 GHz, the sample clock jitter has to be lower than 0.6 ps Root mean square (rms) [8].

$$\text{SNR}_{jitter,dB} = -20 log \left(2\pi f_{max} t_{jitter,rms}\right) \tag{2.4}$$

2.1.5 Stability

The measurement device has to operate under different conditions. Therefore it needs to be stable over time, humidity and temperature variations. To solve this problem, a calibration procedure is required to correct the changing measurement device characteristics.

2.1.6   Measurement system requirements overview

Table 2.1 summarizes the system requirements derived in the previous section.

Bandwidth (3 dB)	5 GHz
Dynamic range	35 dB
Maximum input voltage	120 V
Maximum input current	50 A
IIP2	1.4 kV
IIP3	520 V
Maximum sample clock jitter	0.6 ps rms
Scalability	Lower input signal levels
Long term stability	Recalibration
Electromagnetic Compatibility (EMC)	Near an ESD pulse

Table 2.1: Summary of the measurement system requirements

2.2   Architecture exploration

In this section, several system architectures are presented together with their advantages and drawbacks. Afterwards, the one that offers the best perspective will be realised. As the measurement problem deals with the characterisation of on-chip pulses, the first architecture is an on-chip sampling architecture.

2.2.1   On-chip sampling architecture

In the first architecture, a small high speed sampling circuit is added to the DUT for each point-under-test. As the circuit implementation depends on the chip technology, it can be included in every future design of ESD-protection devices made in the same technology. Two possible approaches are to be considered: repetitive and single shot sampling.

2.2.1.1   Repetitive sampling

A periodic signal is sampled at a low speed, providing only a few samples per period. As not only the input signal value, but also the sample time is sampled in comparison to a trigger signal, the samples can be rearranged into the signal shape [9]. Due to the lower requirements on the sample

rate, a repetitive sampling measurement system is more economical to design. Therefore the validity of this approach in this application is carefully considered.

This approach requires a repetitive input signal with a well-defined start time or trigger signal. Although it is possible to generate multiple ESD-pulses, the reproducibility of the pulse can not be guaranteed. Also the pulse start time can not be predicted due to generator mechanics. If the uncertainty on timing is larger than the jitter specification, this results in a lower dynamic range of the reconstructed pulse due to phase noise. Also because of the large peak power (in the order of 100 W) fired at the DUT, the test might be destructive for the DUT, resulting in a varying pulse response over a number of pulses. These three objections eliminate the use of repetitive sampling as a solution for this problem, which leaves single shot sampling as the only option.

2.2.1.2   Single shot sampling

Single shot sampling is a technique in which only one input pulse is used to reconstruct the signal. This technique can be used for non-periodic signals. The major drawback of this technique is that all samples have to be collected during one input pulse, resulting in much higher sampling requirements. The feasibility of integrating a small single shot sampling on-chip was research to investigate the effect of the high dI/dt values of incoming ESD-pulses on the circuit operation.

A first order model of an ESD-pulse is a discharging capacitor. A non-negligible amount of electric charge is injected at the input of a system during a very short time. An effect of this charge injection is the generation of a very strong magnetic field in the bondwires by which the DUT is connected. When an ESD pulse arrives, there is a sudden charge injection at the input op the chip, resulting in a dI/dt with order of magnitude of 10 to 100 A/ns. This current variation results in a large change in magnetic field [10], inducing a voltage drop over the bondwires connecting the chip in a real application. This voltage drop over a bondwire of 1 nH has an order of magnitude of 10 to 100 V. When these bondwires are used for connecting ground and power rails to the chip exterior, this results in rail bounce. This rail bounce can have a large influence on the biasing of the transistors used in an active circuit. This results in an extra system requirement: only circuits with a very large power supply rejection ratio can be used. In the targeted application, this power supply rejection ratio is needed at frequencies in the GHz-range. To obtain this large power supply rejection, the sampling circuits need a very large gain-bandwidth. To meet these speci-

fications, a technology optimized for the design of a high speed sampling oscilloscope front-end needs to be used.

These two objections question the use of an on-chip sampling architecture in this application. If only technologies optimized for very high speed can be used to perform the on-chip sampling, the waveform characterisation technique can only be implemented on ESD structures in these high speed technologies. In most cases ESD problems can be found in other applications e.g. automotive, industrial,... The technology requirements in these sectors are often very different. Therefore an ESD waveform characterisation technique which is independent of chip technology would be most valuable.

2.2.2   Measurement solution

In the sampling solutions mentioned above, the sampling circuit was always integrated in the IC-under-test. Other possible measurement solutions can be obtained by moving the sampling circuit out of the IC-under test. Again there are two possibilities:

- A measurement solution consisting of two dies, i.e. the IC-under-test with the ESD-protection circuit which is connected to a sampling chip in a technology optimized for high speed sampling.

- A measurement solution consisting of the IC-under-test and a small communication module which captures the pulse and transports it via a communication channel to an external high speed sampling measurement device located in an EMC-clean environment.

In both cases, the IC-under-test is connected to (a part of) the measurement solution. In order for this to work, the IC-under-test has to be adapted in a minimal way to bring interesting voltage and current signals accessible to bondwires or probe tips. Then the measurement solution can be wirebonded to or probed at these outputs. This approach provides the major advantage of technology independence. As long as both IC's can be connected, both the measurement solution and the IC-under-test can be implemented in different technologies. Still the question remains which course to take.

The first approach has as main advantage that the actual measurement device can be encapsulated in a single package, where extra components are only required to collect the sampled data. This in opposition to the second approach where the solution's only function is transportation of the captured signals to the high speed sampling device. Although there are less design restrictions and each part can be designed in a technology optimized

for the application, it can't be guaranteed that the measurements of the first system will not be impacted by the incoming ESD-pulse. The measurement will only be valid if the sampling system is completely isolated from the incoming ESD-pulse, which means that the distance between the IC-under-test and the sampling system has to be large enough. It is clear that the second approach has a higher chance of success. In this case, complete sampling devices, e.g. high speed oscilloscopes, can be used to take care of the sampling functionality and signal processing. This transforms the main measurement problem into a problem of transportation, which is much easier than in situ sampling.

In the next paragraphs multiple ways of signal transportation are reviewed.

2.2.2.1 Differential buffer

The easiest way to transport a signal across a great distance (order of magnitude 1-10 m) is by means of a buffer or line driver. This circuit amplifies (in power) the signal before it is sent to the output pins and driven across a transmission line in the direction of a measurement device. This architecture is depicted in Figure 2.5.
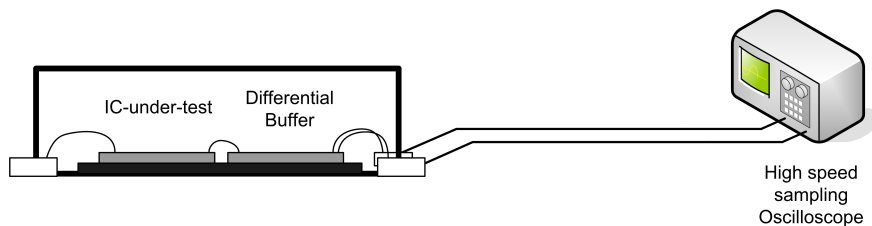
Figure 2.5: Differential buffer measurement solution

The major drawback of this method is that the spectrum of the internal ESD-signal, carrying the desired information, and the ESD-signal on the exterior of the package, a strong interfering signal, overlap in frequency. As the interconnection between the chip and the measurement device will be long (order of meters), the output signal can be impacted by external input-output electromagnetic coupling. The exact isolation value is defined by the mismatch errors in the system, and it is not yet clear if this isolation will suffice. A survey on standard IC-packages resulted in an input-output isolation of 30-50 dB at 1 GHz in a 50Ω environment [11]. This value can be improved by using a differential implementation of the buffer, transmission line and receiver. Also this device has very high demands in terms of

speed, linearity and common-mode rejection. To minimize the risk of fail-
ure, the buffer has to be implemented on another die in the same package.
This implementation comes with a larger cost compared to a single die
solution. Therefore, other solutions with a lower risk of electromagnetic
coupling were considered.

2.2.2.2 Frequency conversion

If the input and output signal are separated in the frequency domain, the
useful output information is accessible irrespective of coupling. As the in-
formation is located within the almost DC - 5 GHz band, only upconversion
can ensure the separation in frequency domain. Two possible techniques
can be used: analog and optical modulation.

- *Analog modulation*

This technique is based on the now commonly used analog modulation
techniques for communication: Amplitude Modulation (AM) or Frequency
Modulation (FM). The information is modulated on a high frequency car-
rier in a linear way, and then transported to the receiver in an EMC-clean
environment, where it can be demodulated and subsequently sampled by
a high speed oscilloscope. In order to have completely separated input
and output spectra, the carrier frequency must be more than 10 GHz. This
frequency should be higher (between 15 and 20 GHz) if practical demod-
ulation and filtering has to be taken into account. The influence of the in-
coming ESD-pulse on the carrier generation can be completely nullified if
the carrier signal is generated by an external signal generator. This way the
on-chip communication module is implemented as an AM- or FM- modu-
lator for a 5 GHz input signal on a 20 GHz carrier with 45 dB of linearity,
which is possible in very fast semiconductor technologies.
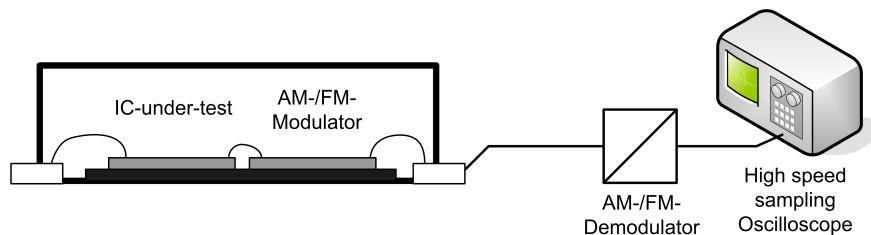
Figure 2.6: Analog modulation-based measurement solution

A complete measurement solution could consist of a package incorporating
the IC-under-test connecting to such a modulator die. This connected via a

wired or antenna link to a suitable AM- or FM- demodulator connected to a high speed oscilloscope. This architecture is depicted in Figure 2.6.

- *Optical modulation*

Another possible solution can be obtained by going into the optical domain. This architecture is depicted in Figure 2.7. In this case a laser diode is modulated by the ESD-signal, and then the emitted light is captured in a well-positioned fiber and directed to an optoelectronic converter in an EMC-clean environment. The resulting baseband signal can then again be sampled by a high speed oscilloscope. To this end, a small module should be included in the package of the IC-under-test (Figure 2.7), or the naked die is to be probed by a small module. This module would consist of one or more laser diodes with their respective bias circuit and some laser drivers.
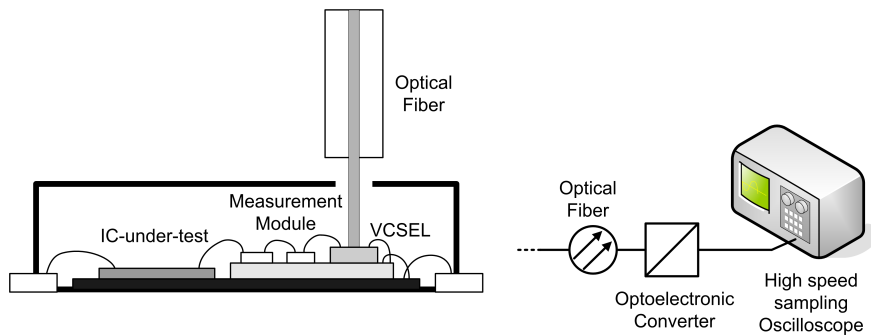
Figure 2.7: Optical modulation-based measurement solution

After comparison of the two remaining possibilities, the optical modulation technique was chosen. This is due to the simplicity of the module to be added in the same package. This way the research can be focused on the main problem at hand: capturing voltage and current waveform information in an EMC-hostile environment.

As stated in the beginning of this chapter, the goal of this measurement device is the monitoring of the voltage waveform on the IO-pad and the current waveform through the ESD-protection. For each of these monitoring tasks, identical laser modules will be used. As there are two quantities to be measured with the same device, i.e. voltage and current, one quantity has to be transformed into the other. In this case, voltage has been chosen as the quantity to be measured. The voltage measurement at the IO-pad can be performed in a direct way. In order to measure the current, Ohm's law

can be used. If the differential voltage across a known resistor can be measured, the current waveform through that resistor is the measured voltage waveform divided by the resistor value. This way, the ESD-current can be measured if voltage probing points are well chosen.

2.2.3   Measurement architecture vs. system requirements

In the previous paragraph, it was proposed to divide the waveform reconstruction problem into two problems:

- Transportation of the waveform of interest to an EMC-clean environment

- Reconstruction of this waveform in this EMC-clean environment

Each of these problems is less difficult than the original problem.

2.2.3.1   Reconstruction of the waveform

Most waveforms in EMC-clean environments can easily be digitized and reconstructed by standard lab equipment. For the reconstruction of the high frequency signals of interest, commercially available high speed oscilloscopes provide a large enough bandwidth and dynamic range. The sample rate and jitter characteristics are good enough for single shot reconstruction of a pulse with frequency information up to 5 GHz and more [12]. Also, the high speed sampling oscilloscopes have trigger circuits that can trigger on signal level at their disposal. This way, these devices are capable of performing high quality single shot pulse measurements without needing extra trigger information from the ESD pulse generator. The major drawback is the cost of such a device, however, nowadays these devices belong to the standard lab equipment that can be found in high frequency electronics and ESD labs. Also, the proposed optical technique provides a galvanic isolation between the DUT and the oscilloscope. This nullifies the chance that this expensive measurement device gets destroyed during ESD measurements.

2.2.3.2   Transportation of the waveform

Nowadays there is a large range of commercially available laser diodes with a bandwidth higher than 5 GHz. A laser diode has a voltage-current diode-characteristic (Figure 2.8), which is strongly non-linear around the threshold current, but linear in its conducting region. The emitted optical power is a function of the diode current (Figure 2.9).
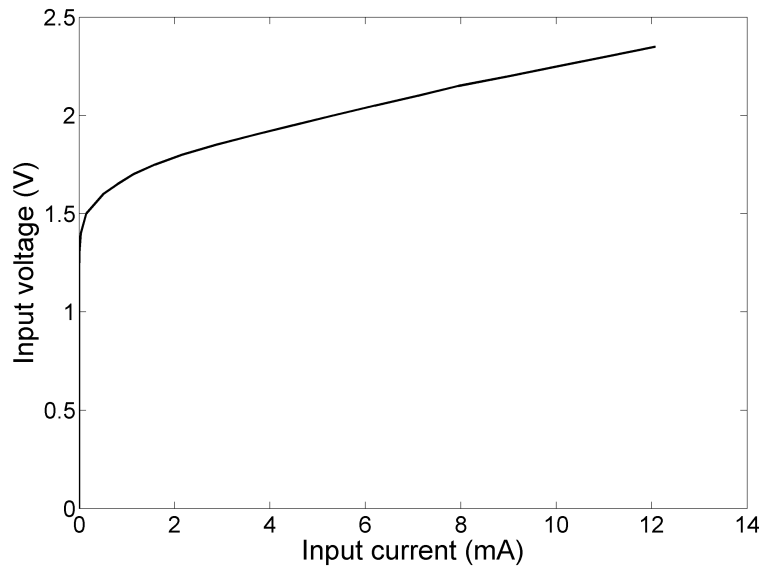
Figure 2.8: DC-VI-characteristic of a laser diode
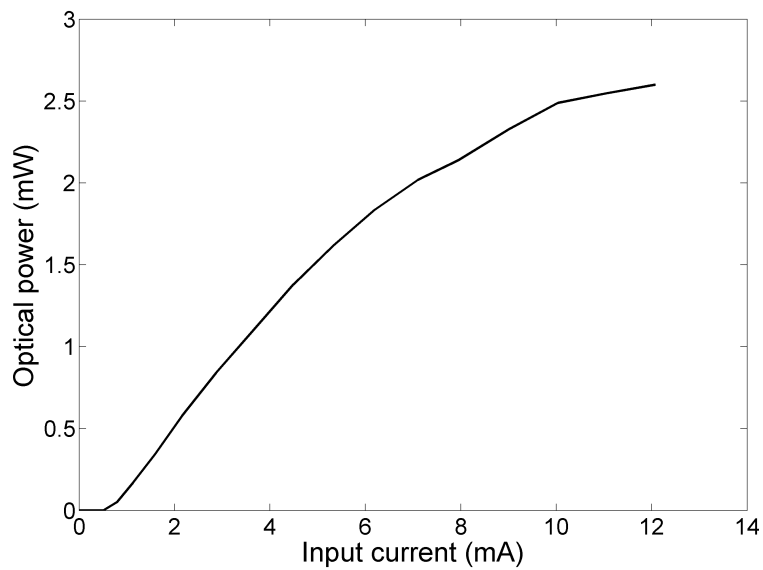
Figure 2.9: DC-PI-characteristic of a laser diode

A bias current has to be injected in order to push the diode in its linear operating range, and then the diode can be modulated by superposing an AC-current onto this current. This improves the linearity of the measurement solution. In this region a laser diode has a stable impedance. This means that an AC-voltage can be used to drive the laser diode. There is a limited input voltage range in which laser diodes can be used. For the laser diodes that have been used in this work, this range is limited up to a few 100 mV. Therefore a large attenuator is required in the laser driving circuit, which also improves the linearity. By changing the attenuation, the system is scalable with input voltage. A laser is susceptible to aging and temperature, therefore the link needs to be calibrated once the laser is in steady state.

In the next sections, a test setup for high voltage pulse waveform measurements will be presented and tested. In section 2.6, it is shown how this architecture can be used for current waveform characterisation.

2.3   Voltage waveform measurement test setup

In the previous paragraphs, the optical modulation architecture presented in Figure 2.7 emerged as the most promising option. This architecture consists of a module, connected to the DUT, which modulates the captured ESD-pulses by means of a laser, an optical fiber leading to a fast photodetector that converts the optical signal back into an electrical signal, and a high speed sampling oscilloscope to perform the digitization. To evaluate the feasibility of the proposed ESD waveform characterisation system, a test setup was developed. Its goal is to digitize high voltage pulses arriving at the measurement input. The setup consists of a high voltage pulse generator which is connected to a measurement module. This module consists of a laser driver circuit and a laser diode. This laser diode is pigtailed to a multimode fiber, which is connected to a photodetector via a Fixed Connector (FC)-connector. This photodetector is then connected to the oscilloscope via a SubMiniature version A (SMA)-connection. If required, low noise amplifiers can be added in between. In the following paragraphs each of these components is thoroughly described.

2.3.1 High voltage pulse generator

As there was no system-ESD pulse generator available in the lab at the time these measurements were performed, for test purposes a high voltage pulse generator was designed of which the generated pulse has specifications comparable to those of a system-ESD pulse.

2.3.1.1 Pulse generator specifications

A typical system-ESD pulse has a rise time which is less than 1 ns. As the DUT will be protected by its ESD-protection, the voltage will be clamped by this protection. The generated pulse needs to have a voltage peak which activates the ESD-protection. This voltage peak has to be larger than 100 V. It would be interesting if, as an extra feature, the pulses have a predictable timing. This is not the case for system-ESD pulses. Also the time between the pulses must be large in order to keep the average power low, thus preventing the destruction of the DUT and measurement module due to heating.

2.3.1.2 Pulse generation methods

There are 2 commonly known ways for high voltage pulse generation:

- Magnetic induction

- Charge based circuits

The first well known pulse generation method is based on magnetic induction. A basic schematic that illustrates the operation principle is shown in Figure 2.10 [13].
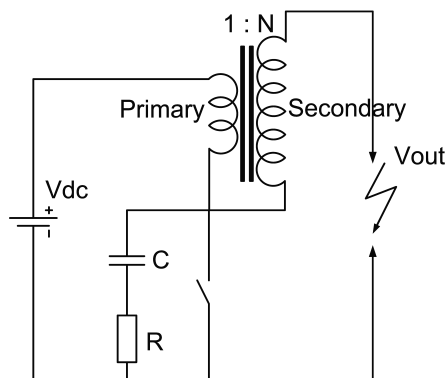

Figure 2.10: Magnetic induction based high voltage pulse generator

The main parts are a DC-voltage source, a high voltage switch and an auto-transformer with a high ratio of turns. Initially the switch is closed, and the voltage source provides a large DC-current flowing through the primary winding of the autotransformer. Due to this DC-current, a large amount of energy is stored in the magnetic field. When the current changes, the amount of energy stored in this field also changes. Due to the conservation of energy, this energy is manifested as electromotive force in the primary of the transformer, resulting in a voltage over the primary winding of the transformer. If the DC-current is suddenly interrupted, e.g. by means of a switch, the magnetic field dissolves very quickly, resulting in a high voltage peak across the primary. This voltage pulse is transformed into an N times larger voltage pulse across the secondary, given by the turn ratio of the autotransformer. The output voltage is then given by equation 2.5.

$$\mathrm{V}_{out} = \mathrm{NL}_{primary} \frac{\mathrm{dI}_{primary}}{\mathrm{dt}} \qquad (2.5)$$

The determining component in this circuit is the switch. This switch has to be selected carefully. It must be able to stand high peak voltages and high peak currents. Also the switch times play a major part in the output voltage waveform. In order to lower the requirements on the switch, a capacitor can be used as indicated on Figure 2.10 to slow down the collapse of the magnetic field. Without this measure, opening the switch could result in an electric arc, possibly damaging the switch. The resistor in series with the capacitor is used to prevent welding of the switch contacts caused by short circuiting the discharging capacitor with the switch. The combination of the resistor and capacitor is often integrated in a so called 'spark quencher' [14].

This method is used to generate very high voltages in a very simple way, therefore it is commonly used in spark generation applications e.g. ignition devices of cars, airplanes, or lighting. A major disadvantage of this method is that both positive and negative pulses are equally generated, where system-ESD pulses are mostly single-sided, as the injected charge is positive or negative.

A second method for high voltage pulse generation is charge based. Again the basic principle is fairly easy. Charge is collected in a reservoir at high potential. This charge is released at a given time, discharging the reservoir to ground potential. This all happens in a very short time, resulting in a high current pulse, which can be converted into a high voltage through an impedance [15]. This general idea can be realized in an electronic circuit, as an example shows in Figure 2.11.
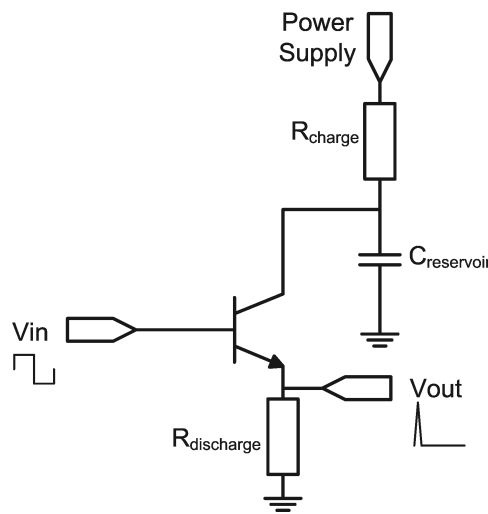
Figure 2.11: Charge based pulse generator

In this figure, the charge reservoir is implemented as a capacitor $C_{reservoir}$, which is connected to ground via a bipolar transistor and a resistor $R_{discharge}$. A DC voltage source is slowly, but constantly, charging the capacitor through a very large resistor R_{charge}. This resistor isolates the voltage source and the rest of the circuit. A pulse closes the switch (the transistor) and the capacitor is discharging via the transistor into the load. If the switch remains closed after the pulse has passed, a small current, defined by the resistor R_{charge}, leaks through the switch. After a while the switching transistor opens again and the capacitor charges again, resulting in a rise in collector voltage.

The major drawback in this circuit is that, in order to have a high voltage output, the supply voltage has to be high enough, as there is no multiplication gain as in a transformer. Also the amount of charge has to be high enough compared to the load resistance and the charging capacitor needs to be able to endure the high DC-voltage when the switch is open.

As this circuit performs well, contains only standard components, is easy to make and provides single sided pulses, this method was chosen as a basis for pulse generation.

2.3.1.3 Avalanche discharge pulse generator

This generator's schematic is displayed in Figure 2.12. As indicated, the supply voltage is very high (+145 V), driving the bipolar transistor in its avalanche region. This region is characterized by avalanche breakdown. In the forward active operating region, electron-hole pairs are generated due to thermal energy. If there is a voltage gradient over the semiconductor, the electrons will move according to that gradient. If the voltage gradient is very large, these electrons rapidly gain speed, moving fast enough to 'knock' other electrons free, creating new electron-hole pairs. This results in a sudden increase in current, thus an increase in transistor speed. This makes this region very suited for high voltage pulse generation with very short rise times [15].
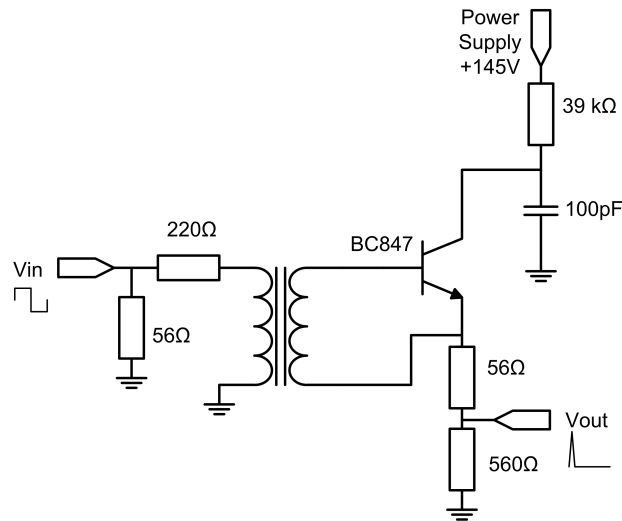
Figure 2.12: Avalanche discharge pulse generator

As the avalanche region of a transistor covers a fairly large voltage range, an optimal bias point needs to be derived. It can easily be deducted that there is a direct connection between the collector-emitter-voltage and the rise time and voltage level of the output pulse. If this initial voltage is higher, a stronger electric field is present within the transistor. This results in a higher carrier speed and a higher kinetic energy of the carriers, which

on its turn results in a more pronounced avalanche effect. Still there is a voltage limitation that has to be taken into account. If the electric field is higher, the transistor becomes much more sensitive to the base voltage. If the collector-emitter-voltage reaches a certain level, thermal noise in the base region of the semiconductor is instigating avalanche breakdown. This voltage level is transistor dependent. Below this level the avalanche breakdown can be controlled by operating the transistor base. Above this level, avalanche breakdown happens at random intervals, even if the base voltage remains low, and therefore no current is to be expected. Consequently the capacitor is constantly charging, up to the random moment when an avalanche breakdown happens. As in the pulse generator the timing of the pulses has to be deterministic, the collector-emitter-voltage must not rise above the self-exciting level. Therefore the optimal supply voltage is a few volts below that level. Throughout the remainder of this chapter, this voltage level will be called the random breakdown level.

One of the major drawbacks of avalanche operation is that it can be fairly destructive for most bipolar transistors. Therefore some transistors have been optimized for operation in this region. These have been named avalanche transistors. Still there are bipolar transistors which, depending on the manufacturer, can operate in their avalanche region, although they are not categorized as avalanche transistor. One of those transistors is the BC847 from Siemens, now Infineon [16]. This transistor was used in the pulse generators presented in this work. Measurements show that the random breakdown level is situated around 147 V. Therefore, the power supply has been set at 145 V.

The two resistors at the input provide an input match to 50 Ω, while the resistors between emitter and ground provide an output match to 50 Ω. While the transistor is in its conducting region, so low impedant, there is mainly a low output impedance visible. To obtain better matching, a resistor was added in series until no reflections were visible on the transmission line. The input signal is a square wave with a peak-to-peak voltage of 1 V, and can be generated by standard lab equipment. In this test setup a HP33120A 15 MHz arbitrary waveform generator was used to generate these square waves. The period of the input square wave is directly converted in a pulse repetition rate, while the rise time of the output pulse is defined by the avalanche operation.
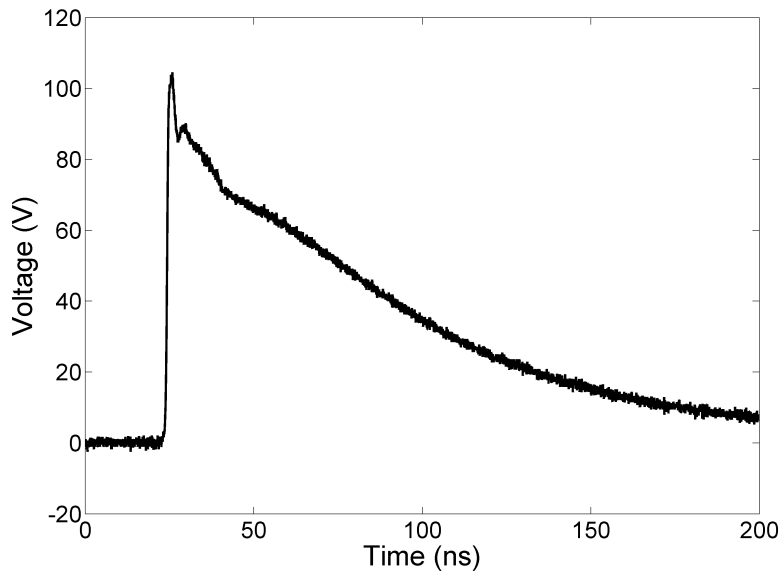
Figure 2.13: Output avalanche discharge pulse generator

The output signal of this high voltage pulse generator is shown in Figure 2.13. The input impedance of the measurement circuit was 2 kΩ. The measured peak voltage is over 100 V and the rise time is about 500 ps. The pulse has a length of about 150 ns and can be generated with repetition frequencies up to a few kHz without noticeable waveform change. This circuit has as extra advantage that the timing is very predictable. No jitter was perceived in the output signal, when triggering on the input signal during pulse generator measurements.

In some applications it might be interesting to know that the waveform can be adapted by changing the shape of the charge reservoir. In this case a 0603 100 pF capacitor has been used, which results in a discharge pattern of a capacitor by a resistor. If this reservoir is shaped like a transmission line, e.g. a coax cable, the resulting output waveform is a reflecting square wave [17]. If the characteristic impedance of the line is chosen well, a high voltage square wave is generated.

If the charge reservoir is large enough, the output peak voltage is limited by the power supply voltage, and consequently by the random breakdown level of the transistor. For some applications, this voltage is too low. In order to allow a rise in supply voltage without requiring another transistor, the transistors can be put in cascode as indicated by transistors T_2 and T_3 in Figure 2.14 [18].
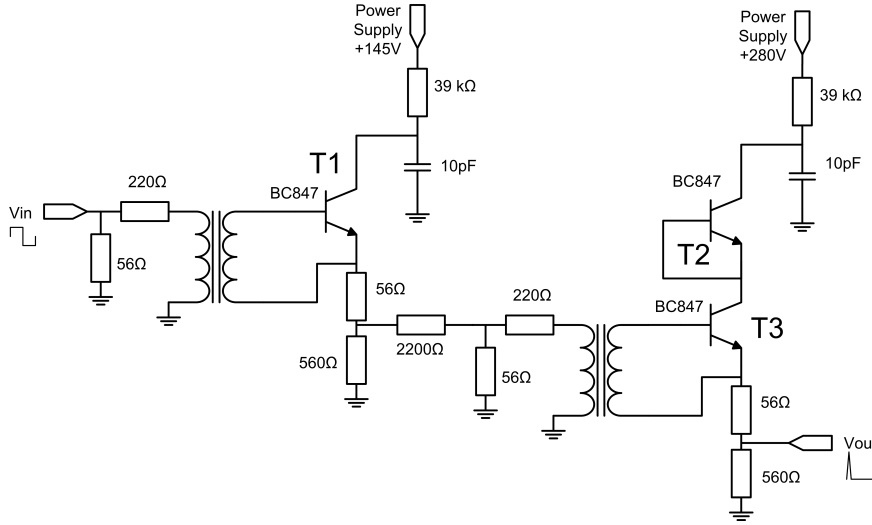
Figure 2.14: Avalanche discharge pulse generator with high voltage extension

When V_{BE3} is low, both transistors are in cut off and the supply voltage is divided over both transistors. This way each transistor has a V_{CE} of half of the supply voltage. This way the supply voltage can be augmented over a large range without going over the random breakdown level of each transistor. When V_{BE3} goes up, transistor T_3 will start conducting, V_{CE3} becomes low and avalanche breakdown will occur in T_2. In order to keep the average output power low, thus protecting the circuit itself, the DUT and laser driver, V_{BE3} must only become high for a very short time, e.g. the duration of the pulse itself. Therefore V_{BE3} is driven by another avalanche discharge pulse generator. This is the circuit around T_1. The output signal is given in Figure 2.15.
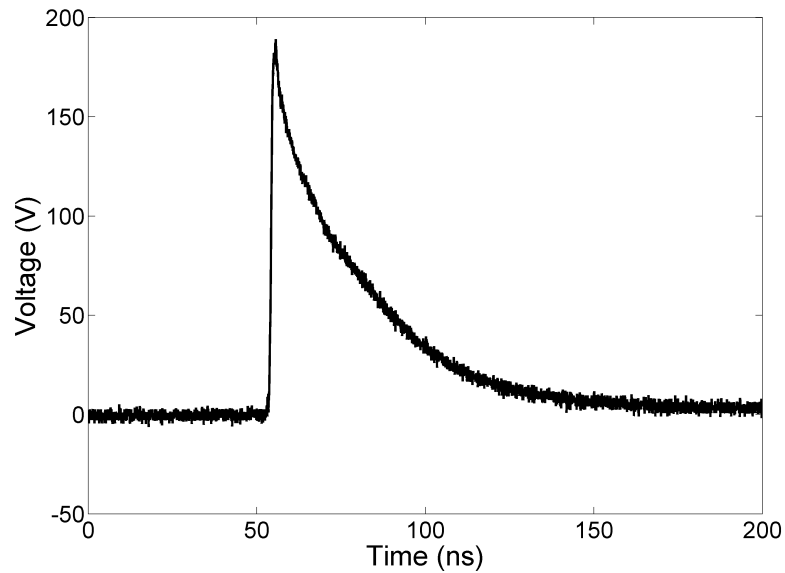
Figure 2.15: Output avalanche discharge pulse generator with high voltage extension

This circuit clearly has the advantage that it generates pulses with a higher peak voltage with a rise time of 1 ns. The major drawback is that there is more jitter on the start time of the pulse, which results in less predictability.

In this test setup, the test pulses have been generated by the avalanche discharge pulse generator depicted in Figure 2.12, as its peak output voltage is high enough and the timing of the output pulse is more predictable, and consequently repeatable. This can be an advantage if averaging is required.

2.3.2 Proof-of-concept voltage measurement module

The voltage measurement module consists of a laser diode, a bias circuit and a laser driver.

2.3.2.1 Laser diode

The first important question is which type of laser is to be used in the module. After a thorough survey of the available laser types, the Vertical-Cavity Surface-Emitting Laser (VCSEL)-type (pronounced 'vixel') has been chosen. As the name suggests, the VCSEL emits the laser light from the surface of a wafer, as opposed to standard edge-emitting semiconductor lasers.

VCSELs are very efficient electro-optical converters. They have relatively low threshold currents in the order of 5 mA, consume little power and generate less heat than standard semi-conductor lasers. This provides improved device lifetimes. VCSELs are relatively easy to manufacture and package. In opposition to edge emitting laser types, VCSELs can be tested after multiple manufacturing stages, providing a higher yield, and a lower cost. Above threshold, VCSELs have an input impedance which is almost constant and in the 40 Ω to 200 Ω range [19]. This impedance is much higher than impedances of other standard laser diodes. This is an important property in this application as this makes laser driving with voltage signals easier. Another major advantage of VCSELs is that, where the output light of edge-emitting lasers can be slightly astigmatic, this is not the case with VCSELs. A VCSEL produces a low divergence circular beam which allows for easy and efficient coupling to a fiber [20].

VCSELs are currently available for different wavelengths of which 850 nm is mostly used, although some manufacturers also provide 1310 nm and 1550 nm VCSELs. For 850 nm, VCSELs with bandwidths up to 10 GHz are no exception. In this work, the Raycan RC14xxx2-F 850nm VCSEL has been used [21]. This VCSEL is designed for high speed, high performance communication applications. It supports data rates up to 10 Gbps and therefore has a bandwidth exceeding 5 GHz. The major disadvantage of using a laser for analog modulation, is that these lasers are usually used for digital communication, and almost no analog specification is provided. Therefore these characteristics need to be measured. The DC-characteristics of this VCSEL are presented in Figures 2.16 and 2.17.
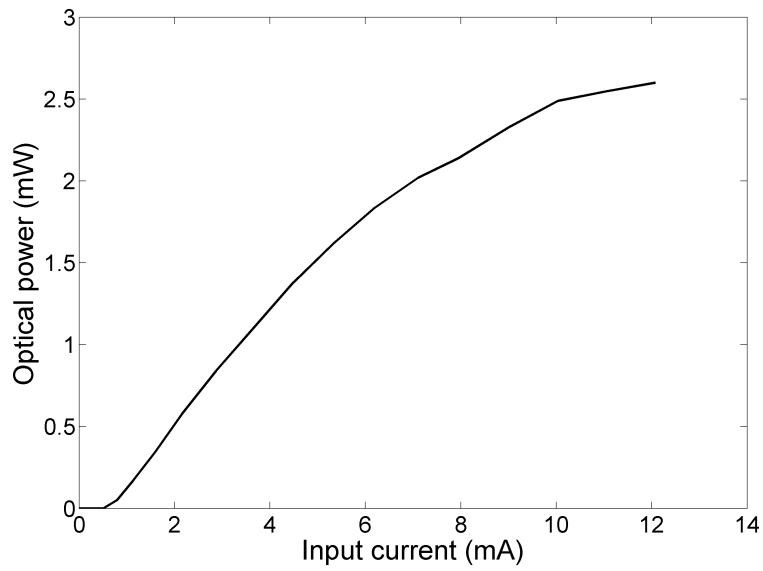
Figure 2.16: Measured DC-PI-characteristic of the Raycan RC14xxx2-F 850nm VCSEL
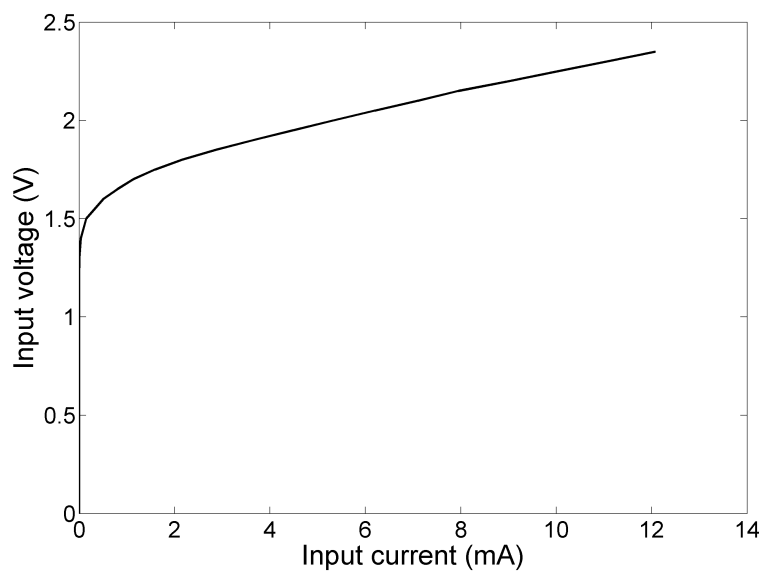
Figure 2.17: Measured DC-VI-characteristic of the Raycan RC14xxx2-F 850nm VCSEL

The threshold current is about 1.5 mA. The forward voltage at this point is 1.7 V. In the region above threshold level, the input impedance varies between 45 Ω and 100 Ω. This region is limited to a maximum forward current of 12 mA. Another important value is the maximum reverse voltage as lasers are very sensitive to this value. This VCSEL can stand a reverse voltage of 5 V.
These VCSELs are available in multiple packages:

- TO-CAN package pigtailed to multimode fiber

- 4-channel array

In this test setup, the pigtailed version has been used. This way, no attention needs to be paid to laser alignment. In the future, the 4-channel arrays can be used instead to monitor multiple signals at the same time, e.g. current and voltage.

2.3.2.2 Laser driver and bias circuit

As explained in section 2.2, the optical modulation measurement architecture uses a small communicating module for signal capture. This module consists of a laser chip and a laser driver with bias circuit. To make a robust module, this circuit will consist of the minimal number of components required in order to bias the laser, and to attenuate the high input voltage to a voltage level in the linear input range of the laser diode.

Figure 2.18: Simple laser driver circuit

A very basic circuit that can provide the required laser bias and attenuation functionality is depicted in Figure 2.18. As the input impedance of

a VCSEL is fairly constant above threshold, the attenuator can be implemented by means of a resistive voltage divider. The lack of active componen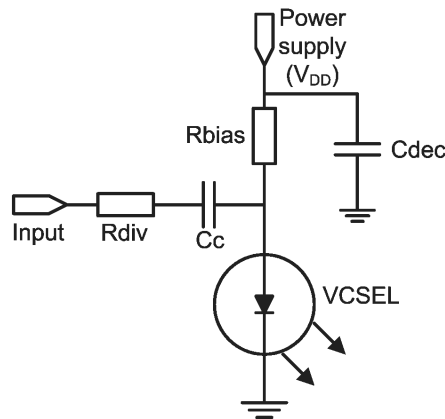ts in this circuit ensures a high linearity. In Figure 2.18, this is implemented by means of the VCSEL and a single resistor. To prevent the input signal from changing the laser bias setting, this input signal is AC-coupled before reaching the laser diode. To isolate the power supply from the VCSEL in AC, a resistor is used. As the ESD-signal is a broadband signal, and each inductor has a limited frequency range and a limited quality factor, it is much harder to make an inductor based bias tee. A resistor however, although it has the disadvantage of introducing a DC-voltage drop, has a much higher bandwidth, therefore its use is preferred. The bias current I_{bias} is externally controlled via the supply voltage V_{DD}. Its value is presented in equation 2.6 in which V_{VCSEL} represents the bias voltage across the VCSEL. An extra advantage of AC-coupling of the input signal is that it allows for measurements of both positive and negative pulses.

$$I_{bias} = \frac{V_{DD} - V_{VCSEL}}{R_{bias}} \qquad (2.6)$$

Because of the susceptibility to parasitic effects, high impedance nodes are better avoided in high frequency circuits. Also, the input resistor value of the voltage divider can become very large for very high measurement voltage levels. This is why this resistor of the voltage divider is better replaced by a resistor ladder network, as is depicted in Figure 2.19.
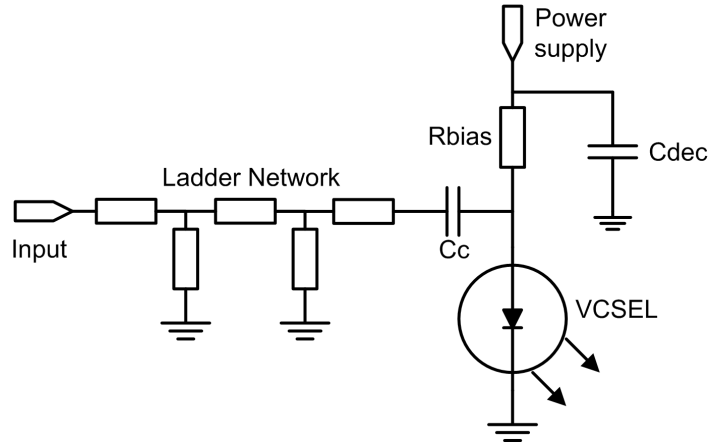

Figure 2.19: Laser driver circuit with resistive ladder network

This provides a large attenuation, while maintaining a low impedance in each node. The limiting factor of such a resistor ladder network is the

fact that the majority of the input power is dissipated in the first step of the ladder. As the module needs to operate in a frequency range up to 5 GHz (section 2.1), only on-chip resistors or discrete resistors with very small dimensions, e.g. 0402 or smaller, can be used, as these generally show the best high frequency behaviour. If the power dissipation in these components is limited, e.g. to 50 mW, and the maximum input voltage is 80 V, a low impedance ladder network can't be used. As the instantaneous power dissipated in the first step is very high, but the average power is very low, it can be expected that the resistors can take a much higher peak dissipation than the value mentioned in the datasheet. Once the module was assembled, some stress tests were done to make sure that the attenuator could stand the target pulses.

This section presents the derivation of the laser driver circuit component values. The laser diode has to be driven in such a way that it remains linear. Therefore it needs to be biased above threshold, and the deviation of the signal around this bias point needs to be small. To do this, it is important to look back at the DC-characteristics of the laser diode in Figure 2.16. In the test setup, the bias current was set at 3 mA and the maximum signal current modulation is set at 2 mA. The expected input voltage range was between 0 V and 100 V. The coupling capacitor can be adjusted to change the high pass corner frequency. In this test setup, this frequency is set at 150 kHz. This results in the values in Figure 2.20. If another input voltage range is of interest, the resistor values can be changed accordingly.
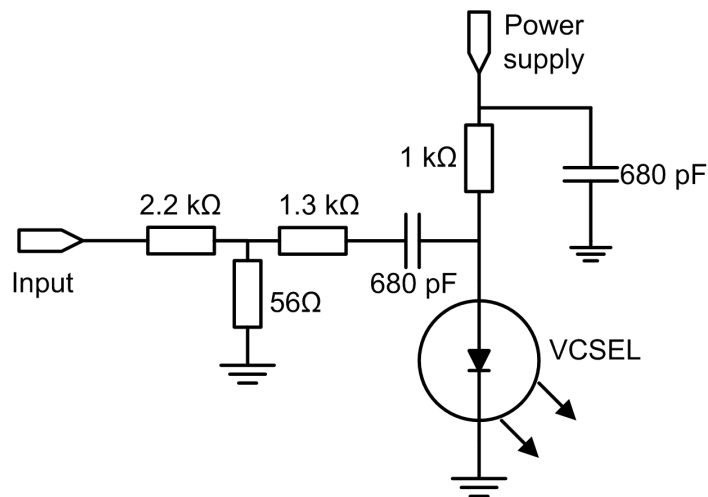
Figure 2.20: Laser driver circuit with component values

2.3.2.3   Measurement module realisation

On a single layer Printed Circuit Board (PCB) with a 1.5 mm Flame Retardant 4 (FR4) substrate, two versions of this measurement circuit have been implemented. The only difference is the size of the resistors and capacitors used, which are 0402 and 0201. Both versions have their own SMA input connector, VCSEL protection diode, VCSEL and supply connectors. In Figure 2.21, the layout of the PCB is shown. In this picture, white and blue represent top layer metal, where white indicates that the metal piece is part of a component layout cell, while black indicates lack of top layer metal. A conducting plane is connecting all ground pins of both versions, providing a low impedance ground. This plane is obstructed near the attenuation resistors to minimize the capacitive coupling across these resistors. The VCSELs are pigtailed to a multimode fiber, provided with an FC-connector. This way the module can be easily coupled to a photodetector.

Both implementations were put to a stress test, where pulses with a peak voltage of 200 V were generated at repetition rates of 1 kHz during 24 h. No behavioral change was measurable at the end of each test. The test results that are presented in section 2.4 have been obtained by testing the 0402 implementation [22].
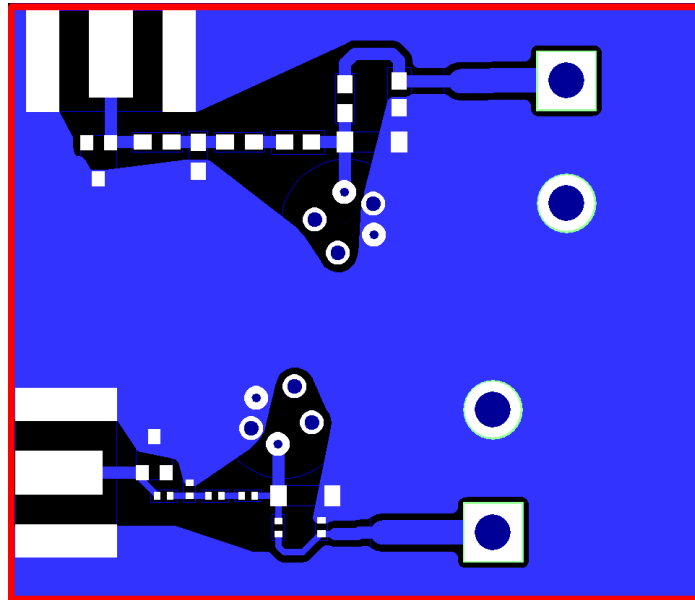
Figure 2.21: PCB layout with a 0402 and 0201 version of the proof-of-concept voltage measurement module

2.3.3 Photodetector

For conversion of the optical to electrical signals, a photodetector with a very high bandwidth is required, and which is sensitive to light with a wavelength of 850 nm. In this setup an UPD-30-VSG-P ultrafast photodetector from Alphalas was used (Figure 2.22) [23]. This biased photodetector has a spectral range of 320 nm to 900 nm and a quantum efficiency of 40%. It also has a bandwidth of 10 GHz and a rise time of less than 30 ps. In order to maximize the received signal power, the sensitive area of the photodetector needs to be larger than the core diameter of the optical fiber. Therefore the diameter of the photodetector needs to be as large as possible. In this case the photodetector has a sensitive area of 0.04 mm^2 which is fairly large for 10 GHz photodetectors. This photodetector has an SMA-connector output. This way it can be connected to an input port of a measurement device or broadband low noise amplifier.
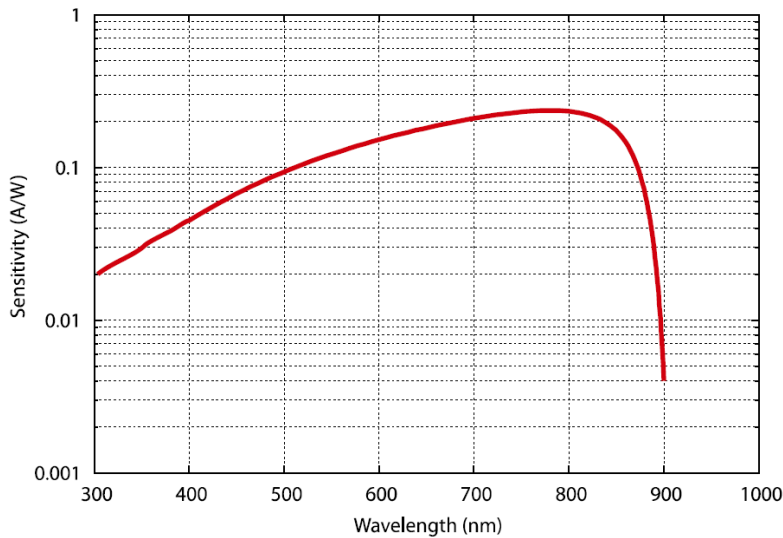
Figure 2.22: Spectral response GaAs Schottky photodetector: UPD-30-VSG-P

2.3.4 Oscilloscope

In this test setup a 20 GSps Tektronix TDS7404 Digital Phosphor Oscilloscope takes care of the waveform reconstruction. It has a bandwidth of 4 GHz and a 50 Ω input impedance [24].

2.4   Voltage measurement results

As explained in section 2.3.1, an avalanche discharge pulse generator was used to generate broadband, high voltage pulses. The voltage waveform of such a pulse is, for comparison purposes, presented again in Figure 2.23.
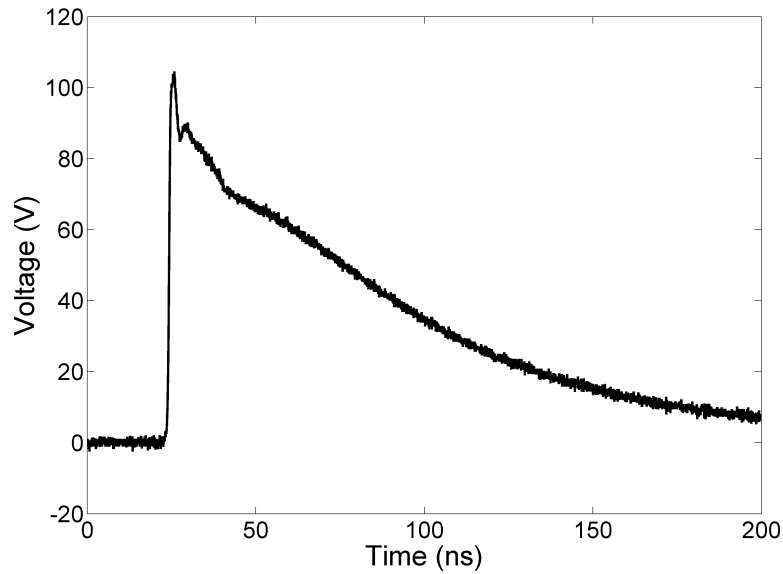
Figure 2.23: Output avalanche discharge pulse generator

The reconstructed voltage waveform of this pulse is presented in Figure 2.24. The input waveform can be recognized in the output waveforms. Still the signal has a low SNR. If for comparison purposes the output signal is averaged 10 times by the high speed sampling scope, the waveform presented in Figure 2.25 appears.
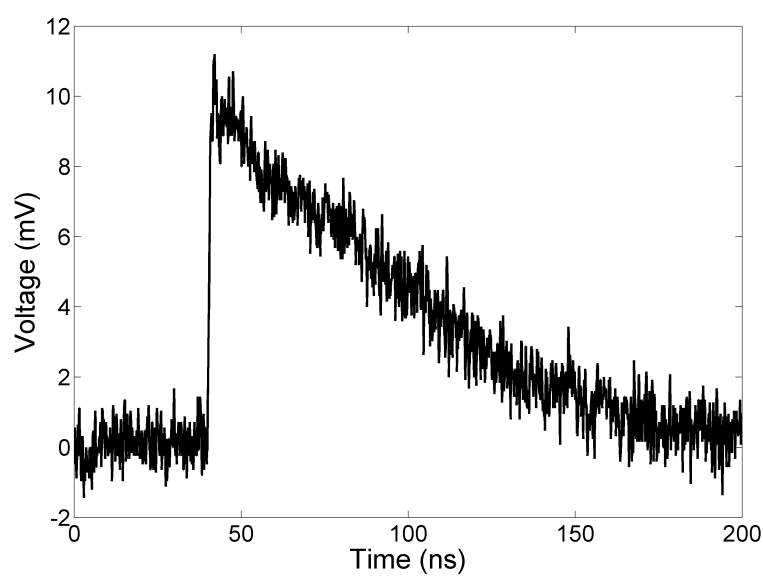
Figure 2.24: Reconstructed voltage waveform
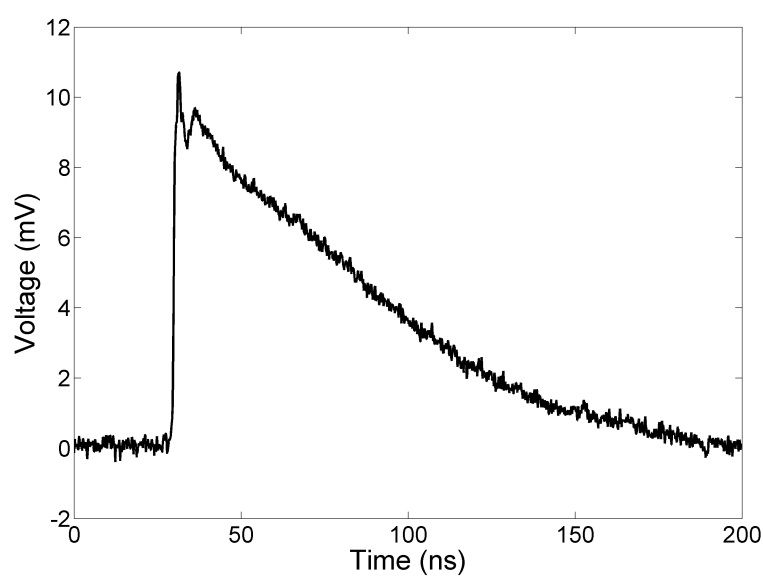
Figure 2.25: Reconstructed voltage waveform (10x averaging)

2.5   Evaluation of the measurement results

A comparison of the waveforms in Figures 2.23, 2.24 and 2.25 leads to the following conclusions:

- The waveform is transported to the oscilloscope without major distortion.

- The output signal is slightly deformed due to the non-perfect frequency characteristic of the measurement solution. The fact that the measured pulse tail drops below zero, while this isn't the case for the input pulse, is a clear indication of AC-coupling in the lower frequency range.

- The signal-to-noise ratio needs to be improved in order to meet the single shot measurement requirements.

In this section, these problems will be analyzed in depth and appropriate solutions will be proposed.

2.5.1   Frequency dependence

In this paragraph possible channel characterisation techniques are proposed. This channel information is used to compensate for the frequency response of the measurement solution.

The frequency dependence of the measurement solution is easily derived through network analysis. A well known test signal is sent through the DUT. At the output, the resulting signal is then compared to the original signal. The easiest way to obtain the frequency response of a channel is by inserting a sine wave with known frequency, phase and amplitude at the input of this channel. If the channel behaves in a linear way, another sine wave with the same frequency appears at the output. If phase and amplitude of both sine waves are compared for each test frequency of interest, the linear, time-invariant channel is completely defined. This method is implemented in any vector network analyzer.

The signal processing becomes much more complicated in the case of a non-linear channel. Each output signal can be written as a series expansion of the corresponding input signal, with channel dependent coefficients. These coefficients can be obtained through comparison of the input and output signals. Again, a sine wave is used at the input, which results in a sum of sine waves at harmonic frequencies. If the sine wave is again swept through the frequency domain of interest, the non-linear, time-invariant channel is

completely defined. Nowadays, this feature is implemented in the more advanced vector network analyzers [25].

However, in many cases, the channel behaves just slightly non-linear. Even a non-linear device has a linear characteristic in a small region around the bias point. This means that if the input signal is small enough, this linear characteristic can be used. This is the case in the measurement solution. A laser diode has a non-linear power-current characteristic, but the laser is driven by a sufficiently small input signal superimposed on a bias current. In this input range, the device still behaves in a linear way. As an ESD-pulse can have a large amplitude, an attenuator is required to reduce the pulse until it fits in this linear region. This way standard vector network analysis can be used to define the frequency characteristic of the measurement solution.
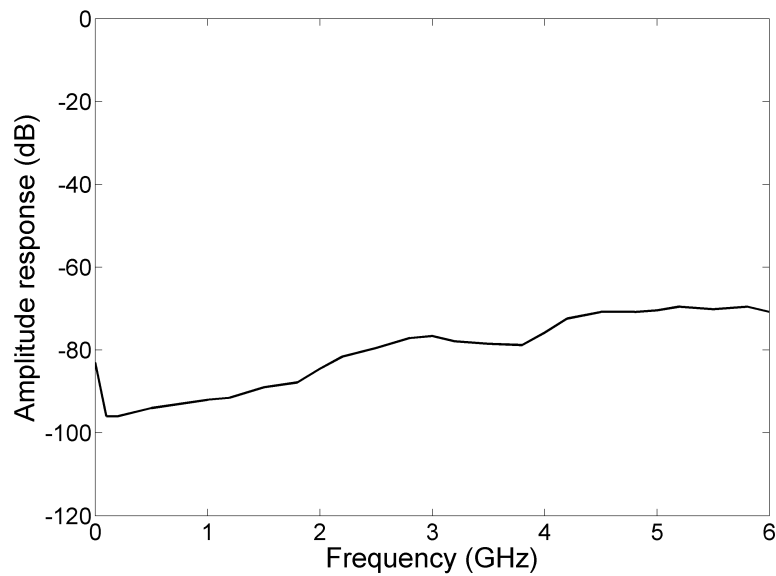
Figure 2.26: Amplitude response attenuator and optical link

In Figure 2.26 the amplitude response of the measurement solution is depicted. Not only the large attenuation of about 90 dB, but also a high pass filter response is visible. This decrease in attenuation can be explained by the parasitics in the attenuator. This frequency dependence can be compensated by applying the compensation filter obtained by calibration to the measurement signal.

In this test setup, it is easy to insert a sine wave at the input of the measurement solution. In some future miniature implementations this may not be the case. As the module can be directly connected to the DUT, it may be that the ESD-input is the only input available for testing. As only a limited power is allowed to prevent destructive heating, the amplitude of the test sine wave will have to be small to prevent destruction of the DUT. Such a sine wave at the input will in that case not trigger the ESD-protection and not provoke any change at other points of the ESD-protection structure. In this case channel characterisation by means of a step response will have to be used. This way, even for very strong pulses, the average power dissipation is low. Each linear, time-invariant and stable channel can be characterised by its step response. This step response can easily be obtained as a TLP-generator, a commonly used device for ESD-characterisation, generates rectangular pulses with well known characteristics [26]. These pulses have a large instantaneous power and trigger the ESD-protection, resulting in a signal at the input of the measurement module.

2.5.2   Signal-to-noise ratio

The specifications derived in section 2.1 require a measurement dynamic range of 35 dB, which corresponds for the ESD voltage signal depicted in Figure 2.1 to a SNR of 25 dB. This is obviously not the case in the measurement results discussed in section 2.4. In this paragraph, the reason for this low SNR will be reported and a solution proposed.

Signal-to-noise ratio is the ratio of useful signal power and noise power in a signal. This can mainly be increased by increasing the useful signal power, reduction of the noise bandwidth and reduction of the spectral noise density.

2.5.2.1   Noise Bandwidth

In a frequency range of almost DC to a few GHz, the most significant part of the noise power comes from thermal noise which is approximately white. As the noise spectral density is nearly flat, the total amount of noise power is directly proportional to the measurement bandwidth. As described in section 2.1, an ESD-signal has a very broad bandwidth as it contains frequency components below one MHz up to a few GHz. Reduction of noise bandwidth will result in the loss of important measurement signal information. Although the noise bandwidth is very large, this is not a parameter that can be changed to increase the SNR.

2.5.2.2 Transmitted optical power

Although ESD-pulses have a large amount of instantaneous power and consequently a very large SNR, this pulse needs to be attenuated to make transportation to and further processing by the waveform reconstruction device possible. If the attenuation is lower, there is a larger signal at the input of the laser diode, which results in more optical power and a larger signal-to-noise ratio. The maximum amount of optical power is limited by the characteristics of the VCSEL. In Figure 2.27 the DC-PI-characteristic of the selected VCSEL is shown again.
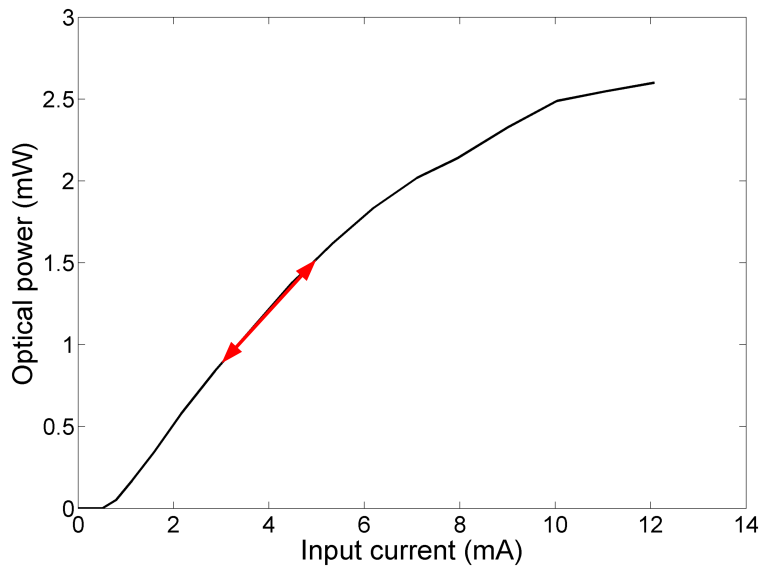
Figure 2.27: DC-PI-characteristic Raycan RC14xxx2-F 850nm VCSEL

In the previous tests, the VCSEL was always biased with 3 mA, and the AC current swing was limited to 2 mA, as illustrated in Figure 2.27. This resulted in an optical power swing of about 0.5 mW. According to the datasheet of the VCSEL, the maximum forward current is 12 mA [21]. This corresponds to a maximum output power of 2.5 mW, so the maximum optical power swing is 2.5 mW, which is a factor 5 higher than what was used in the test setup. Using this maximum optical range can result in a maximum total SNR increase of 14 dB. However, in practice this number will never be reached as a safety margin has to be taken into account to prevent destruction of the VCSEL. Still a total SNR increase of 6 dB is possible.

However, a drawback of generating more optical power is a reduction of transmitter-linearity. A higher optical output swing requires a larger current swing at the VCSEL input. The VCSEL has a non-linear characteristic. This non-linearity can be characterised by means of harmonic distortion measurements. A sine wave is inserted into the laser input, which results in a sum of sine waves at the harmonic frequencies at the photodetector output. The ratio of the signal power of the first harmonic and the other harmonics, also called harmonic distortion, is a common measure for distortion of a system. In Figure 2.28, the 2nd up to the 5th order harmonic distortion are displayed for a standard linearity measurement value of 0 dBm electrical input power (in a 50 Ω environment) and multiple bias currents.
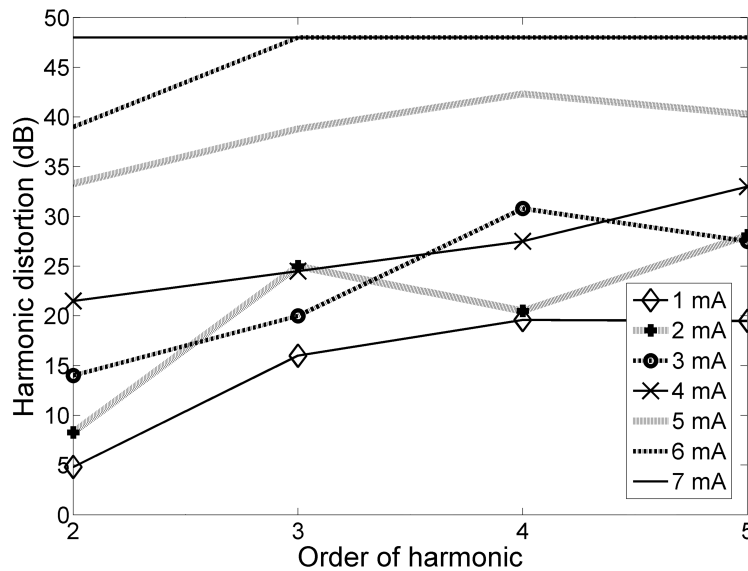
Figure 2.28: Harmonic distortion VCSEL at 0 dBm input power

It seems that only in the case of 6 mA and 7 mA bias current, the VCSEL has about 40 dB of second and third order linearity, which is good enough according to section 2.1. The reason can be found in the type of input signal. A 0 dBm signal was put in an input with an impedance of about 80 Ω, this corresponds to a sine wave with an amplitude of 0.4 V or a total swing of 0.8 Vpp. When this is compared to the DC-characteristics of the laser, the only measured bias current levels that are high enough for a range of 0.8 Vpp to be out of the non-linear region of the diode are indeed 6 mA and

7 mA. The limitation on the linearity comes from the diode threshold. This is confirmed by the oscilloscope measurement displayed in Figure 2.29, which indeed indicates that the non-linearity is caused by the lower region of the sine wave, which corresponds to the non-linear threshold region of the laser diode. Once the signal range is well above the threshold region, the required linearity is obtained. As the range of 0.8 Vpp around a bias of 7 mA corresponds to a current swing from about 2 mA up to 12 mA and as each range within this region has an equal or higher linearity, there is at least 40 dB of linearity in the range of 3 mA to 5 mA.
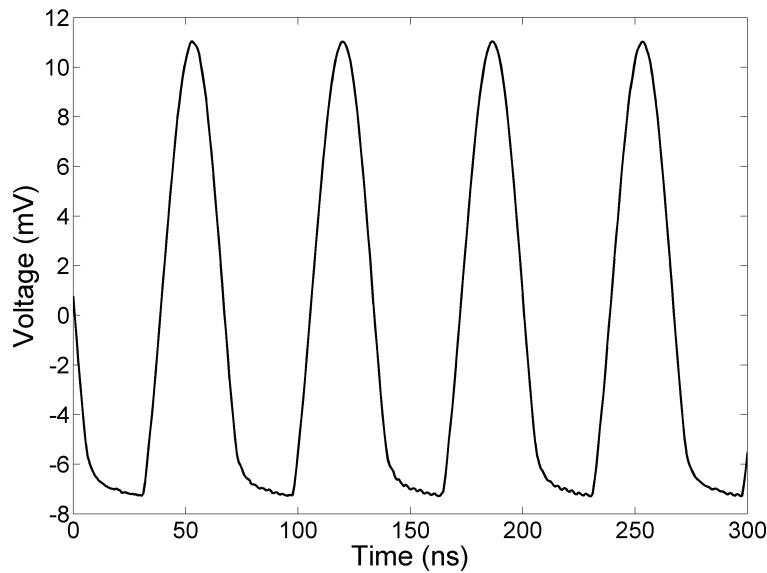
Figure 2.29: Oscilloscope measurement of the received sine wave showing non-linearities due to laser threshold

These linearity measurements also show that it is indeed possible to increase the optical signal power level by 6 dB without linearity problems. Still the question remains if a 6 dB SNR raise is enough. When looking at the obtained measurement results (Figure 2.24), it quickly becomes clear that this is not the case. A 6 dB rise in signal power corresponds to a doubled signal voltage range, which then becomes about 20 mV. If the noise voltage range remains 2 mV, there is at least 10% of noise. The SNR is still below 30 dB.

2.5.2.3   Signal-to-noise ratio at VCSEL input

The previous paragraph indicates that another measure needs to be taken for the SNR to rise above 30 dB. As a real system always decreases the SNR in the same frequency band, the low SNR at the measurement output can be caused by the optical link or it can already be insufficient at the VCSEL input. To rule out the second reason, the optical link was replaced by a coaxial connection. The measurement results that have been obtained with this coaxial test setup exceed the dynamic range requirements by more than 20 dB.

2.5.2.4   Signal-to-noise ratio at photodetector output
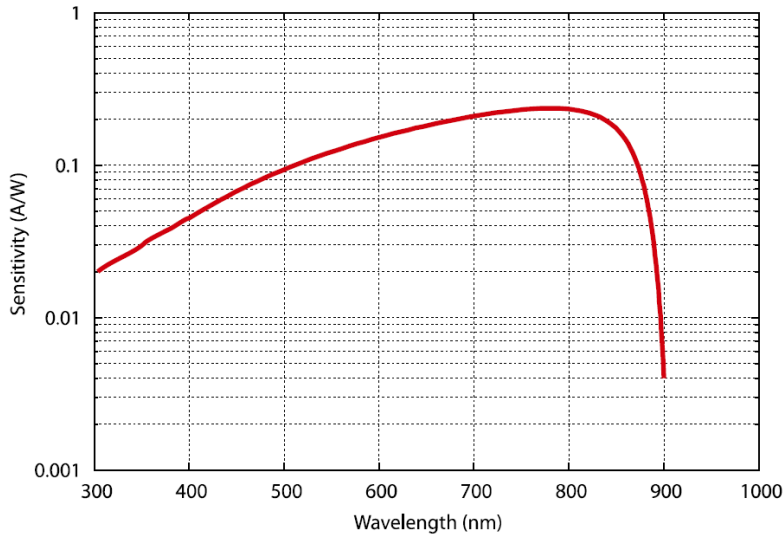
Figure 2.30: Spectral response GaAs Schottky photodetector: UPD-30-VSG-P

As the signal at the VCSEL-input has a sufficient SNR, the reason for the low measured SNR is in the optical conversion. The optical signal has a power swing of about 0.5 mW due to an input current variation between 3 mA and 5 mA. When looking at the spectral response of the UPD-30-VSG-P-photodetector (Figure 2.30), this corresponds to an output current swing of about 0.1 mA [23]. The waveform digitizing oscilloscope has an input impedance of 50 Ω. This results in a voltage swing of 5 mV at the input of the oscilloscope, which is too low as the oscilloscope has a noise floor of about 0.6 mVrms. Therefore, the measurements in Figure 2.24 were per-

formed with a 10 dB preamplifier before the oscilloscope. This resulted in a total voltage swing of about 15 mV. The preamplifier gain can still be increased, but the noise floor increases by the same amount. This is the amplified noise of the preamplifier (Noise Figure (NF): 6 dB). A photodetector with a higher transimpedance, so low current noise, is required to amplify the photocurrent.

To obtain a higher SNR, a new photodetector with integrated amplifier has been selected. The selected DC-coupled 1580-B photoreceiver module, distributed by Newport Corporation, has a bandwidth of 12 GHz, a 30 ps rise time and a typical responsivity of 400 $V/W_{optical}$ around 850 nm [27]. It has a noise equivalent power of 5 $\mu W_{optical}$ in a 10 GHz band. This is 40 dB less than the target 500 $\mu W_{optical}$ swing, which can be obtained by a 2 mA current swing in the VCSEL.

In this section the laser noise was not mentioned. This is because no noise specifications are mentioned on the datasheet, which can be understood as in most communication applications the amount of laser noise is negligible to the noise generated by the photoreceiver. It was experimentally verified (laser on/off) that the displayed noise is dominated by the photodetector and the oscilloscope.

2.5.3 Conclusion

Although the SNR of the measurement results of the first prototype is insufficient, these results clearly indicate that the chosen architecture can indeed be used to capture and to transport high voltage pulses out of an EMC-hostile environment. Also, solutions were proposed to increase the measurement SNR.

2.6   Extension to current waveforms

In this section, a current waveform measurement architecture is proposed. A good starting point is to look at the commonly known current measurement systems. A standard ammeter measures the current flowing through the meter. Therefore, the meter needs be placed in the circuit branch, through which the current of interest flows, which makes this measurement technique intrusive. Furthermore it needs to have an input impedance that is negligible to the impedance in series with the meter over the complete frequency range, in order not to influence the system.

Often the current measurement application makes it impossible to use an intrusive technique, e.g. if the current needs to be measured at a specific point, where opening the circuit would result in the destruction of the circuit-under-test. Several non-intrusive current measurement techniques are known. These are often based on magnetic coupling or on voltage measurements across a known circuit resistor. As already mentioned in section 2.2, this current waveform measurement system will use the second technique.

ESD currents can be very large, often in the range of Amperes. Even a small resistance (less than 1 Ω) can make the voltage high enough to perform current measurements. Such small resistances can be found in every circuit and are commonly known as conductors. In each branch of a circuit, a conductor can be found. This way, the current waveform can be calculated in each branch of any electronic system; at least, if it is possible to probe there and if the resistance value is known (e.g. via a four probe Kelvin setup). To meet this requirement, extra bondpads will be added at both ends of the conductor-under-test, or extra wide conductors can be used for direct probing.

2.6.1   Current probe architecture

Although the selected current measurement technique can be transformed into a voltage measurement technique, which can be realized by means of the voltage measurement solution, it needed to be investigated if this architecture can meet the current waveform measurement requirements.

As stated earlier, the current waveform will be obtained by means of a voltage waveform measurement across a conductor and a current waveform extraction technique. In order for this technique to extract the current waveform with the required accuracy, the voltage measurement needs to comply with certain requirements.
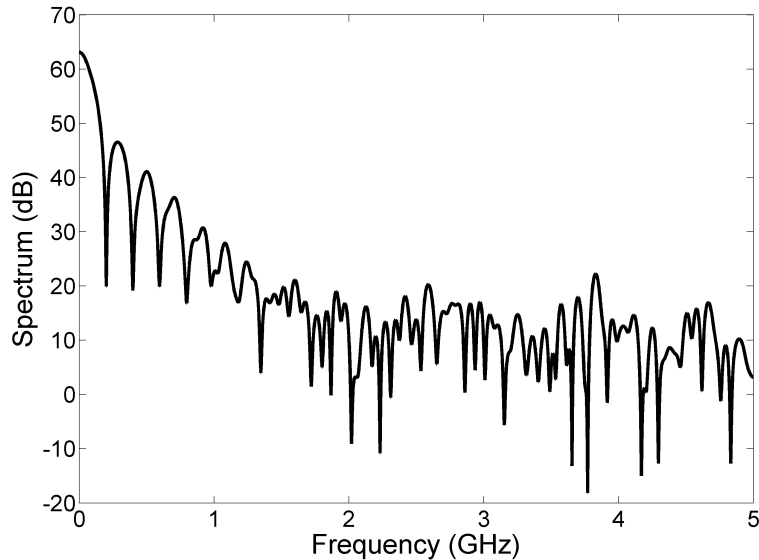
Figure 2.31: Spectrum of the incoming ESD current signal

The first specification is the bandwidth of the measurement device. To define the required bandwidth, the spectrum of the current pulse (Figure 2.31) was studied. It can easily be seen that the current bandwidth is about 1.5 GHz. This is lower than the bandwidth of the voltage pulse (5 GHz). This is caused by the dI/dt component in the voltage signal. If the voltage waveform measurement bandwidth requirements are met, the current waveform measurement bandwidth will be completely covered. The current pulse dynamic range is again about 40 dB.

An easy way to measure the voltage level across a conductor is by means of two voltage measurement devices with the same reference. The voltage waveforms, captured at both conductor interfaces, are transported to a dual channel high speed sampling oscilloscope, and sampled simultaneously. Then the difference of the two waveforms is calculated, which results in the voltage signal. This is a useful measurement technique in most applications. Still it has a major drawback as its useful dynamic range is limited by the input common-mode signal and the mismatch. In this ESD measurement application, the voltage across a conductor is measured, which, due to the high current, is large enough to measure (order of magnitude: 1 V). The same high current instantly charges the ESD protection circuit, providing a high common-mode voltage (order of magnitude: 100 V). Should this mea-

surement technique be used, about 40 dB of measurement dynamic range is used in common-mode signal measurement. A solution to this problem is to do the subtraction in an analog way, by means of a differential module with a sufficient CMRR [28].
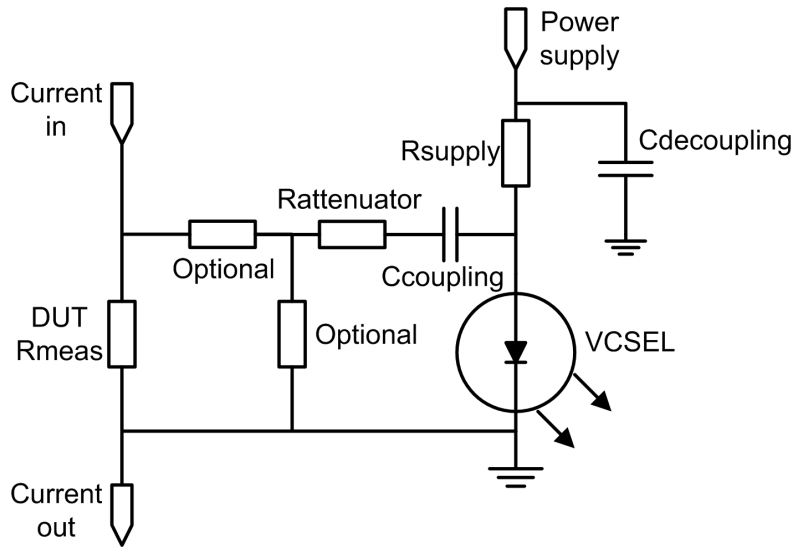
Figure 2.32: Adapted voltage measurement module

A differential module can be designed by adapting the voltage measurement module. Its schematic is presented in Figure 2.32. This differential module consists of the voltage measurement module as presented earlier in this chapter, but instead of using it in a single ended way, both input and ground pins are connected across the DUT, which is in this case a very small resistor. By changing the attenuator, the target voltage range can be set. There is only one drawback to this circuit; it can only be used if the ground pin is connected to a stable ground in the circuit. As this is a serious restriction, this differential module was further adapted into the full differential module presented in Figure 2.33.
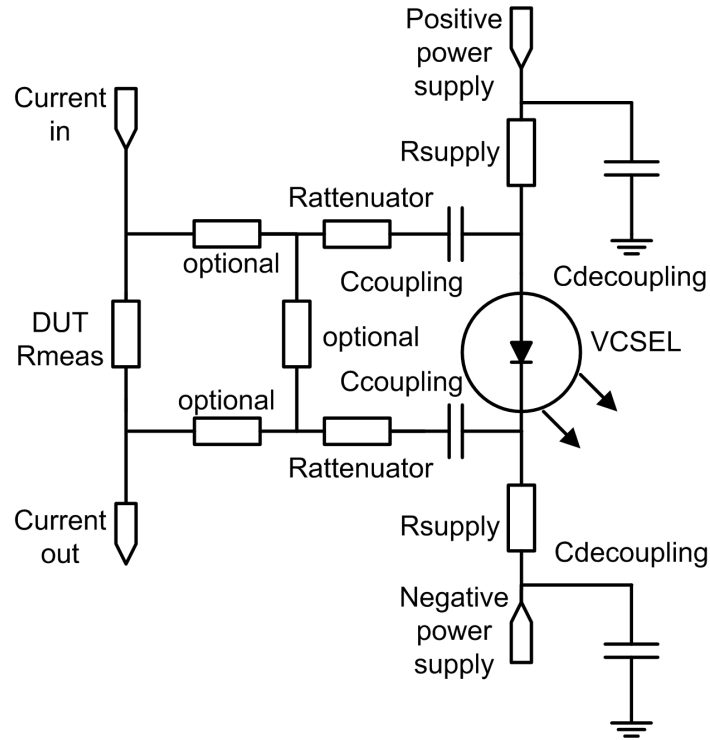
Figure 2.33: Full differential module

This differential module consists of a differential attenuator that is connected across the VCSEL via a pair of capacitors. To make the circuit completely symmetrical, the VCSEL is powered via a differential power supply and two equal resistors. This way the symmetry of the system is guaranteed.

2.6.2 Probe component values

In section 2.5, it was calculated that a VCSEL input current swing of 2 mA is a good compromise to meet the SNR-requirements. This means that 160 mV is the input voltage swing that needs to be used, as the VCSEL has an impedance of about 80 Ω.

In Table 2.2, the attenuation resistor values required to obtain a 2 mA VCSEL input current swing are calculated for multiple DUTs. As the attenuator is essentially a voltage divider, these values are current dependent. In these calculations, a current pulse with peak value of 30 A is used. The capacitor values in this table correspond to a cutoff frequency of 1 MHz.

The optional resistors in Figure 2.33 are not used.

DUT-Rmeas (Ω)	Rattenuator (Ω)	Ccoupling (pF)
0.2	1465	109
0.1	715	223
0.09	640	249
0.08	565	282
0.07	490	325
0.06	415	384
0.05	340	468
0.04	265	601
0.03	190	838
0.02	115	1384
0.01	40	3979

Table 2.2: Component values corresponding to resistive DUTs and a 30 A current pulse

An extra limitation on the measurement resistor is the linearity of the current output. Within the target input current range of the VCSEL, this device has a varying resistance between 70 and 80 Ω. In order to minimize the influence of this resistance variation, the attenuator resistance needs to be as high as possible compared to DUT R_{meas}. If this influence is to be limited to 1% or 5% a 0.07 Ω or respectively 0.02 Ω measurement resistor is at least required.

The use of low attenuation resistor values poses no isolation problem as the main isolating resistors in this circuit can be found in series with the power supply.

2.6.3 Common-mode rejection ratio

It was stated before that the CMRR is an important characteristic of a differential current probe. In this paragraph the influence of component tolerance on this CMRR is presented. In these calculations, the component values corresponding to a DUT of 0.05 Ω are chosen. To measure the CMRR, both probe inputs are connected to the same circuit node. This node is then connected to a 3.3 Ω test resistor through which a current pulse of 30 A flows. The probe asymmetry is implemented by using the maximum component value in the tolerance range in one branch of the attenuator, and the minimal component value in the other branch. This is the worst case scenario.

In the following paragraphs the CMRR is calculated by dividing the peak input voltage by the input referred peak voltage across the VCSEL. To obtain a better estimation, current pulse data, measured by our project partner, has been used to generate these results.

2.6.3.1   CMRR due to resistor tolerance
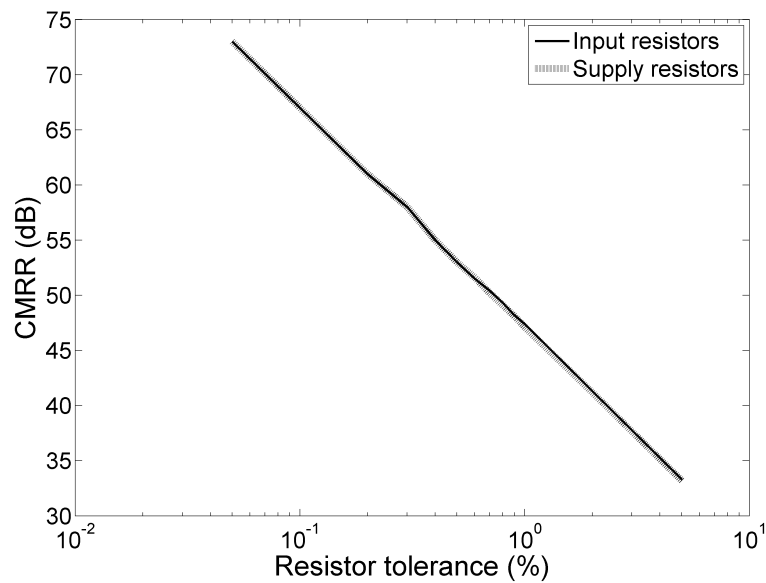
Figure 2.34: CMRR versus input attenuation and supply isolation resistor tolerance

Figure 2.34 shows the CMRR as function of attenuation and supply isolation resistor tolerance. This indicates that there is the same amount of influence of attenuation resistor and isolation resistor tolerance. If using resistors with 0.1% tolerance, a CMRR-value of 67 dB can be expected.

2.6.3.2   CMRR due to coupling capacitor tolerance

The CMRR due to coupling capacitor tolerance is presented in Figure 2.35. This figure clearly shows that the CMRR is less sensitive to coupling capacitor tolerance. Using capacitors with a tolerance of 1%, a CMRR-value of 78 dB can be expected.
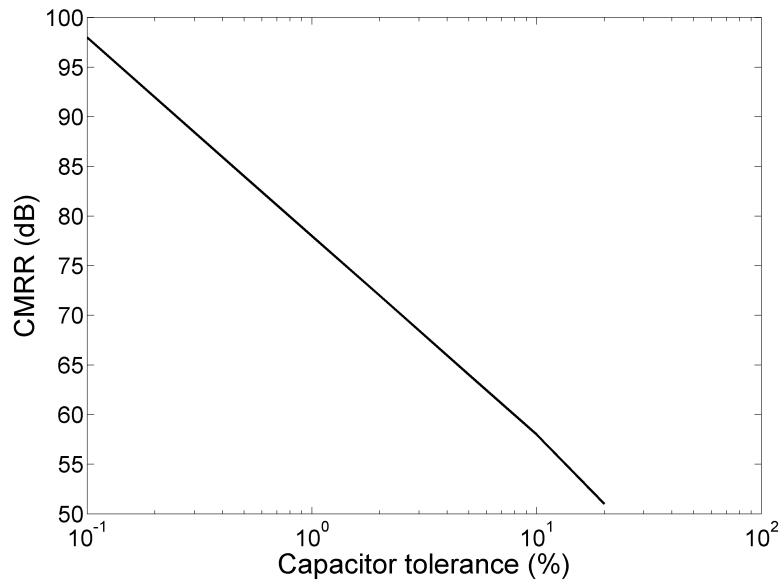
Figure 2.35: CMRR versus coupling capacitor tolerance

Considering process variations on both resistors and capacitors, a CMRR value of 60 dB is obtained if 1% tolerance capacitors and 0.1% tolerance resistors are used.

2.6.3.3   Parasitic capacitance tolerance

However, not only the components have a large influence on the common-mode rejection ratio, the same thing applies to board and assembly parasitics. To obtain an idea of this influence, a simulation result is shown in Figure 2.36. This is the result of an ideal system with 0.3 pF $\pm$ 10% parasitic capacitances to ground at each VCSEL-pin.

Figure 2.36: CMRR of an ideal system with 0.3 pF $\pm$ 10% parasitic ground capacitances at each VCSEL pin

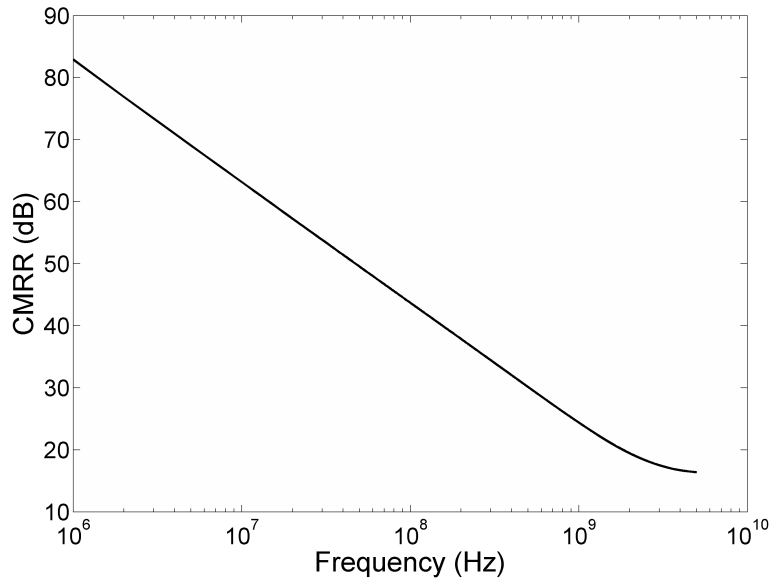Comparison between multiple CMRR-measurements shows there are two parasitic properties that directly influence the resulting CMRR: the mean parasitic capacitance, and the deviation on this value. The CMRR decreases when these properties increase. This way, it is clear that the used discrete passive components should be suited for operation in the RF-range. Another way to reduce parasitic capacitance is careful board layout, e.g. by using single layer layouts or removing the ground plane near high impedance nodes. The parasitic capacitance deviation can be reduced by using a symmetric board layout and careful PCB assembly. Still there is another limiting factor on the CMRR of a system: Electromagnetic coupling. This will be estimated in chapter 5. It is clear that careful module design and assembly are required to obtain a high CMRR in the ESD frequency range.

2.6.4 Current measurement through devices-under-test with resistive and inductive components

In the previous part, the DUT was assumed to be resistive. This means that the voltage across the DUT is directly proportional to the current flowing through the DUT. In reality, each conductor has a parasitic capacitance and parasitic inductance. The parasitic inductance provides an inductive voltage component that is directly proportional to the derivative of the current. As the rise time of an ESD-current is below one ns, while the current increases over multiple Amperes (e.g. for 1 nH, ΔI = 30 A and Δt = 1 ns, LdI/dt becomes 30 V). Even with a small inductive component, its contribution to the voltage across the DUT becomes non-negligible compared to the resistive part. This in contrast to the parasitic capacitance, of which the influence on the voltage level across the DUT is negligible compared to the resistive and inductive component (e.g. a current of 30 A can charge a 1 pF capacitance in 1 ns up to 30 kV. This means that only a negligible fraction of this current is used to charge this parasitic capacitance up to the voltage level of 30 V). There are multiple techniques that can be used to reconstruct the current waveform. These can be mainly hardware or software based. In this part, the following four current measurement techniques are shown:

- Inductive current probe

- Capacitive compensation

- Separation of inductive and resistive part

- Differential voltage probe and software calibration

2.6.4.1 Inductive current probe

There are a lot of commercial non-intrusive current probes available, most of them having the same architecture [29]. A core with a high magnetic permeability is closed around the conductor-under-test. Then a second conductor is wound around this core in order to have a sensitive measurement coil. This way the magnetic field of the conductor-under-test is concentrated in the core, and transformed into current in the measurement coil. This current is directly proportional to the current in the conductor-under-test. If the coupling factor is chosen lower and the number of measurement windings higher, a large current can be transformed into a lower current. This way a higher secondary resistor can be used, across which the voltage, which is directly proportional to the current, can be measured. The low
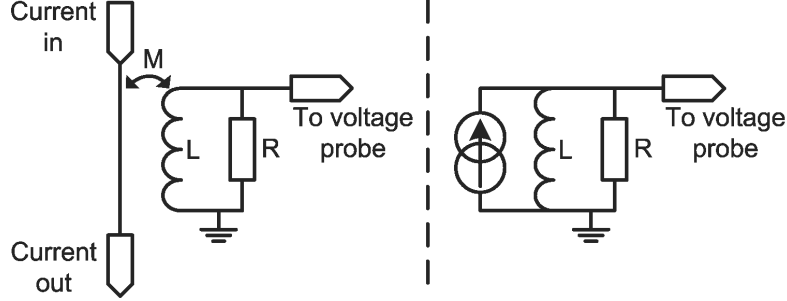
Figure 2.37: Inductive current probe and model

frequency response of the current probe can be compensated using extra information [30].

A System-ESD pulse has a frequency range between 1 MHz and 5 GHz. The measurement circuit should have the same frequency range in order for this to work. This frequency range can easily be calculated if the input magnetic field is modeled by a current source (Figure 2.37). The voltage across resistor R is then given by:

$$V = \frac{sRL}{sL + R}I = R\frac{s}{s + \frac{R}{L}}I \tag{2.7}$$

This transfer function corresponds to a high pass filter with cut-off frequency:

$$f = \frac{R}{2\pi L} \tag{2.8}$$

Even with a cut-off frequency of 1 MHz and a resistor value of 1 Ω, this results in an inductance of 160 nH, which is not feasible on chip with a resistance much lower than 1 Ω. An on-chip probe system based on this method is suited for pulses in the higher frequency range, but not for our requirements.

2.6.4.2 Capacitive compensation of an inductive device-under-test

A way of measuring the current via a differential voltage measurement device, is through compensation of the inductive part of the device-under-test. A simple pole-zero analysis shows that an inductive component can be completely compensated by means of a parallel resistor-capacitor-series circuit (Figure 2.38).
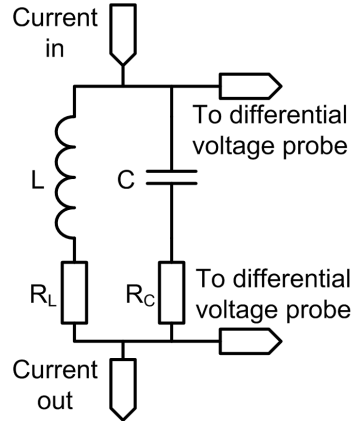
Figure 2.38: Capacitive compensation of an inductive device-under-test

Full compensation can be realised if:

$$R_C = R_L = R \qquad (2.9)$$

$$C = \frac{L}{R^2} \qquad (2.10)$$

The voltage across the compensation network is then R times the current through the network. If the voltage waveform across the compensated DUT can be measured in an accurate way, the current waveform is easily derived. Still there are some drawbacks to this compensation technique:

- This is a hardware compensation technique, using hardware adaptations to the system to compensate the inductive part of the DUT. If the DUT is changed, this will have its influence on the system response.

- Another drawback of this hardware technique is that both the resistive and the inductive part of the DUT have to be estimated very accurately during the design of the ESD-protection.

- This compensation is not always feasible, especially for low resistor values, as the capacitor value grows in a quadratic way as this resistance decreases. For a parasitic inductance of 0.1 nH and a conductor with 0.05 Ω resistivity, the compensation capacitance needs to be 40 nF with a resistance of 0.05 Ω. This is hard to obtain.

- This compensation circuit also has a parasitic inductance which has to be taken into account. As it crosses the same distance, this inductance can become equally large as the inductance to compensate.

As the required compensation circuit shows several drawbacks, another solution is proposed.

2.6.4.3 Isolation of inductive and resistive component

Another technique is to separate the inductive voltage contribution from the resistive voltage contribution. At this point, the parasitic inductance of the DUT is too large to be negligible, compared to its resistive part. If a resistor can be made with an increased resistive part while slightly increasing, or in the best case keeping the same inductive part, this inductive part can be made negligible. This way the voltage across the resistor can be measured, and the current waveform can be derived if the resistance is known.

This technique can be used to separate the inductive and the resistive voltage component across the DUT, even if the DUT is undividable in a resistive and a reactive part. To do this, a parallel path is added to the DUT. This path has an impedance of n times the DUT impedance and consists of an inductor and a low parasitic resistor. If the impedance ratio is chosen large enough, e.g. 100, the total parallel impedance is negligible compared to the impedance of the DUT. This technique is illustrated in Figure 2.39.
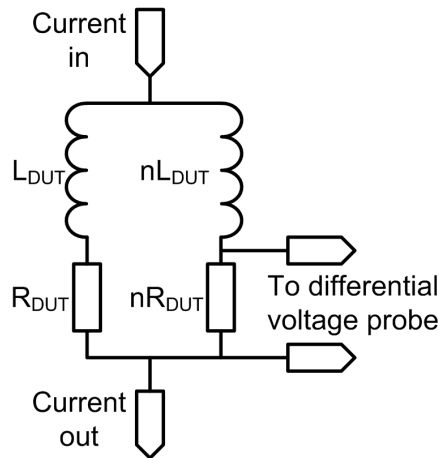
Figure 2.39: Circuit for isolation of inductive and resistive component

A DUT with an impedance of 0.05 Ω and 0.1 nH will need a parallel impedance of 5 Ω and 10 nH. If such an on-chip inductor can be made with a resistance less than 5 Ω, an extra resistor can be added in series. The voltage across this resistor can be measured, and the current through the resistor, and the current through the DUT, can be directly calculated. Again

the DUT has to be exactly known in order to keep the measurement errors small.

It is interesting to know what amount of misestimation results in what amount of error. Before answering this question, a means of waveform comparison is defined in the case of different waveforms. In order to have this figure of merit, the measured current waveform is multiplied up to the point that the current level of that waveform and the real current waveform through the DUT are equal at the end of the current pulse through the DUT. At this point the voltage across the DUT is mostly defined by the resistive part of the circuit as dI/dt is low. Then this resulting signal is subtracted from the current waveform through the DUT, which results in an error signal. The absolute maximum deviation of this error signal is then compared to the point of reference, which results in a number. This number is taken as measurement error. A point of reference can be found if the DUT is not compensated. This results in a measurement error of 260%. In Figure 2.40 this figure of merit is shown for inductive and resistive tolerances.
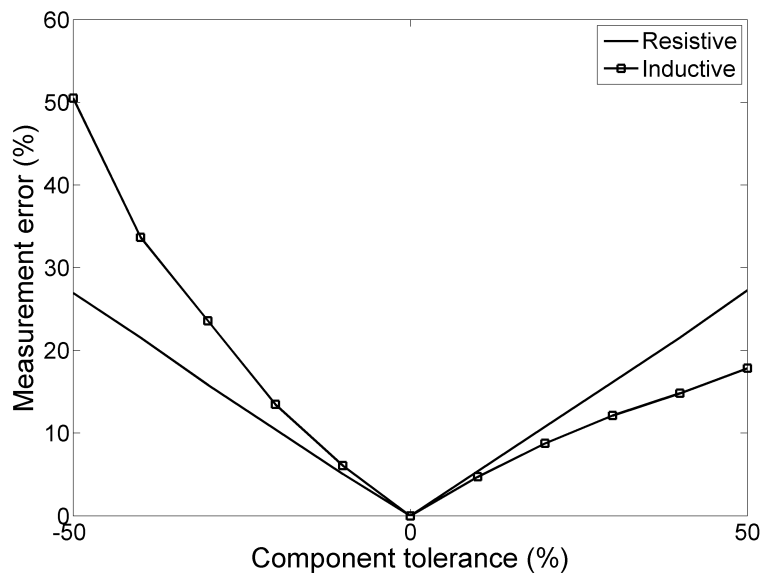

Figure 2.40: Measurement errors due to component tolerance

The component tolerance has a large impact on the total measurement error. This can be countered by using a system with software calibration. Such a calibration technique is presented below.

2.6.4.4 Differential voltage probe and software calibration

Another possible measurement technique is to measure the voltage across the DUT with the differential voltage probe, which has been presented earlier in section 2.6.1. Thereafter, the current waveform is derived from the voltage waveform by means of calibration parameters. These parameters are derived during a current probe calibration sequence.

The voltage waveform across the DUT consists of a resistive and an inductive component. This means that this voltage waveform can be written as a linear combination of the current waveform and its derivative. These waveforms are displayed in Figures 2.41 and 2.42.

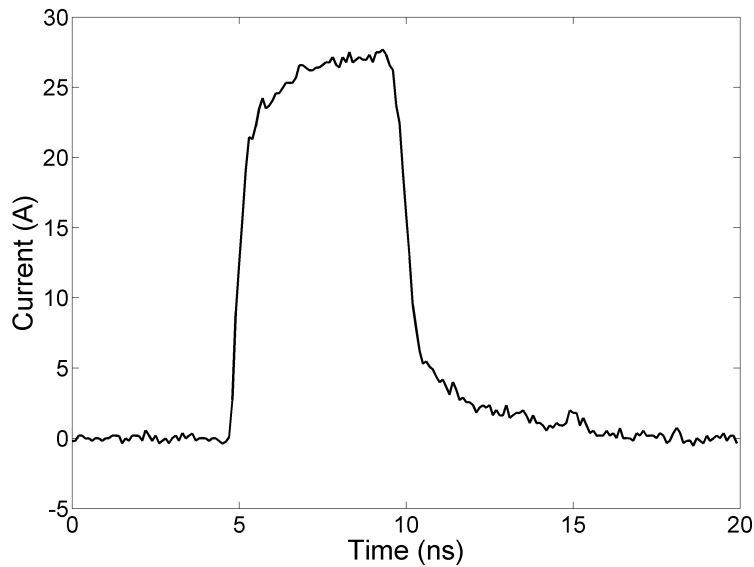Figure 2.41: Current waveform

The coefficients in that linear combination are respectively the resistance and the inductance of the DUT. The voltage waveform of a linear combination with coefficients 0.05 Ω and 0.1nH, and the current waveform and its derivative is depicted in Figure 2.43.
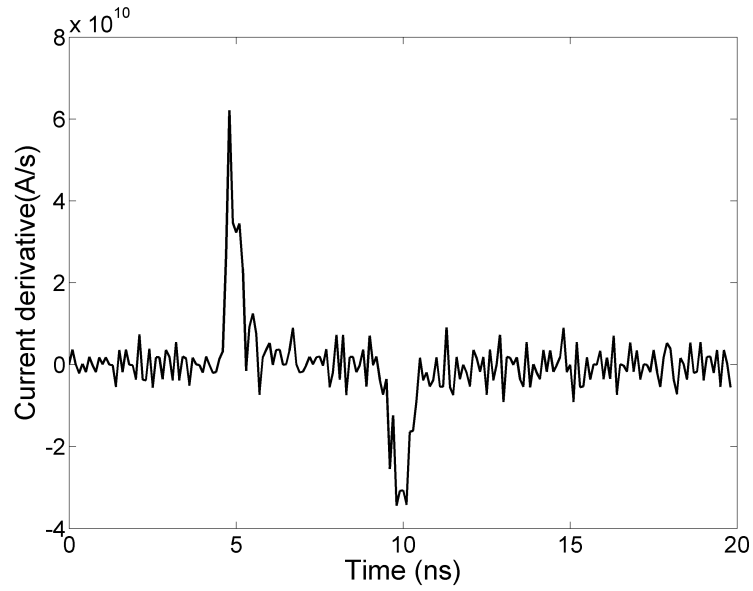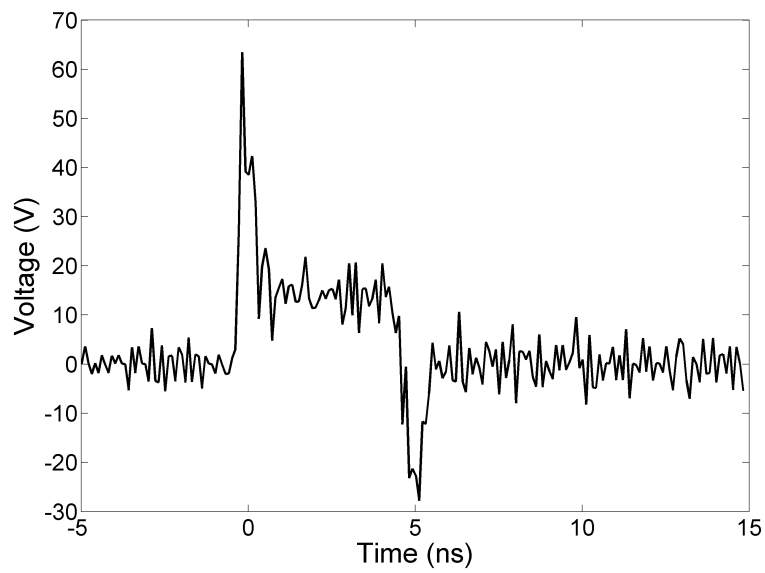
Figure 2.42: Current derivative waveform

Figure 2.43: Voltage waveform across a DUT of 0.05 Ω and 0.1 nH

Although the voltage waveform shows no direct relation to the current waveform on sight, the current waveform can be calculated out of the voltage waveform if a good estimation of the inductance and the resistance is available, and the linear combination is taken into account. The equation below shows the relation between the two waveforms.

$$V\left(t\right) = L\frac{dI\left(t\right)}{dt} + RI\left(t\right) \qquad (2.11)$$

The solution to this differential equation is given by the equation below. The constant named 'c' can be found by assuming causality and nulling the current at a time before the pulse.

$$I\left(t\right) = \left[\int \frac{V\left(t\right)}{L}dt + c\right] e^{-\frac{Rt}{L}} \qquad (2.12)$$

Although mathematically correct, this equation can become very hard to calculate as the exponential factors can become instantly very large, resulting in numerical overflow. A solution to this problem is to take a detour via the Laplace domain. The impulse response of the inverse impedance is:

$$h\left(t\right) = \frac{1}{L}e^{-\frac{Rt}{L}} \qquad (2.13)$$

The current waveform can then be found by convolving the measured voltage waveform and this impulse response. Even with a small number of impulse response samples, this can be calculated with fairly high accuracy. The result of this convolution is given in Figure 2.44.

Extra attention needs to be paid to the digital time resolution. The timestep should be significantly smaller than the timeconstant of the impulse response. If this criterion is not met, the digitized exponential function is an estimation of a unit impulse function. This then again results in the voltage shape instead of the current waveform. Still if this constraint is taken into account, and the digital timestep is reduced, excellent current waveform reconstruction is possible. Note that no extra amount of samples has to be taken in order to reduce the digital timestep. Even if the waveform is resampled using basic digital techniques, e.g. linear resampling, the obtained result is more than satisfying. In Figure 2.45 the resulting relative output error is presented in function of L/R. This relative output error is defined as the maximum difference between the calculated waveform and the ideal waveform, divided by the peak value of the waveform.
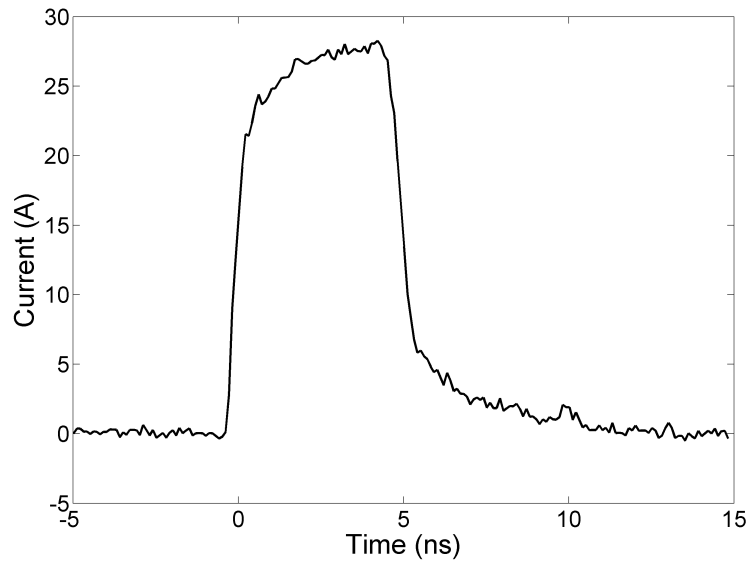
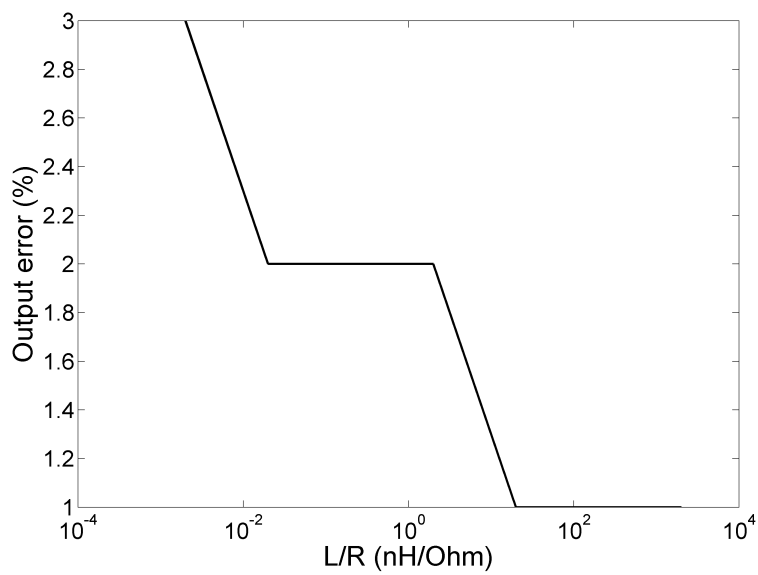Figure 2.44: Resulting current waveform after calibration

Figure 2.45: Relative output error after waveform reconstruction with known DUT

The major advantage of this technique is that only a coarse estimation of the DUT and the current waveform is initially required. This way the voltage level across the DUT, and after attenuation, the VCSEL, can be estimated. If the attenuator is adapted accordingly, this will prevent destruction of the VCSEL. The current waveform can be derived after calibration of the DUT, which results in a better estimation if the DUT impedance is constant during the ESD-pulse. This estimation will be used to perform the current waveform reconstruction during calibration. This way the DUT doesn't have to be known with high precision beforehand, as this has no effect on the layout of the device.

The major drawback of this system is that it highly depends on the fine estimation of the DUT during the calibration sequence. It is interesting to see what the results are after misestimation. Figures 2.46 and 2.47 show the result after 10% of respectively resistive and inductive estimation error.
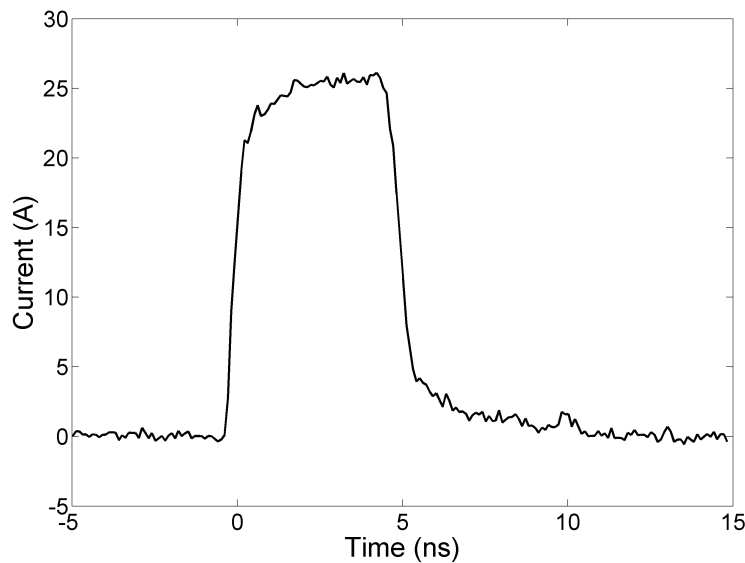
Figure 2.46: Resulting current waveform after calibration with 10% of resistive estimation error
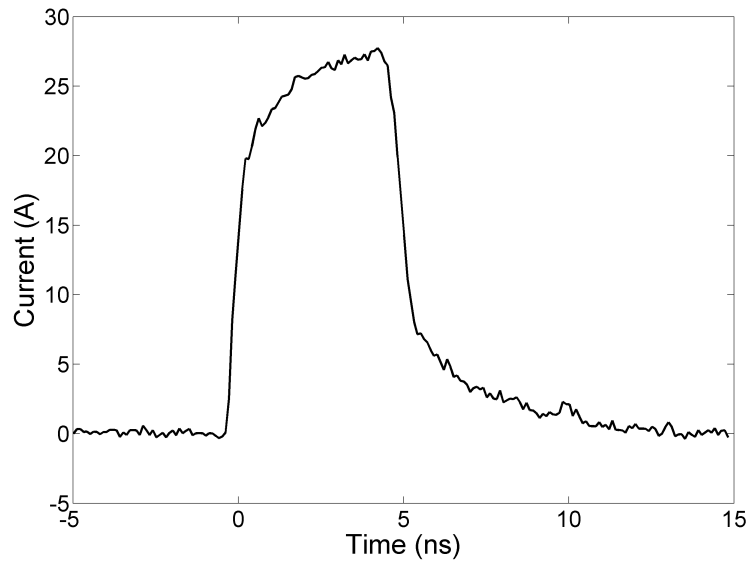
Figure 2.47: Resulting current waveform after calibration with 10% of inductive estimation error

For various devices-under-test, the resulting error has been calculated after a misestimation of R and L. As the response varies a lot for different R and L ratios, the DUTs can be mainly divided in 3 groups: highly inductive, highly resistive and balanced DUTs. During simulations, these groups were respectively represented by DUT impedances of 10 nH and 0.05 Ω, 0.1 nH and 5 Ω, and 1 nH and 0.5 Ω. The simulation results are presented in Figures 2.48 and 2.49.

Figure 2.48: Relative output error after misestimation of resistive error in multiple DUTs

Figure 2.49: Relative output error after misestimation of inductive error in multiple DUTs

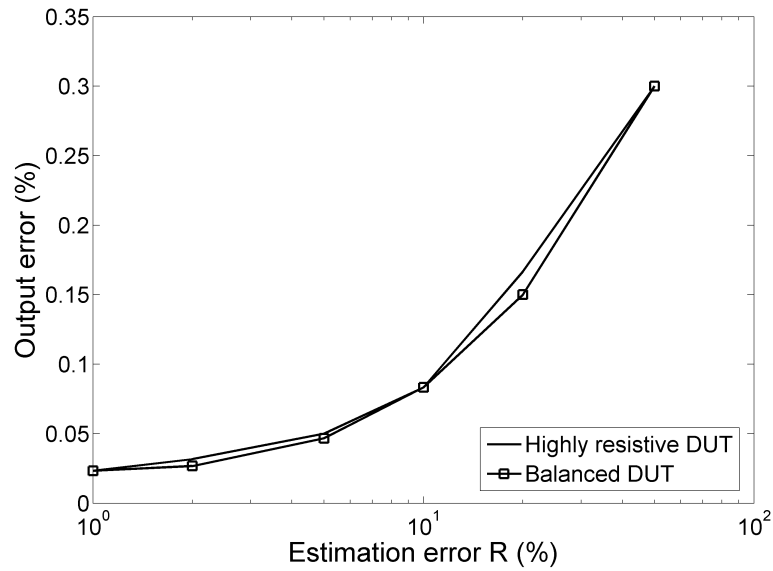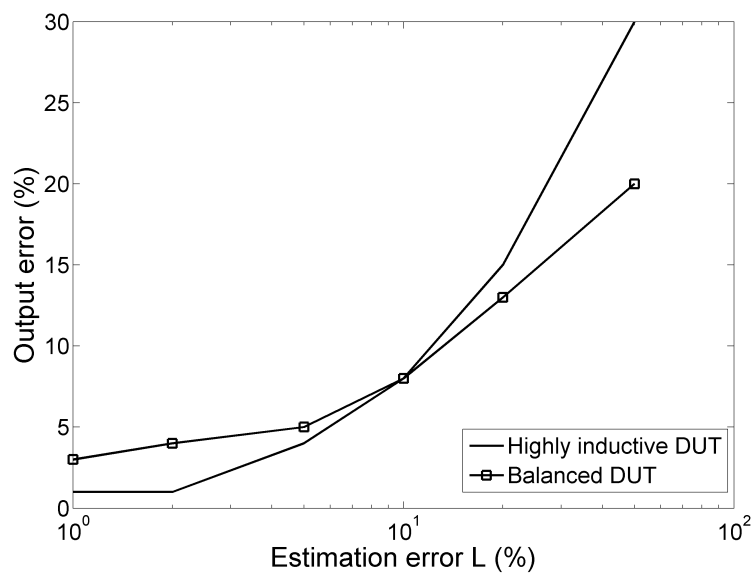Next to misestimation of the device-under-test, the dynamic range can also become a problem, as the spectrum of the voltage signal can differ significantly from the spectrum of a current signal. In Figure 2.50 the relative output error is presented versus the signal-to-noise ratio.
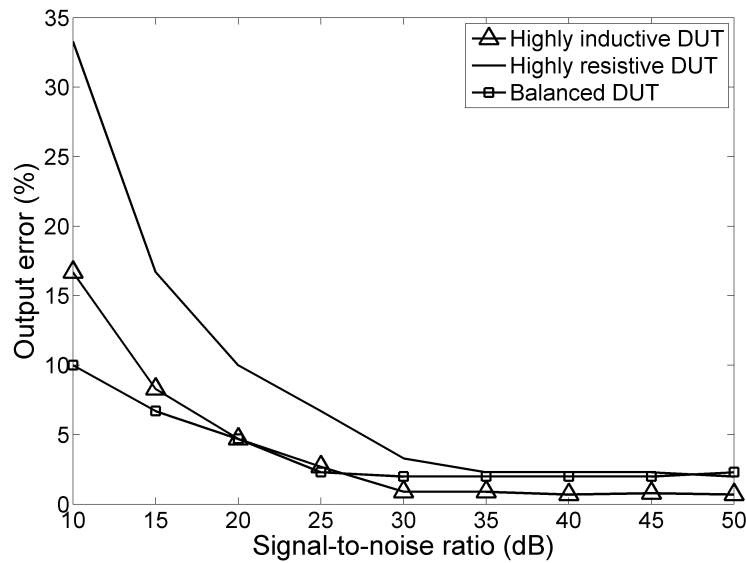
Figure 2.50: Relative output error vs. signal-to-noise-ratio in multiple DUTs

In Figures 2.51, 2.52 and 2.53 the calculated output current waveforms with a SNR of 20 dB are presented. In each of these figures the reference current waveform is represented by a grey line, while the calculated current waveform is represented by a black line.

As can be expected, noise on a highly resistive DUT is directly visible as noise on the current signal, while in the inductive case, the noise is mostly integrated, providing a good result near the starting point, which gets worse as the pulse continues. Still due to this integration process, this results in less noise than in the resistive case, as each noise sample contributes as a fixed measurement error, which is compensated over time, as white noise has a mean value of zero.

Figure 2.51: Current waveforms calculated from a voltage signal with 20 dB (Black) and infinite (Grey) SNR across a highly inductive DUT

Figure 2.52: Current waveforms calculated from a voltage signal with 20 dB (Black) and infinite (Grey) SNR across a highly resistive DUT
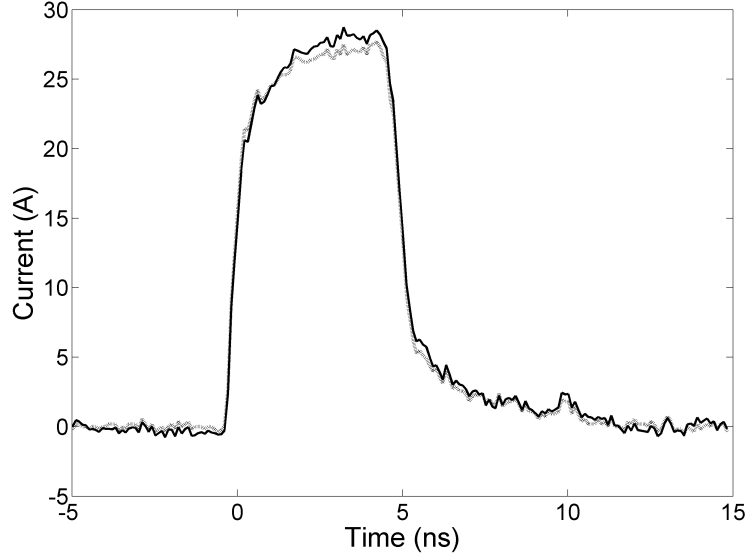
Figure 2.53: Current waveforms calculated from a voltage signal with 20 dB (Black) and infinite (Grey) SNR across a balanced DUT
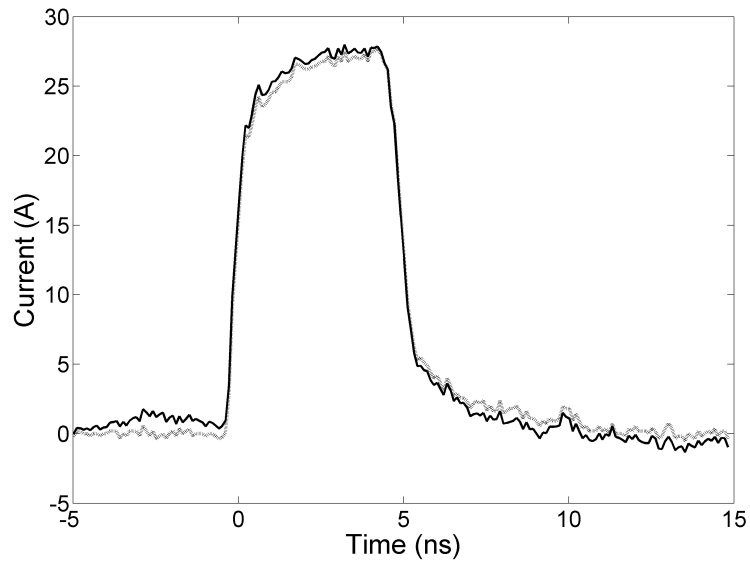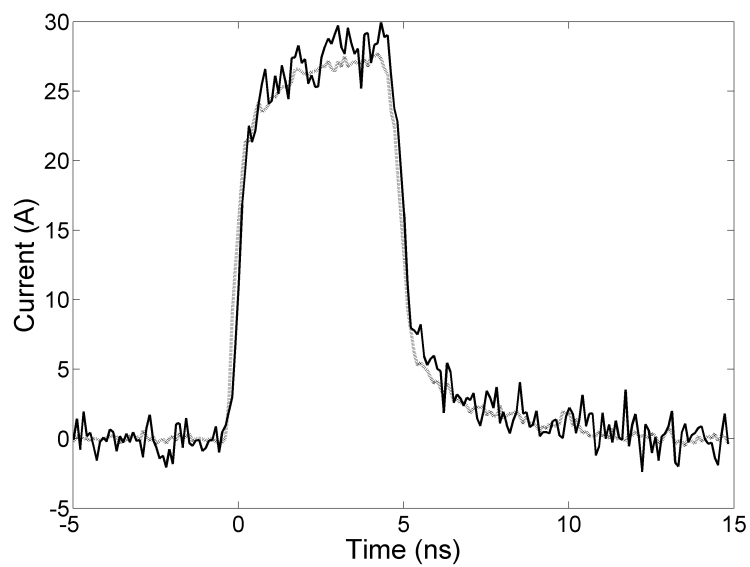
Another advantage of this calibration technique is that there is no direct effect of bondwires and other parasitics on the output signal, as long as this effect can be estimated and calibrated. Magnetic coupling only results in an extra voltage term at the VCSEL input. As long as this magnetic coupling is incorporated in the DUT-estimation, this will have no negative effect on the reconstruction. Still the added voltage component has to be small enough to prevent destruction of the VCSEL. This is presented in equation 2.14, where A is the attenuation of the measurement module, L and R are the inductivity and the resistance of the DUT and M is the mutual coupling between the input current and the VCSEL.

$$V_{VCSEL}(t) = A\left[L\frac{dI(t)}{dt} + RI(t)\right] + M\frac{dI(t)}{dt} \qquad (2.14)$$

2.6.4.5   Proposed current probe and calibration parameter extraction

The proposed current probe is the differential voltage probe, where the current waveform is calculated out of the voltage waveform after calibration. To do this, the DUT has to be well known. As stated earlier, the DUT can be modeled as a series resistance R and inductance L. The resistance consists of the resistance between the two DUT measurement interfaces,

while the inductance consists of the self inductance of the DUT and the mutual inductance between the ESD path and the measurement circuit.

Any resistor value can be calculated by using Ohm's law, as the current through this resistor is directly proportional to the voltage across it. This relationship is frequency independent. As resistors and resistance measurement equipment are commonly used in any electronics lab, this seems easy to implement.

An estimation of the resistance R can be obtained from the design information of the DUT. Often, this DUT is an on-chip test structure. The estimation errors on the DUT-resistance can be high, as in an IC production process the absolute errors can be considerable (e.g. up to 25%).

Another measurement solution can be to apply a DC-current to the DUT, and to measure the DC-voltage across the DUT. The main problem here is that the DUT is part of an ESD protection. This conductor has a very low impedance and is only accessible through the ESD protection. In order to have sufficient current through the DUT, the DC-voltage has to take such a high value that it triggers the protection. After it triggers, there is a low impedance to ground. To measure the DC-voltage across the DUT, the DC-current needs to be very large (several Amperes). Not only a voltage source with high output current is required, the amount of power dissipated in the ESD-protection will destroy it.

The solution to this problem can again be found in pulses. If charge pulses can be made with well known specifications, large enough to trigger the ESD-protection but short enough not to destroy the ESD-protection, the DUT can be characterized. Such a pulse is a transmission line pulse. A TLP-generator generates a charge pulse with a well known rectangular current shape and rise and fall time [31]. This current pulse instantly triggers the ESD-protection and goes through the DUT. The DUT-resistance provides a rectangular voltage component, while its inductance provides peaks during rise and fall of the pulse. The resistance R can then easily be defined by using Ohm's law in the rectangular voltage region. If the current waveform is taken into account, the inductance L can be obtained by differentiating this well known current waveform, and comparing the measured voltage peaks to this derivative. This way the calibration parameters can be estimated accurately, ensuring a good current probe calibration.

2.7   Conclusion

In this chapter a solution was presented to the ESD-waveform characterisation problem. To this end, measurement system specifications was defined, whereafter multiple measurement architectures were presented and their capabilities evaluated against those requirements. This resulted in the selection of a final architecture, which is based on the 'divide and conquer' principle and which is further defined throughout this work. A voltage waveform characterisation test setup was presented of which the measurement results led to a positive evaluation. Finally, a procedure that obtains the required current wave information using measured voltage pulse data, was described.

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3

Measurements on ESD-protections

In chapter 2 an ESD waveform measurement solution was presented and its voltage pulse measurement capabilities were tested. It was concluded that waveform characterisation is indeed possible. However, compensation of the frequency response by a calibration sequence is required to accurately reconstruct the waveform, and a new photodetector module is needed to obtain a higher SNR. In this chapter the voltage reconstruction capabilities of this measurement solution on real ESD-protections are tested and the measurement results evaluated. To this end, ICs with different ESD protection test structures were provided by ON Semiconductor Belgium. In section 3.1 more information on the ICs and the connection possibilities is given, section 3.2 deals with the measurement PCB design and in section 3.3 the measurement results are presented and evaluated.

3.1 ESD-protection test structures

ICs with different ESD-protection test structures were provided by ON Semiconductor Belgium. A schematic of such a typical ESD-protection test structure is provided in Figure 3.1. As a test condition, an unbiased test with Out-Vss stress was selected. An ESD-signal is applied to the out-pin while the Vss-pin is connected to ground, and the other pins are not connected. No DC-voltage is applied to any pinin an unbiased ESD-test. The connections between the test structure, the ESD signal generator and the waveform measurement solution are provided on the test PCB.
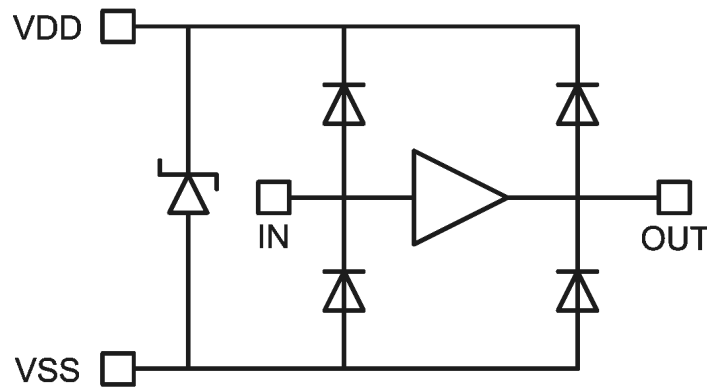
Figure 3.1: Schematic of an ESD-protection

An IC consists of a silicon body in which the components are integrated, and a few metal layers on top that connect these transistors. This way, only connections to the top metal layer can be made via special metal pads, called bondpads. These bondpads can be connected via bondwires, probed with wafer probes or directly connected to the PCB via flip-chip techniques. On this prototype PCB, the connections will be made with bondwires. Although bondwires introduce parasitics, these connections can easily be realized. In a next miniaturization step, this measurement solution can be incorporated in a wafer probe.

Figure 3.2: ESD path and bondwire probing possibilities

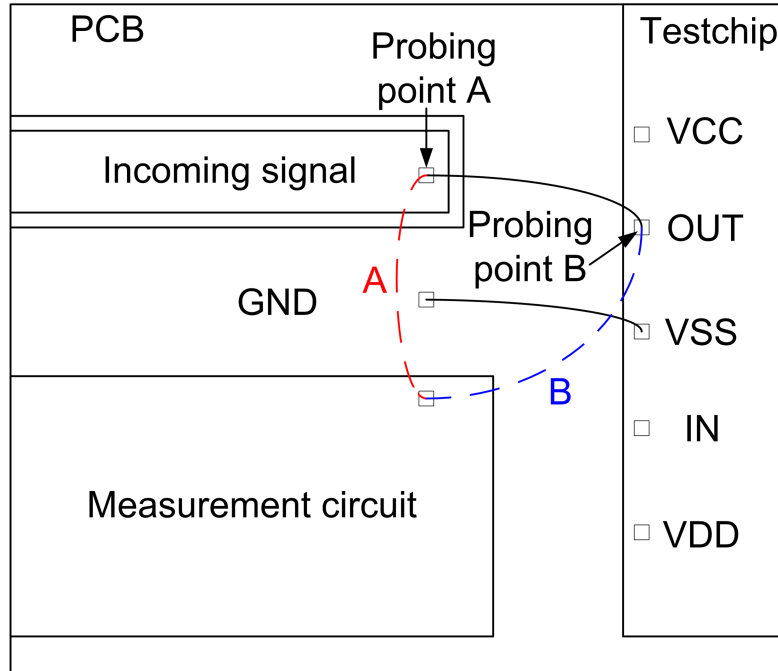As all connections to the test chip are implemented with bondwires, the ESD-current needs to go through at least two bondwires. In this case there is one forward current bondwire, and one bondwire to ground for the return current. The ESD path and all possible bondwire probing points are depicted in Figure 3.2. The reference voltage for this measurement is the external ground. A simple probing point is point A. If the parasitics of the bondwire to the Out-pin are neglected, the voltage at both bondwire ends is the same. This assumption is not correct. The ESD-current is going through this bondwire, resulting in a voltage drop across this bondwire. Especially the inductive component of this bondwire plays an important part. A bondwire with an inductance of 0.5 nH can cause a peak voltage drop of 30 V (section 2.6). The measurement bondwire needs to be connected to an on-chip bondpad. As there are no other bondpads connected to the Out-pin of the IC-under-test, a double-bonding technique is used to connect both the ESD-bondwire and the measurement bondwire to the same bondpad (probing point B). As the input impedance of the measurement solution is much higher than the impedance of the ESD-path, the voltage drop across the measurement bondwire can be neglected. This way the on-chip voltage waveform can be captured by the measurement solution.

3.2   Measurement PCB Design

In this section the design of the PCB, to measure the ESD waveforms on the testchip, is discussed. The first part deals with design constraints. In the second and third part, the schematic and layout are presented.

3.2.1   Design constraints

Before the design of the schematic and PCB layout can take place, the target functionality, main components and external constraints have to be well defined. In this case the target functionality of this PCB is still to measure on-chip ESD-protections. Consequently the design defining component is the IC-under-test. This IC-under-test contains six ESD-protection test structures of which each one is to be double bonded to the PCB.

Each of these test structures requires access to an ESD-signal, a ground connector and a measurement module. Although the reuse of a measurement module seems interesting, it would require a separate PCB that can be attached to the PCB-under-test to minimize the parasitics. This will be further described in chapter 5. To obtain a simple layout, this prototype PCB contains six measurement modules circuits. To minimize the cost, only the VCSELs will be reused.

Next to the main components, the interfaces to the pulse generator and the VCSELs should be defined. In chapter 2, the bandwidth of ESD-pulses was defined as 5 GHz. This means that the connectors need to cover such a bandwidth with low losses. In the case of the ESD input connector, the choice seems straightforward as the TLP-generator that will be used in the tests has an SMA-output. These popular connectors often have a bandwidth of 18 GHz, depending on the materials used by the manufacturer [1]. However, due to the use of a wirebonder that is normally used for ICs, this device can only process small PCBs. Therefore extra attention needs to be paid to the total PCB size. To minimize the on-PCB connector area, small Rosenberger mini-SMP connectors are used instead of SMA-connectors [1]. Although they have the same length as SMA-connectors, the width is much smaller, creating board space next to the connectors. These components have a bandwidth of 65 GHz. The connector is then connected to a controlled impedance trace, leading to the bondpad on PCB. The VCSEL output has other constraints. As described earlier, the same VCSEL is used for different test structure measurements. To do this, the pigtailed VCSEL is attached to a connector, which can be connected to a matching on-board connector. In this case a 3-pin header has been used. As this is not commonly used in the higher frequency range, the S21-characteristic of the

connection was verified, as shown in Figure 3.3. It is clear that, although there is some slight attenuation visible, these pin headers can still be used as VCSEL connectors.
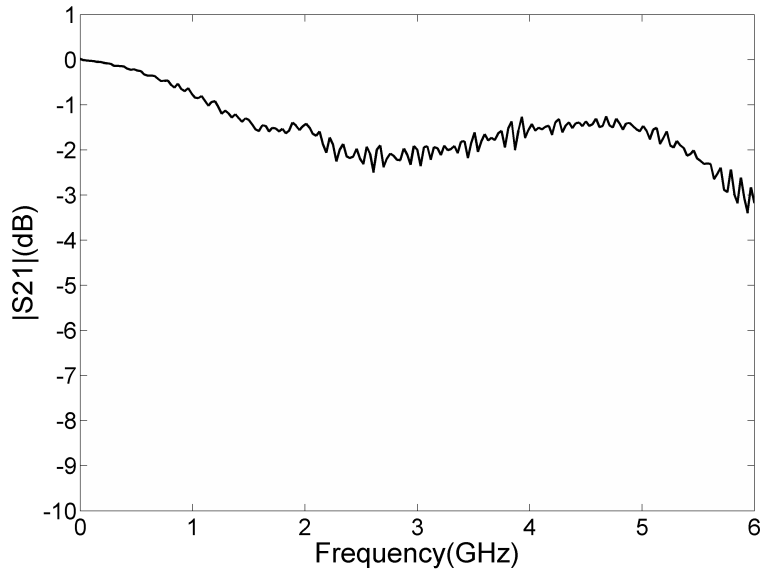

Figure 3.3: Transmission amplitude characteristic of a 3-pin header connection

As described earlier, the wirebonding process causes some PCB size constraints. Also during this process, the wirebonder keeps the target device in place by means of a vacuum chuck. This means that the device can't be correctly wirebonded if there are holes in the PCB. In a normal PCB, there are lots of holes to be drilled, e.g. through-hole component holes, mounting holes and vias. This means that the vias need to be filled by the PCB manufacturer and component holes need to be filled temporarily during the wirebond process. This can be easily done by solder, as this can again be removed afterwards. The mounting holes, which are much harder to fill, are to be placed at the outside of the PCB. This way the vacuum chuck can be used in the center of the board.

There are also other constraints caused by the use of this test chip and its bondwire connections. Bondwires need bondpads on which wirebonding can be performed. These bondpads can be made on PCB by using a certain surface finish. As there are 2 commonly used types of bondwires, Al or Au,

these can require different surface finishes. Our PCB-manufacturer offers
the possibility of using Pb-free Universal Pad Finish (Electroless Nickel /
Electroless Palladium / Immersion Gold - ENEPIG or also NiPdAu) [2].
This surface finish is suitable for soldering and bonding with both Al and
Au wires. In this work PCB-bondpads of 0.25 mm x 0.15 mm have been
made using this technique. Now that the bondpads can be made, the ques-
tion remains where to put them, as bondwire connections need to have a
certain length. With the help of ON Semiconductor Belgium, the layout
dimensions of the chip and bondpads have been defined. These dimensions
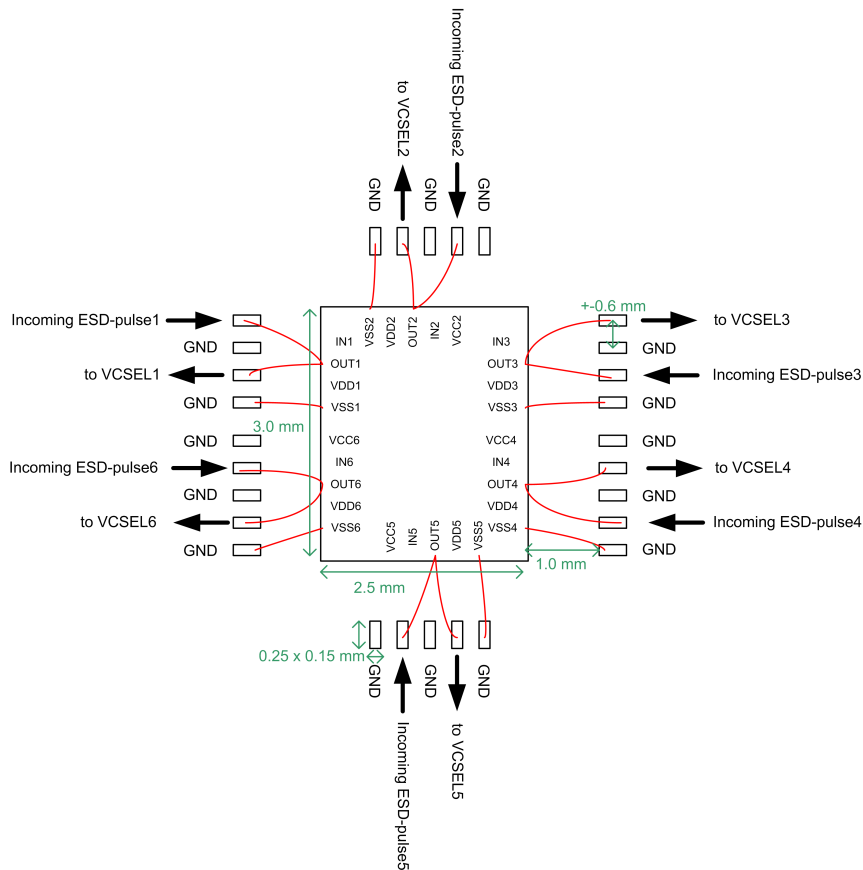and the double bonding connections are depicted in Figure 3.4.

Figure 3.4: Test chip dimensions and input/output connections

3.2.2 Schematic

On each board the following components need to be added:

- 1 test chip with bondpads

- 6 input mini-SMP connectors

- 6 measurement module attenuators and bias circuits

- 6 pin headers for VCSEL connections

- 6 reverse voltage VCSEL protection diodes

- 1 power supply connector

These are all connected in the schematic presented in Figure 3.5.
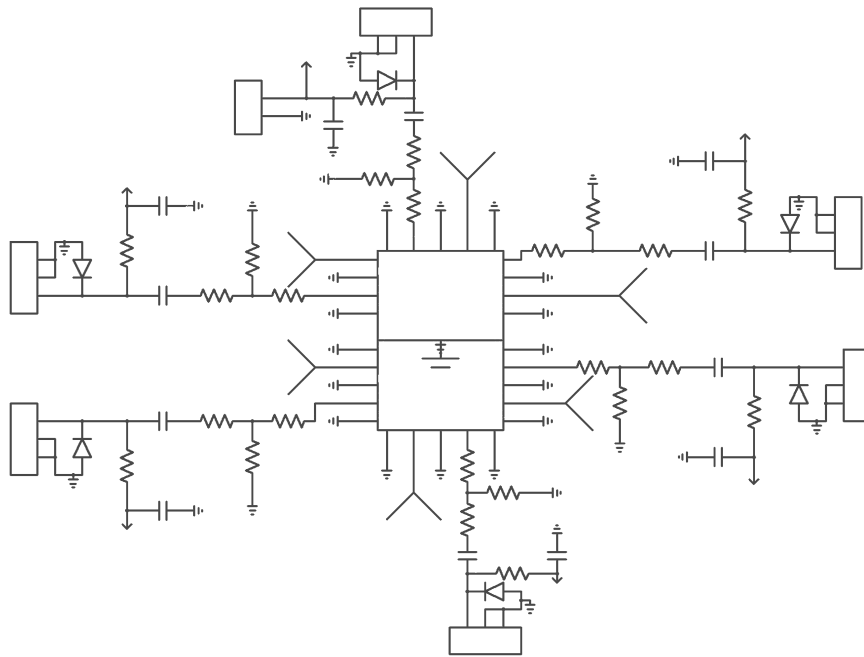
Figure 3.5: Schematic measurement PCB

The test chip symbol is placed in the center of the schematic. This symbol represents the footprint (presented in Figure 3.6) containing the bondpads on the PCB and the pad to connect the bulk of the chip.
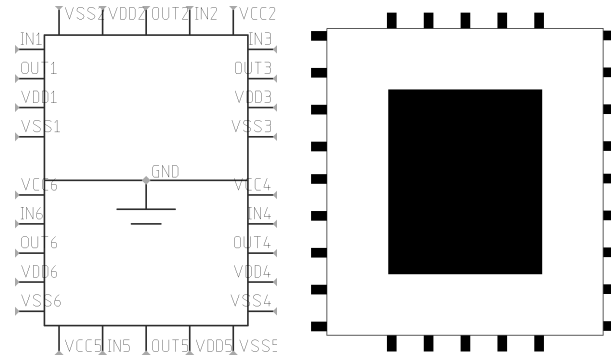
Figure 3.6: Symbol and layout footprint of the test chip

Around this test chip, the six measurement modules are placed, each connected to the bondpads according to Figure 3.4. The unused bondpads are connected to ground. Each measurement module consists of 4 resistors, 2 capacitors, a protection diode (BA595 [3]) and a pin header [4]. This circuit is depicted in Figure 3.7, where the values are chosen to withstand a 25 V input peak voltage.

Figure 3.7: Measurement module circuit

3.2.3 Board layout

The first layout step is component placement. In this step the board space is partitioned into areas reserved for the major building blocks. The conne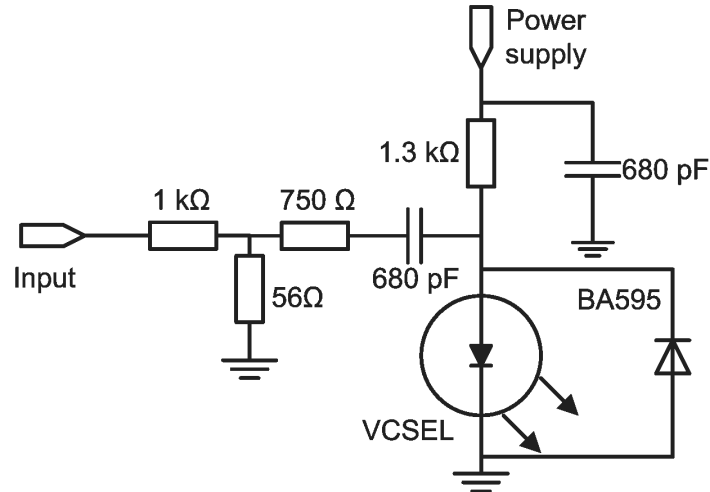ctions between these building blocks are defined. This then provides a good indication of the required number of layers, after which the layer stack can be selected. Then each component is placed in its assigned segment. Finally, the components in each segment are arranged to allow for easy routing. This placement step is followed by the routing step, where traces, vias, mounting holes and planes are defined, sometimes resulting in slight changes in the component placement. Both steps are further defined in the next paragraphs.

3.2.3.1 Component placement

One of the most important limitations to this PCB is the board size. This means the placement needs to be very well considered. The schematic consists of a test chip surrounded by six measurement modules. This can easily be copied in the board layout if the test chip is placed in the center of the top layer. The measurement circuits will be implemented with 0201-resistors and capacitors to minimize the used space. The power supply connector needs to be put near the edge of the board, crossing the board outline, as these connector types are generally large. Also, the well-decoupled supply connections can be longer than the signal connections as they generally don't contain high frequency components. Such a board layout diagram is presented in Figure 3.8.
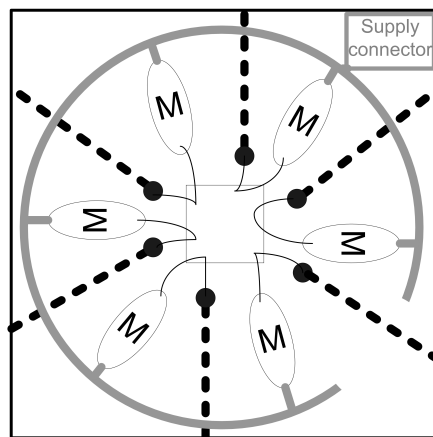
Figure 3.8: Board layout diagram with single supply connector

The routing in this layout can become complicated as each test structure needs access to the ESD-input, ground and the measurement module. Each measurement module needs to be connected to the ground and the power supply. Although it is possible to connect all supply pins on a 2-layer board proposed in Figure 3.8, this configuration is best used with a 4-layer board with a power and ground supply plane on the inner metal layers. The reason is signal integrity. Currents going through the ground plane at one layer are obstructed by the ESD input traces, going from the center of the board to the edge. To maintain a good ground connection all over the PCB, an extra ground plane is put on the other layer, which is obstructed by the large power supply connections. A large number of vias is then used to connect the two ground planes and prevent board resonances. On this 2-layer board the return path of the ESD input transmission lines will be disrupted by the supply connections, generating a larger current loop or a higher inductance if the current is sent through vias.

This problem can easily be solved as only one test structure needs to be tested at the same time. If multiple supply connectors are used, of which only one is connected at the same time, the other power supplies don't need to be connected (Figure 3.9). The only remaining question is if there is enough board space to include these extra connectors. This can be solved by using normal pin headers instead [4]. As a result, extra attention needs to be paid to the positioning as these headers can be misconnected. Again a protection diode is added to prevent destruction of the laser caused by misconnection or negative voltage peaks.
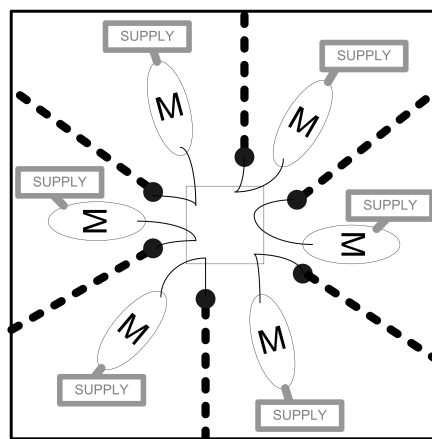

Figure 3.9: Board layout diagram with multiple supply connectors

The board efficiency can be further increased by rearranging the board layout. If the position of the input transmission line and the measurement module corresponding to one test structure are exchanged, the power supplies corresponding to this test structure and one of the adjacent test structures are located next to each other. As only one test structure is measured at the same time, these two power supplies can be replaced by a single power supply. This way, six power supplies can be reduced to three, saving extra board space.

At this point, a choice needs to be made between the first configuration on a 4-layer board or the second configuration on a 2-layer board. A 4-layer board has as advantage that routing becomes much easier compared to a 2-layer board as the inner metal layers can be used as supply and ground plane. These also provide extra isolation between measurement circuits and the input ESD signal traces, as these are situated on opposite outer signal layers. The drawback is the cost. Not only the board itself becomes more expensive if it has more layers, but also to avoid resonances in the power supply plane, this layer needs to be effectively decoupled by vias and a large number of decoupling capacitors. As a large number of vias are drilled through the board, the isolation advantage also reduced. Therefore, a double layer board has been chosen. As dielectric, FR4 is used with a thickness of 0.71 mm. This is commonly used in the industry, and therefore has a low cost. Also it has as advantage that it is lossy, which further reduces the chances on resonance. The two copper layers have a thickness of 35 μm. The top layer will contain the measurement circuits and the bottom layer will contain the input ESD signal traces. On both layers, the unused parts of the board will be covered with a ground plane, which will be connected with vias to prevent resonances.

3.2.3.2 Routing

Completion of the routing results in the final board layout (Figure 3.10). The different layers of this layout are depicted in Figure 3.11.

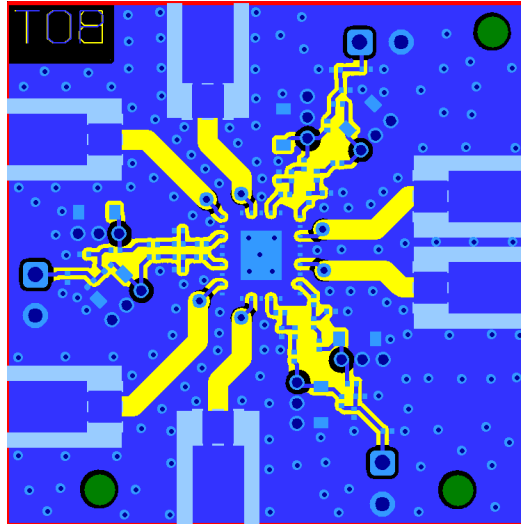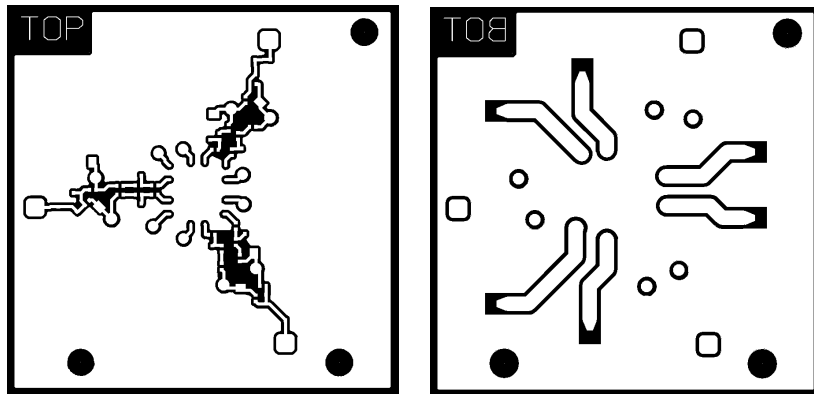Figure 3.10: Board layout measurement PCB

Figure 3.11: Layout top (left) and bottom (right) layers measurement PCB.

As stated earlier, the board layout consists of two signal layers. These signal layers have been covered with a ground plane for extra isolation, except where extra parasitics should be avoided, e.g. near the attenuator. A ground plane would provide extra parasitic capacitance to ground, provid-

ing an extra bandwidth reduction. To prevent resonances in the measurement frequency range, these ground planes have been interconnected by a large number of vias.

To obtain a good measurement result, reflections on the input interface should be omitted. Therefore the characteristic impedance of the input trace, connector and input cable should be the same. As the output impedance of a TLP-generator is 50 Ohm, and this is a common value in high frequency electronics, this characteristic impedance was selected. This is also the characteristic impedance of the Rosenberger Mini-SMP connectors. To be able to use these connectors, cut-outs need to be made in the board. These are not shown in Figure 3.10 or Figure 3.11.

Next to the vias and component holes, there are also three mounting holes visible on the PCB layout. This can be used to attach the PCB to a test setup and to protect the bondwires while handling the PCB.
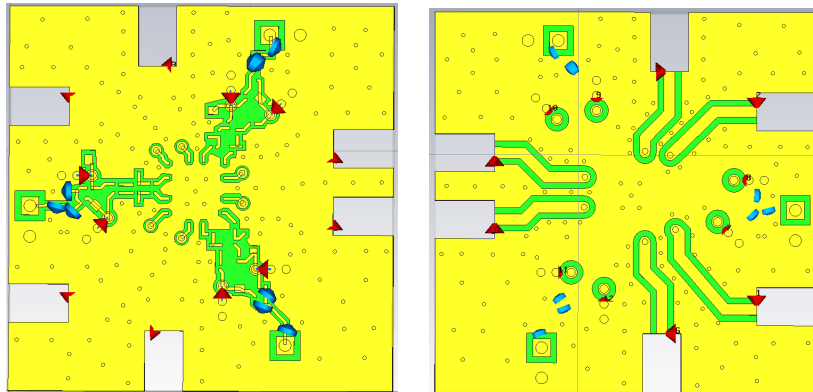
3.2.4   Layout simulations

Figure 3.12: Top (left) and bottom view (right) of the board layout in CST microwave studio (bottomview)

If the PCB layout has been made, the next step is to send it to a manufacturer. However, experience tells that in high frequency designs it is best to always be wary of resonances. This is especially the case when designing high bandwidth attenuators, as resonances in the structures surrounding the attenuator (e.g. package, PCB,...) can provide notches in the input-output isolation. Information on the possible existence of resonances inside the PCB-structure before the PCB is manufactured can be obtained by inserting the PCB-structure in a 3D-EM field simulator. In this work CST microwave studio has been used [5]. The imported board layout is shown in

Figure 3.12. The thin arrows represent test ports (input ports and VCSELs) while the thick arrows represent decoupling capacitors.

The simulated isolation between the ESD input port and the laser diode corresponding to the same test structure is depicted in Figure 3.13. The input-output isolation decreases with frequency, but there is no resonance peak visible in the curve. As the isolation is better than the target attenuation, this poses no measurement degradation.
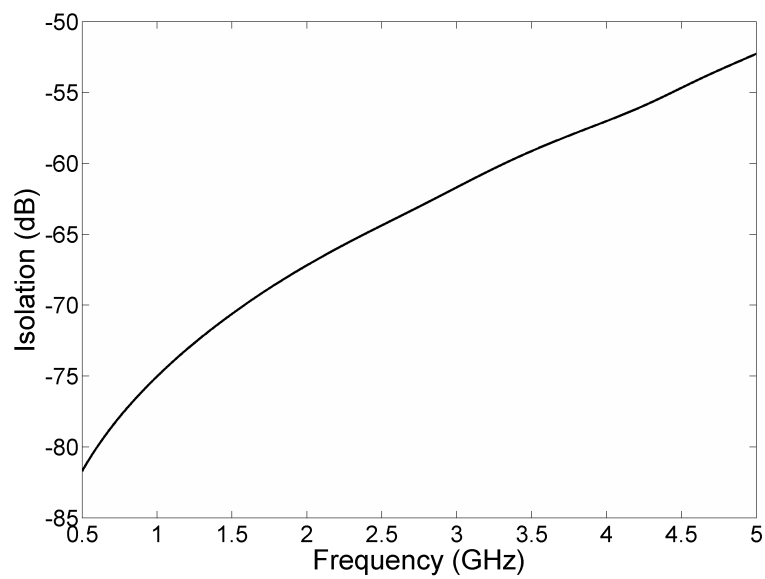

Figure 3.13: Simulated isolation between the input port and the laser diode

The finalized board with soldered components is depicted in Figure 3.14.
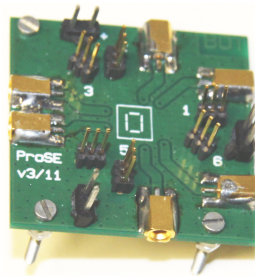
Figure 3.14: Finalized board with soldered components

3.3 PCB measurements

To perform the first voltage pulse measurements on a real ESD-protection device, a test setup identical to the one presented in section 2.3 was used (Figure 3.15).
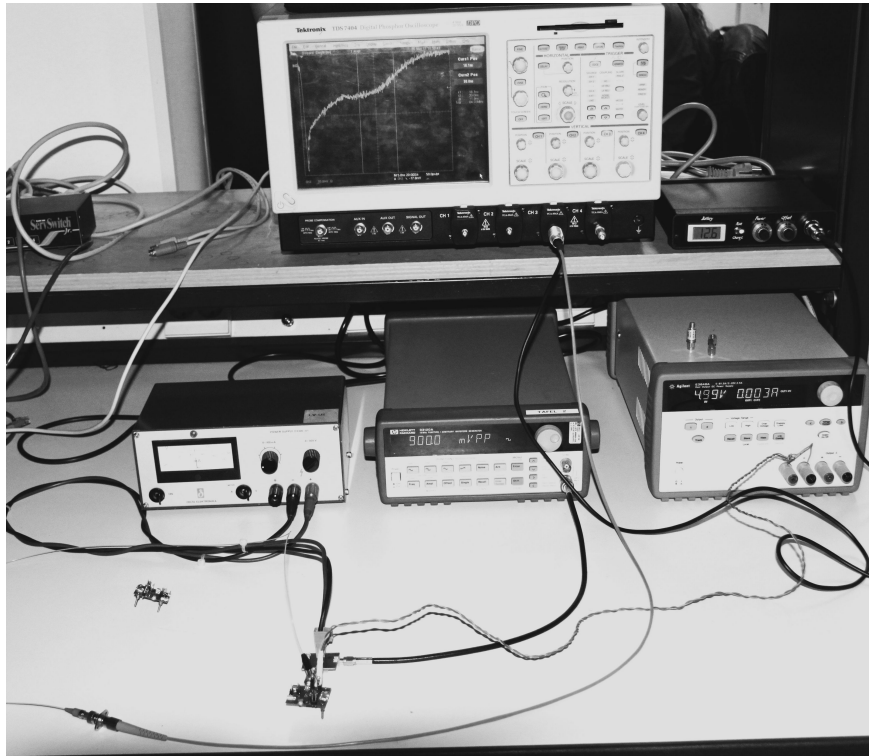
Figure 3.15: Test setup

The avalanche discharge pulse generator was directly connected to the ESD input connector of the PCB. It then generated the pulse depicted in Figure 3.16. This pulse was measured with a high impedance probe. A pigtailed VCSEL is connected to a pin header and the multimode fiber is connected to the photodetector, which is connected to the high speed sampling oscilloscope. The Alphalas photodiode has been replaced by the Newport 1580-B photoreceiver presented in section 2.5 to obtain a higher SNR. The single shot measurement result is presented in Figure 3.17.

Figure 3.16: Avalanche discharge pulse generator output pulse

Figure 3.17: Voltage pulse measured by oscilloscope

There is a clear difference between the generated pulse and the measured pulse, indicating the presence of the ESD test structure. The measured waveform consists of three regions: a voltage peak, a flat region and the pulse tail. The voltage peak at the start of the pulse can be explained by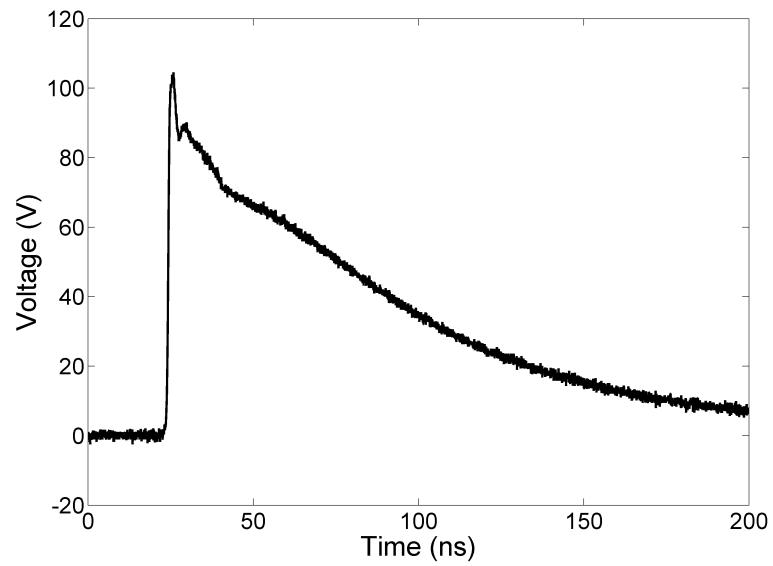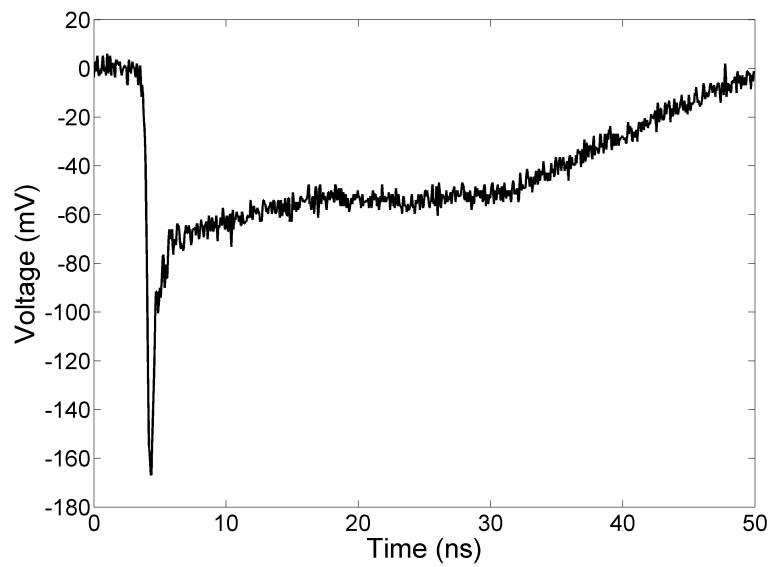 the fast pulse rise time, the delay of the test structure and the inductivity of the bondwire connections. The flat region shows the clamping of the ESD test structure and the pulse tail is caused by the diminished amount of charge, unable to drive the test structure to its threshold level [6].

Although the measured waveform of the pulse can be easily percieved, the measurement system suffers from an unexpected drop in signal-to-noise ratio. As the targeted optical power swing in the transmitter is 500 $\mu W_{optical}$ (chapter 2) and the photoreceiver has a typical conversion gain of -400 $V/W_{optical}$ [7], the expected output voltage swing is about 200 mV. This is about the measured voltage swing that was obtained. The lower SNR is caused by an unexpected rise in noise floor. The noise floor was originally estimated at 1.4 mVrms in a 5 GHz band where the measurement result has a noise floor of 2.7 mVrms. A noise measurement of the measurement solution in operation results in 1.6 mVrms at the smallest amplitude, and therefore the best noise, setting of the oscilloscope. At this point, the oscilloscope generates 0.7 mVrms noise. Therefore, the measurement solution generates 1.4 mVrms noise in operation, which is the calculated value. This means that in the measurement result presented in figure 3.17, the noise is mainly dominated by the oscilloscope. This can be explained as another oscilloscope amplitude setting has been used to digitize the entire signal. To increase the signal-to-noise ratio a digital 5 GHz low pass filter can be used, as no ESD information is situated above 5 GHz. The filtered waveform is presented in Figure 3.18. This noise floor is situated at 1.8 mVrms.

This signal-to-noise ratio can be further increased if a larger input signal is used. Not only the dynamic range of the input signal increases, but the measurement dynamic range of the oscilloscope is used more efficiently, which completely dominates the measurement dynamic range, and the signal to noise ratio of the entire measurement system. To do this the target laser input current swing is set at 5 mA by changing the attenuator circuit in the measurement module. The result is depicted in Figure 3.19. The voltage swing of this measurement is 380 mV, where the noise floor is still situated at 2.7 mVrms, as the same oscilloscope amplitude setting is used.
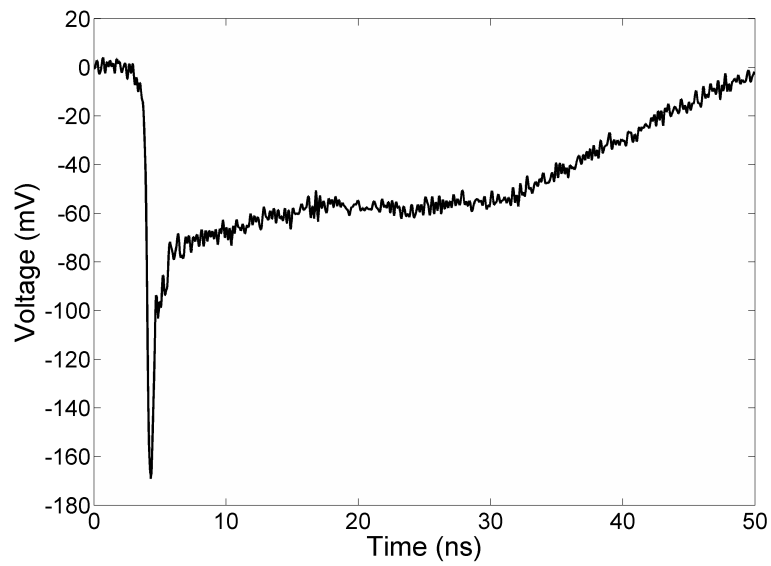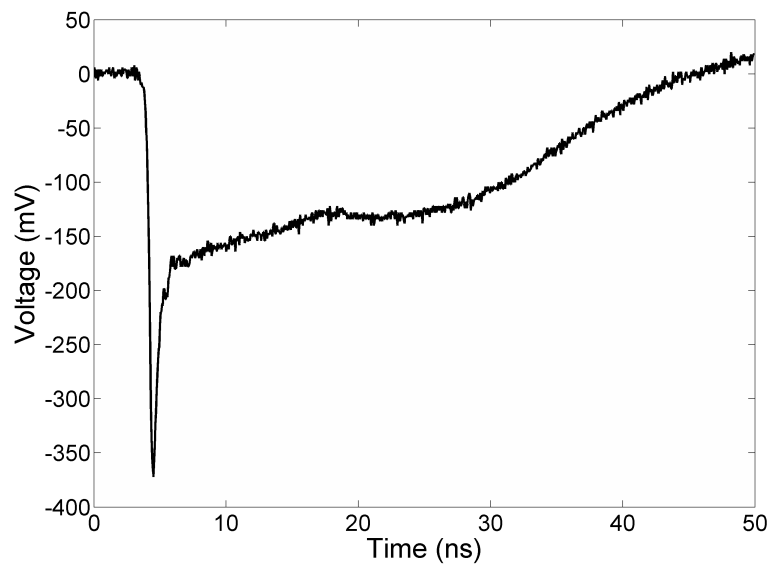
Figure 3.18: Filtered voltage pulse

Figure 3.19: Voltage pulse measured by oscilloscope

After filtering with a 5 GHz low pass filter, the signal becomes as shown in Figure 3.20 with a noise floor of 1.8 mVrms.
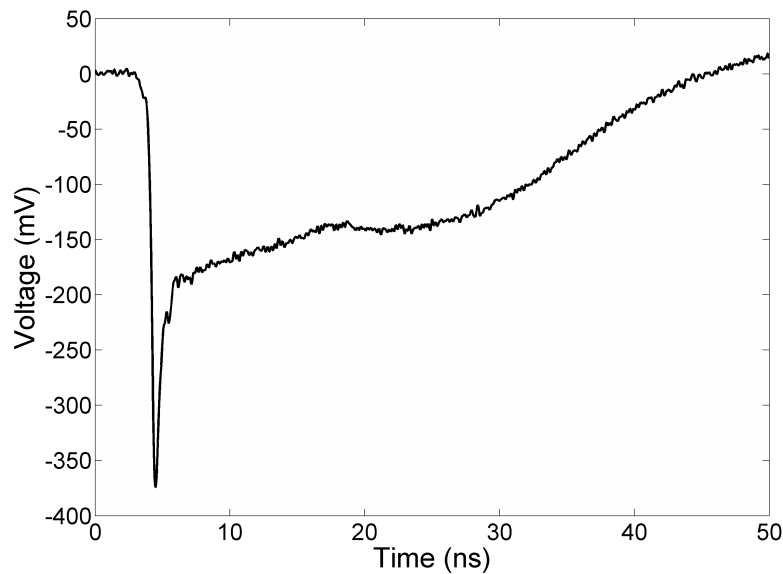
Figure 3.20: Filtered voltage pulse

This way, a dynamic range of more than 40 dB was reached. As a large signal was used to obtain these measurement results, the linearity of the measurement device was measured. This resulted in 45 dB of linearity. Non-linearity errors in this input range can be ignored. This result shows that the proposed solution meets the single shot requirements derived in section 2.1.

3.3.1 TLP-measurements on an ESD protection device

During ESD-tests of a protection device, ESD engineers use different types of pulses. Often the pulse shapes are modeled to correspond to a real life ESD occurrence. One of these commonly used pulse types is a transmission line pulse. In this paragraph one of the results of the TLP-measurements that took place at ON Semiconductor Belgium is shown. In the test setup, the earlier presented pulse generator was replaced by a TLP-generator and another oscilloscope was used. The measurement result of a TLP-test on an ESD protection device is presented in figure 3.21. Again the measurement dynamic range was limited by the used oscilloscope.
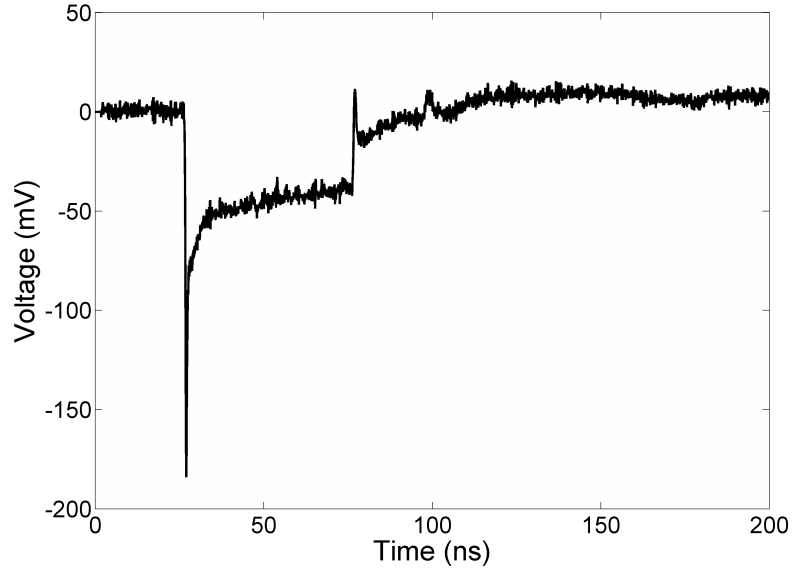
Figure 3.21: Voltage pulse measured by oscilloscope

3.4   Conclusion

In this chapter, a PCB was presented to demonstrate the voltage waveform measurement capability of the measurement solution on an ESD-protection device. As test condition, an unbiased test with Out-Vss stress was selected. The measurement results obtained with the test setup described in section 2.3 were presented and the measurement system was evaluated, showing a SNR and linearity that meet the specifications. Finally, an on-chip TLP measurement result on an ESD-protection device was presented.

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4

Calibration of a measurement probe

Before an instrument can be used in a test setup, it needs to be compared to a calibration standard, a device with a known or assigned correctness. This results in error information of the instrument. The calibration procedure then comprises both the gathering of this information and compensation of the measurement results until these agree with the value of the used standard, within a specified accuracy.

The same thing can be applied to measurement probes. A measurement probe transports information from the probe tips to the input port of a measurement device. In this application, this measurement device is an oscilloscope. Information on the characteristics of the probe can be used in a calibration procedure to obtain correct measurement data, as the measurement device itself is calibrated.

Which probe characteristics are to be used for calibration depends on the type and complexity of the probe. The measurement solution presented in chapter 2 is a linear, time invariant system. It can therefore be completely defined by means of its impulse or frequency response [1]. This frequency response can then be compensated by filtering the measurement data in a filter based on this frequency response. These steps are described further in this chapter.

4.1   Frequency response of the measurement solution

A measurement device that is often used to obtain the frequency response of a system is a Vector Network Analyzer (VNA). This device measures both reflection and transmission characteristics of a DUT at known frequencies in a 50 Ω system. The transmission characteristics can only be used directly if the input impedance of the DUT is 50 Ω. The reason is that a VNA measures the transmission characteristics in a 50 Ω system, so that other impedance levels cause reflections of the input signal. As the measurement solution probe measures voltage, with minimum influence on the ESD operation, it has a high input impedance. Its frequency response can then be calculated easily from the obtained transmission characteristics if its input impedance is known at the same frequencies. This input impedance can be derived from the reflection characteristics that have been measured by the VNA. To obtain the S-parameters of a high impedance wafer probe by means of a vector network analyzer, the technique presented in [2]. As high speed sampling oscilloscopes also have a 50 Ω input impedance, there is no compensation for the output impedance required. In [3] P. Kabos includes the oscilloscope reflection coefficient in the calibration.
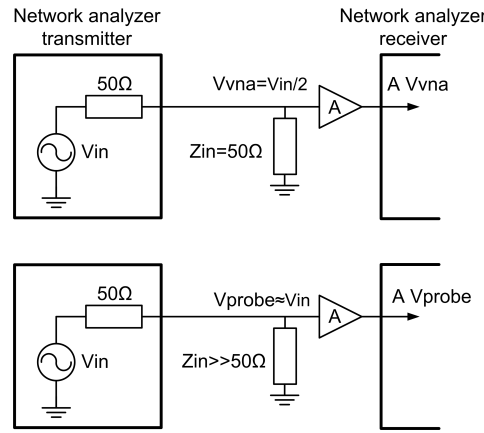
Figure 4.1: Effect of input impedance on transmission characteristics

The ratio of the measured transmission characteristic and the frequency response at a certain frequency due to a high input impedance can be easily calculated from Figure 4.1. The amplifier A is an ideal voltage amplifier. V_{in} can be written as function of V_{probe} and as function of V_{VNA}:

$$V_{in} = 2V_{VNA} = \frac{50 + Z_{in}}{Z_{in}} V_{probe} \qquad (4.1)$$

This results in:

$$V_{probe} = \frac{2Z_{in}}{50 + Z_{in}} V_{VNA} \qquad (4.2)$$

Z_{in} can also be written as function of its reflection parameter S_{11} and the characteristic port impedance 50 Ω [4]:

$$Z_{in} = 50 \frac{1 + S_{11}}{1 - S_{11}} \qquad (4.3)$$

Substituting equation 4.3 in equation 4.2, this formula further simplifies to:

$$V_{probe} = (S_{11} + 1) V_{VNA} \qquad (4.4)$$

This can be used to calculate the frequency response of the measurement solution:

$$H(f) = \frac{S_{21}(f)}{(S_{11}(f) + 1)} \qquad (4.5)$$

As this formula is valid for all possible input impedances, this parameter can be used to optimize the accuracy of the frequency response calculation. This is the same result as was obtained in [3] for the oscilloscope reflection coefficient equal to one.

4.2 Calibration filter selection

As mentioned earlier, each linear, time invariant channel can be represented by its impulse response $h(t)$ and frequency response $H(f)$. This means that a linear, time invariant filter can be used to compensate for this channel characteristic. The channel not only distorts the input signal, but also adds noise afterwards. The channel characteristic and the compensation filter are presented in Figure 4.2.
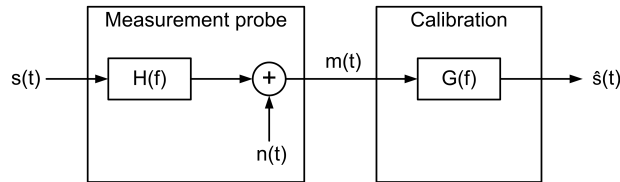

Figure 4.2: Channel characteristic and compensation filter

4.2.1   Inverse filter

The filter that can be used to obtain ideal frequency compensation is the inverse filter. Its frequency response G(f) is given by:

$$G_{inverse}\left(f\right) = \frac{1}{H\left(f\right)} \tag{4.6}$$

In the frequency domain the spectrum of the compensated signal ŝ(t) is presented by:

$$\widehat{S}_{inverse}\left(f\right) = S\left(f\right) + \frac{N\left(f\right)}{H\left(f\right)} \tag{4.7}$$

In a noiseless channel, this filter provides perfect compensation as the compensated signal is equal to the input signal. The problem arises when noise is added to the channel, or in this case the measurement probe. The second term in equation 4.7 can become very large when the channel frequency response H(f) becomes very low, thus amplifying the noise. This happens in the stop bands of both low- and high-pass filters, due to AC-coupling or the inherent high frequency limitation of the components used. Also, if the channel characteristic shows a notch filter response due to a resonance in the circuit, this will be visible in the compensated signal as ringing. To recapitulate, this filter provides ideal frequency compensation, but can reduce the signal-to-noise ratio to unusable quantities.

4.2.2   Maximum a posteriori estimator

There is more information available than has been used to design the inverse filter: the expected a priori signal-to-noise ratio. Therefore it is more appropriate to design a filter that takes this into account. This can be done by using Bayesian estimation.

In Figure 4.2 a signal $s(t)$ with frequency spectrum $S(f)$ passes through a filter with frequency response $H(f)$. Then noise with spectrum $N(f)$ is added, which then results in the measurement signal with spectrum $M(f)$. If for each frequency point f, a complex filter $G(f)$ can be found that transforms $M(f)$ in a good estimation of $S(f)$, then $m(t)$ will be transformed in a good estimation of $s(t)$. As each frequency point is treated separately, the notation will be simplified by leaving out the (f) in the next discussion. To obtain this good estimation of $S(f)$, the Maximum A Posteriori (MAP) estimator will be used [5]. This estimator returns the $S(f)$ that has the highest probability of being generated by $M(f)$.

$$\widehat{S}_{MAP}(M) = arg\max_{S} p(S|M) \qquad (4.8)$$

Applying Bayes' theorem to equation results in:

$$\widehat{S}_{MAP}(M) = arg\max_{S} p(M|S)\, p(S) \qquad (4.9)$$

To derive both distributions $p(M|S)$ and $p(S)$, $n(t)$ is assumed to be white Gaussian noise with known variance and mean value 0. Then N has a complex-valued circular symmetric Gaussian distribution with known variance and mean 0. This results in:

$$p(M|S) = C_1 exp\left(-\frac{|HS - M|^2}{2A^2}\right) \qquad (4.10)$$

where M, S and H are complex numbers. As the initial signal power can be estimated, and the phase of the input signal at each frequency point is unknown, a Gaussian distribution with mean value 0 and known variance B can be used.

$$p(S) = C_2 exp\left(-\frac{|S|^2}{2B^2}\right) \qquad (4.11)$$

This results in:

$$\widehat{S}_{MAP}(M) = arg\max_{S} C_1 C_2 exp\left(-\frac{|HS - M|^2}{2A^2} - \frac{|S|^2}{2B^2}\right) \qquad (4.12)$$

or as ln(x) is monotonic:

$$\widehat{S}_{MAP}(M) = arg\max_{S} ln(C_1 C_2) - \frac{|HS - M|^2}{2A^2} - \frac{|S|^2}{2B^2} \qquad (4.13)$$

The standard way to determine a maximum is by identifying the derivative with zero.

$$\frac{d}{dS}\left(-\frac{|HS - M|^2}{2A^2} - \frac{|S|^2}{2B^2}\right) = 0 \qquad (4.14)$$

or

$$\frac{d}{dS}\left(-\frac{\left(\overline{HS}-\overline{M}\right)\left(HS-M\right)}{2A^2}-\frac{\overline{S}S}{2B^2}\right)=0 \qquad (4.15)$$

or

$$\frac{d}{dS}\left(-\frac{|HS|^2+|M|^2-2Re\left(HS\overline{M}\right)}{2A^2}-\frac{|S|^2}{2B^2}\right)=0 \qquad (4.16)$$

where $^-$ is used as complex conjugate operator. This equation has no solution as the derivative of $Re(S)$ to the complex variable S doesn't exist. As a maximum still needs to be obtained, the gradient operator can be used instead. This operator is defined as:

$$\nabla f\left(x\right)=\frac{\delta f\left(x\right)}{\delta x_R}+I\frac{\delta f\left(x\right)}{\delta x_I} \qquad (4.17)$$

In this equation, I is the imaginary unit, x_R is the real part of variable x and x_I is the imaginary part of variable x.
Applying the gradient operator to equation 4.16 results in:

$$\frac{|H|^2 S-\overline{H}M}{A^2}+\frac{S}{B^2}=0 \qquad (4.18)$$

as the gradients of $|HS|^2$, $Re(HS\overline{M})$ and $|S|^2$ respectively become $2|H|^2S$, $\overline{H}S$ and $2S$. The MAP estimator becomes:

$$\widehat{S}_{MAP}=\frac{\overline{H}}{|H|^2+\frac{A^2}{B^2}}M=\frac{\overline{H}}{|H|^2+\frac{1}{SNR}}M \qquad (4.19)$$

in which B^2/A^2 is the ratio of the initial signal power and the measured noise power, and therefore a SNR. In case of Gaussian distributions, the MAP estimator is equal to the Minimum Mean Square Error (MMSE) estimator which makes the estimator efficient [6]. For an infinite SNR-value, this estimator, which is in this case also the efficient Maximum Likelihood (ML) estimator, results in the inverse filter. For a limited SNR-value, this value becomes a limitation on the amplification of the filter. As there have been some assumptions on signal and noise spectrum, and to include a degree of freedom, the calibration filter has been chosen as:

$$G_{MAP}\left(f\right)=\frac{\overline{H}\left(f\right)}{|H\left(f\right)|^2+K} \qquad (4.20)$$

where the factor K is user-defined to limit the amplification of noise.

4.3 Frequency compensation

In the previous paragraphs it was explained how the channel's frequency response can be calculated from the transmission and reflection parameters measured by a VNA and how this frequency response can be used to obtain the frequency response of the compensation filter. The only remaining step to obtain the compensated, or calibrated, output signal is filtering the uncompensated signal itself. This can be implemented as a convolution of the measured signal and the filter's impulse response or as a multiplication of the signal spectrum and the filter's frequency response. Both options are possible for analog and digital signals, where computation time is minimized in the digital domain by choosing the second alternative.

When calibrating the measurement solution, the VNA measures its transmission and reflection parameters at a limited number of frequencies. These measurement frequencies are equidistant within a specified frequency range, which is often the full span of the VNA. This poses a problem as the FFT-algorithm expects the frequency components to be equidistant, starting from DC, while a VNA doesn't measure the DC component. This can be solved by choosing the first measurement frequency in such a way that all frequencies are equidistant when a 0 is included as DC-component. Still it is interesting to use non-equidistant measurement frequencies in this application. It can be expected that the frequency characteristic of the channel will show large changes at the lowest and highest frequencies due to the solution's measurement bandwidth, while in between it will only be slightly changing. Therefore, a non-equidistant frequency compensation technique is presented below.

The non-equidistant frequency compensation technique transforms a measurement signal into a calibrated signal by means of a list of frequencies, and its corresponding filter frequency response value. This has to be done in three steps. First, the filter's impulse response is estimated based on the information at hand. Then, this response is sampled with the same sample frequency as the measured signal. If this sample frequency is too low to allow reconstruction of the filter impulse response, the measurement signal is interpolated until this condition is met. In the final step, the convolution of this sampled filter impulse response and the (interpolated) measurement signal is calculated, which results in the calibrated signal.

4.3.1   Filter impulse response estimation

To estimate the filter impulse response, the obtained frequency response samples are interpolated and then inverse Fourier transformed. In this project, linear interpolation has been used. Each linear interpolated signal can be written as a sum of elementary triangles (Figure 4.3), as shown in Figure 4.4.
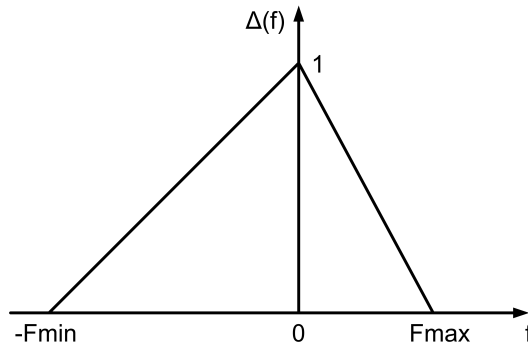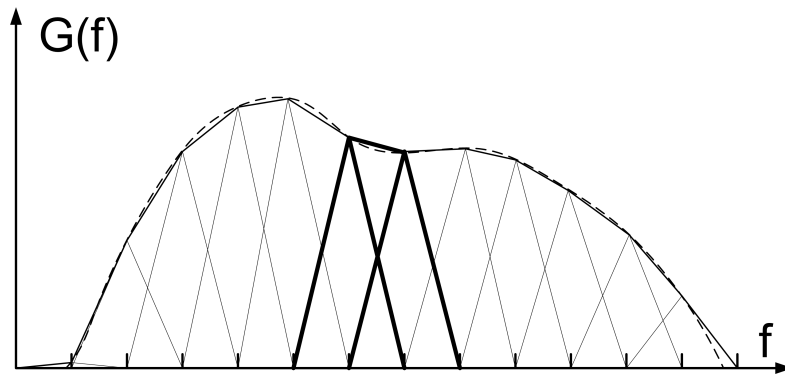

Figure 4.3: Elementary triangle

Figure 4.4: Elementary triangles used for linear interpolation

The inverse Fourier transform of such a signal can be obtained by calculating the inverse Fourier transform of such a triangle and use this basic function to reconstruct the inverse Fourier transform of the whole signal. As the calibration filter is a real filter, the complex conjugate of each filter frequency response sample needs to be used at its corresponding negative frequency. This way, this results in a real valued impulse response.

The inverse Fourier transform of a triangle as shown in Figure 4.3 is given by:

$$\Delta\left(t\right) = \frac{F_{max}\left(1 - e^{-j2\pi F_{min}t}\right) - F_{min}\left(1 - e^{j2\pi F_{max}t}\right)}{4\pi^2 t^2 F_{min}F_{max}} \qquad (4.21)$$

which has as limit for t=0:

$$\lim_{t\to 0}\Delta\left(t\right) = \frac{F_{min} + F_{max}}{2} \qquad (4.22)$$

or in the case F_{min} and F_{max} are equal to F these equations become:

$$\Delta\left(t\right) = \frac{1 - cos\left(2\pi Ft\right)}{2\pi^2 t^2 F} \qquad (4.23)$$

and:

$$\lim_{t\to 0}\Delta\left(t\right) = F \qquad (4.24)$$

The estimated filter impulse response is then given by:

$$\widehat{h}\left(t\right) = \sum_{n=1}^{N}\left(Q_n\left(t\right) + \overline{Q}_n\left(t\right)\right) \qquad (4.25)$$

with

$$Q_n\left(t\right) = H\left(f_n\right)\Delta_n\left(t\right)e^{(j2\pi f_n t)} \qquad (4.26)$$

where N is the number of frequency response measurement points $H(f)$, each at a frequency f_n. In the calculation of each elementary triangle F_{min} is given by $f_n - f_{n-1}$ and F_{max} is given by $f_{n+1} - f_n$. It is clear that the obtained impulse response is a sum of shifted triangles with center frequency f_n, which results in the exponential factor after inverse Fourier transformation. As both measurement and calibrated signal are real-valued, the impulse response needs to be real-valued. To obtain this, the complex conjugate of this sum was added to the result, as this corresponds to the spectrum in the negative frequency range.

Once the impulse response is derived, it is sampled and convoluted with the (interpolated) measured signal. This results in the required calibrated signal.

4.4 Calibration of the measurement solution

In this section, the calibration algorithm is illustrated on the measurement results obtained with the testboard described in section 3.2. First it is described to which constraints the test setup must satisfy to obtain correctly calibrated results.

4.4.1 Calibration constraints on the measurement probe and test setup

This calibration procedure consists of three steps:

- acquisition of a voltage-to-voltage transfer function of the measurement probe

- calculation of the compensation filter

- compensation by means of the impulse response of this compensation filter

To be able to compensate by means of an impulse response of a compensation filter, the compensation filter needs to be completely described by means of its impulse response. To this end, the compensation system needs to be linear and time invariant. As this compensation filter is derived from the measurement probe transfer function in a linear and time invariant way, the voltage-to-voltage transfer function of the measurement probe, this measurement probe needs to be linear and time invariant. These constraints also apply to structures required for de-embedding.

It is clear that if a linear and time invariant transfer function is obtained in a correct way, the compensation filter can be easily calculated, and the frequency characteristic of the measurement system is successfully compensated. A description of this voltage-to-voltage transfer function is obtained in this algorithm through processing of the linear scattering parameters or S-parameters that have been measured on the measurement probe. As a laser link is unidirectional and no compensation for the photodetector output impedance is required, only S11 and S21 need to be used. These S-parameters describe the reflection and transmission system response on incoming signals. In this calibration procedure, the calibration reference plane needs to be placed direcly on the high impedance interface. If a transmission line is added before this interface, it needs to be de-embedded. Also take into account that such a transmission line also changes, and in this case decreases, the input impedance of the measurement circuit. Therefore, the

input attenuator is best put as close as possible to the input of the measurement probe. To give an idea of the order of magnitude: at 5 GHz, a quarter wavelength in free space corresponds to about 1.25 cm. In other environments, this is length even further reduced with the square of the effective relative permittivity of the environment.

4.4.2   Illustration of the calibration procedure

In this paragraph the calibration algorithm is illustrated on the measurement results obtained with the test board described in section 3.2. As the measurement solution module is included in this layout, it is impossible to characterize the stand-alone module in this test setup. Therefore it is also impossible to obtain the calibrated voltage signal on the ESD-protection. This is why the results shown in this paragraph are merely an illustration of the correct operation of the calibration algorithm. No other conclusions should be drawn from these results. If valuable information on the ESD structures is required, an identical measurement module without ESD-protection is to be measured separately, providing the required calibration information. This will result in a decreased measurement error. Using a miniature measurement probe as presented in chapter 5 will be easier to calibrate and further reduce calibration errors, as the same probe that is used for measurement can be directly calibrated.

To illustrate the operation of the calibration algorithm, the signal response on a TLP-pulse measured by the measurement solution (section 3.3.1) is used as uncalibrated signal. This is shown in Figure 4.5. Then the measurement solution, i.e. the combination of the optical link and the PCB presented in chapter 3, was measured with the vector network analyzer. The amplitude of the transmission characteristic is presented in Figure 4.6.

The first step in the calibration procedure is to calculate the channel frequency response from the measured S-parameters using equation 4.5. These calculations result in the response shown in Figure 4.7. There is a clear difference between the S21-characteristic shown in Figure 4.6 and the frequency response shown in Figure 4.7, due to the input impedance of the test setup.
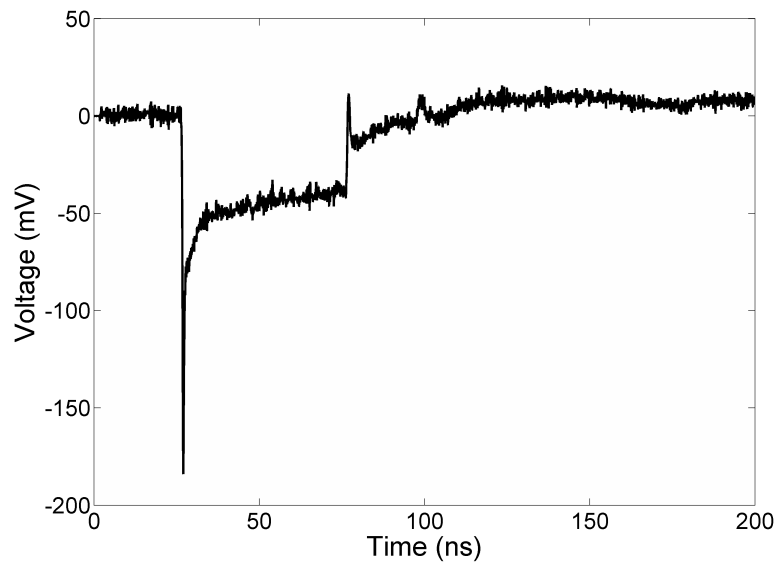
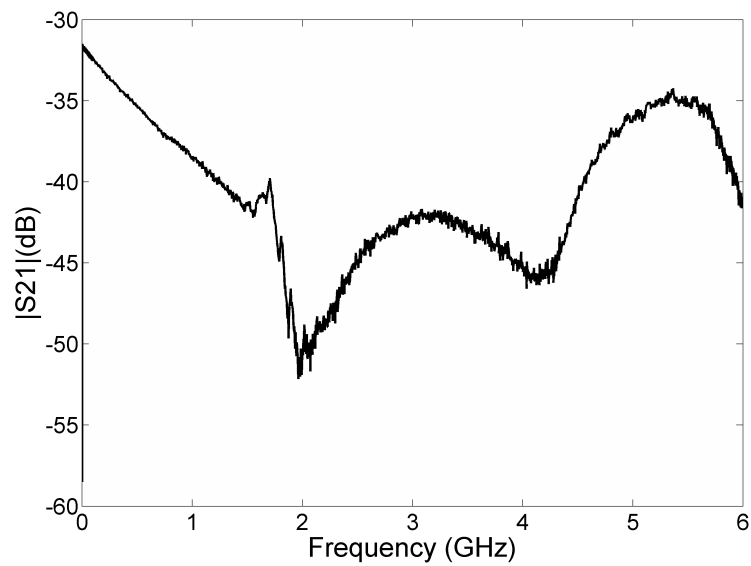Figure 4.5: Uncalibrated voltage pulse

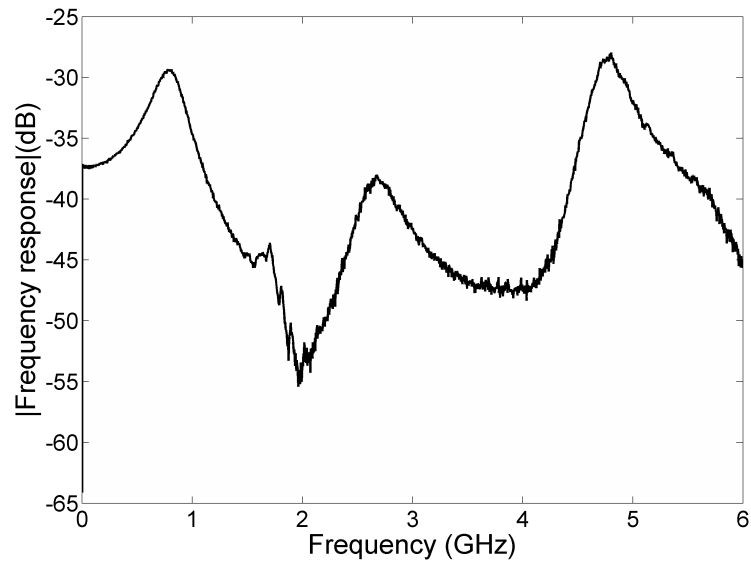Figure 4.6: Absolute S21-characteristic of the measurement device

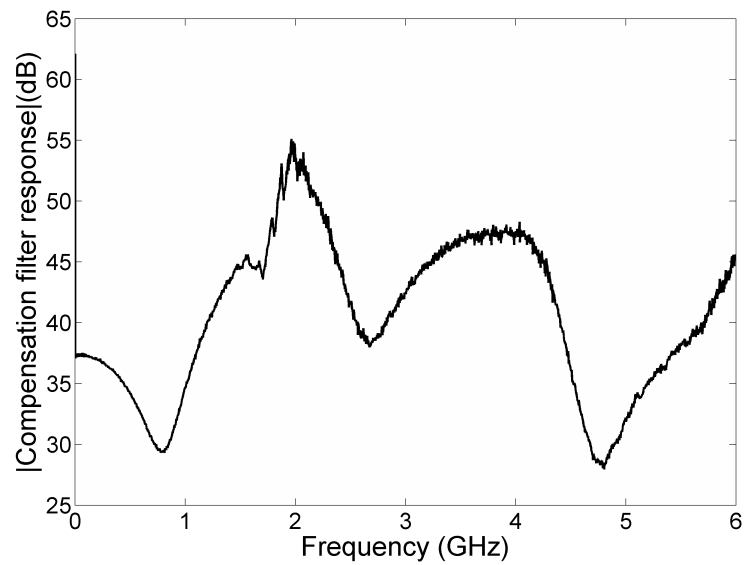Figure 4.7: Absolute frequency response of the measurement device

Figure 4.8: Absolute compensation filter response with K=$10^{-6.5}$

The next calibration step is the selection of an adequate K-value. In this

case, there are no sharp frequency peaks that need to be suppressed. A good K-value seems to be $10^{-6.5}$. This puts an amplification limit of 65 dB on the compensation filter, which is more than the amplification needed to compensate for the complete frequency response. This way, the compensation filter is not altered by this limit, which is clearly visible as the amplitude characteristic of the compensation filter (Figure 4.8) is the inverse of the amplitude response of the measurement device (Figure 4.7).

As the maximum filter frequency is 6 GHz due to the VNA, and the signal sampling rate is 25 GSps, the number of samples doesn't need to be interpolated. The length of the impulse response has been chosen in such a way that the variations at the edges were reduced by a factor 1000 compared to the maximum value. The obtained 'calibrated' signal is presented in Figure 4.9.
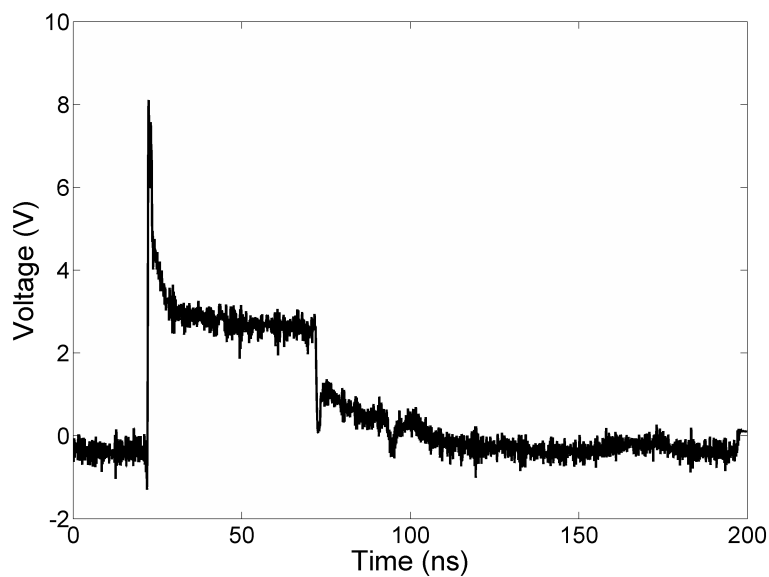

Figure 4.9: Calibrated voltage pulse

The calibration procedure works as expected. The obtained signal is now a positive pulse in the correct voltage range instead of the negative measured pulse, and the shape of the pulse changed as well. Still, this calibration procedure added ringing around the voltage peak of the obtained signal. The reason is the calibration setup that was used. This setup consists not only of the measurement module, but also includes the ESD-testchip with bond-

wires and the long ESD-input transmission line (chapter 3). This ringing is caused by the improper location of the calibration reference plane, as was explained in section 4.4.1. This is illustrated by comparison of the 'calibrated' result with the original reference plane (Figure 4.9) and the result with a shifted reference plane (Figure 4.10). In the last version, no ringing is visible at the voltage peak.
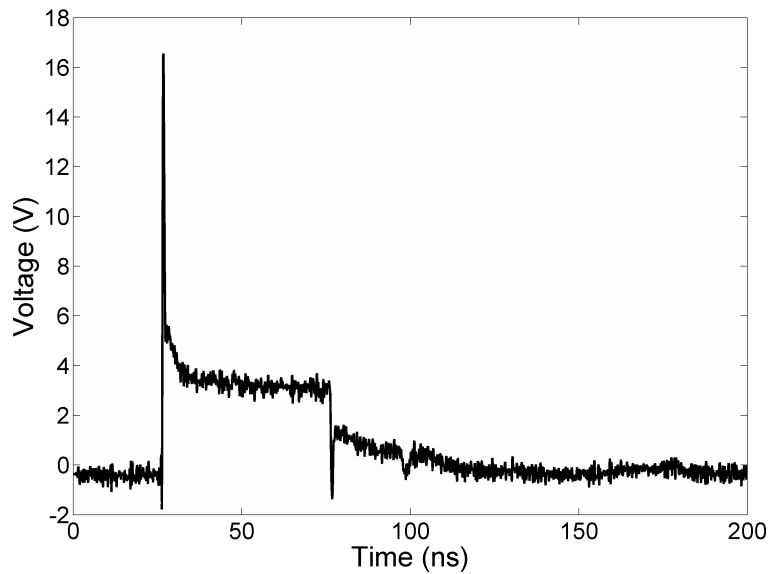

Figure 4.10: Calibrated voltage pulse with shifted reference plane

4.5 Conclusion

The calibration procedure successfully compensates the measurement data with the frequency characteristic of the measurement module. It uses the information stored in S-parameters of the measurement probe at non-uniform frequencies, to compensate for the probe response in the time domain measurement signal. For succesful calibration, these S-parameters need to be obtained according to the constraints stated in section 4.4.1. Also, a K-factor was introduced to put a limit on the noise amplification.

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5
Miniaturisation

In the previous chapters, a measurement setup for on-chip voltage wave-forms and a measurement PCB prototype have been presented. This PCB has two major drawbacks: each time another ESD protection needs to be evaluated, an application specific PCB is to be made, including the presented measurement solution. Also, a second PCB is required to perform the calibration, which is costly and results in calibration errors. In this chapter, more information is given on the integration step of the measurement solution in an ESD waveform measurement probe, which can be used and calibrated independent of test structure.

5.1   Measurement probe design

A measurement probe is a small device that transports information at the probe tips to the input port of an instrument without influencing the device-under-test. The wave sampling measurement probe is a voltage probe for operation in EMC hostile environments, some of which are generated by ESD-signals. To cope with these conditions, the probe consists of a small measurement circuit and an optical connection. Although these parts have been thoroughly described in the previous chapters, some problems, inherent to the design of a miniature measurement probe, haven't been mentioned:

- Measurement reference: The voltage waveform needs to be measured in relation to a reference voltage. In the test setup described in section 3.2, the PCB ground was chosen as reference. In most miniature test setups, there will not be a stable, absolute reference available. As a probe is test setup independent, the measurement reference will need to be redefined.

- Fiber alignment: The measurement probe needs a fiber connection. A mechanical solution is required to align the VCSEL to the fiber.

- Electromagnetic coupling: As this probe will be used in an EMC hostile environment, the influence of electromagnetic coupling due to ESD signals needs to be minimized.

Each of these problems is addressed in the paragraphs below.

5.1.1   Measurement reference

As mentioned before, a test setup independent reference for voltage measurements is required. In most commercial probes, this is provided via a ground pin with a low impedance.
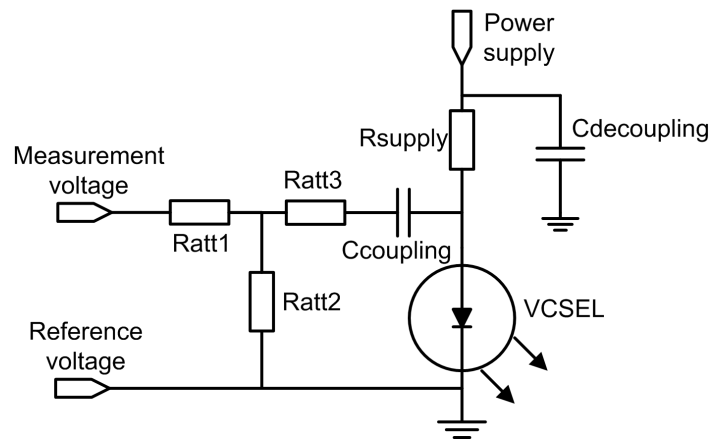

Figure 5.1: Measurement solution circuit

In the test setups presented in the previous chapters the ground plane was also used as reference. In Figure 5.1, it is clear that the measurement reference is directly connected to the negative supply pin, indicated in the schematic by the ground symbol. In this way, the measurement reference imposes the voltage of the negative power supply pin on the DUT, hereby

influencing this DUT. This can be omitted by using the differential voltage measurement circuit presented in Figure 5.2.
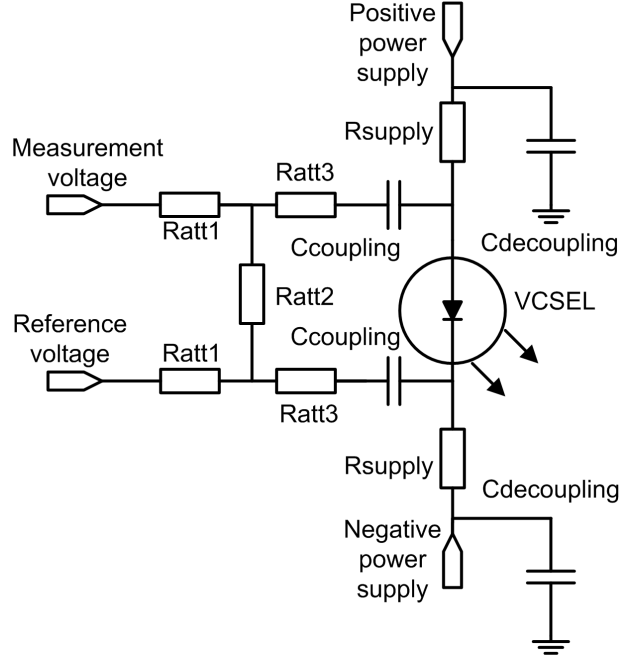

Figure 5.2: Differential measurement solution circuit

This circuit differs from the differential current probe, presented in section 2.6.1, as an extra attenuator step is added. The AC VCSEL current can be approximated by:

$$I_{VCSEL} \approx \frac{R_{A2}}{\left(2R_{A1} + R_{A2}\right)\left(2R_{A3} + R_{VCSEL}\right)} \qquad (5.1)$$

and this circuit's input impedance by:

$$Z_{IN} \approx 2R_{A1} + R_{A2} \qquad (5.2)$$

if:

$$R_{VCSEL} << 2R_{SUP} \qquad (5.3)$$

and

$$R_{A2} << 2R_{A3} + R_{VCSEL} \qquad (5.4)$$

at frequencies where the coupling and decoupling capacitors can be ignored. This way, if the resistor values are well chosen, a differential voltage measurement probe can be made with the required attenuation and input resistance.

5.1.2   Fiber alignment

A photodetector converts an optical signal into a current waveform, which is then transformed into a voltage signal by a transimpedance amplifier. This way an incident optical signal can be displayed by means of an oscilloscope. The amplitude of this resulting waveform is directly proportional to the power of the optical signal reaching the photodetector. For an optimal conversion, the optical beam has to be directed towards the photodetector. This beam is generated by a VCSEL and can be guided from the VCSEL to the detector by means of an optical fiber. This setup is depicted in Figure 5.3.
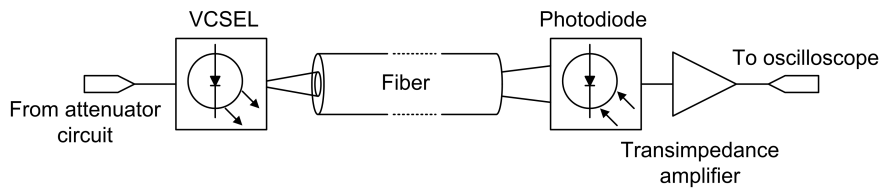

Figure 5.3: Optical setup

Although this light is directed via a fiber, there are multiple phenomena that cause optical power loss in this optical link. These can be reflections at interfaces, power loss inside the fiber or just plain power loss by directing (parts of) the laser beam alongside the fiber core. In this paragraph this power loss is described. As the properties of the optical setup have a major influence on this power loss, first a detailed description of the optical setup is presented.

The setup consists of a 10 Gbps 850nm VCSEL with a 9 μm diameter and a photoreceiver that is pigtailed to a multimode fiber. This graded index fiber has a 65 μm core, a numerical aperture of 0.27 and an attenuation between 2.7 and 3.2 dB/km. As this fiber is pigtailed to the photoreceiver, perfect fiber alignment will be assumed at this end. The other end of this fiber will be aligned to the VCSEL. As the target fiber length is below 10 meters, attenuation is of no concern. As the bandwidth-distance-product of this fiber is between 160 and 400 MHz*km, neither is modal dispersion. As a short multimode fiber is used, the output power distribution is determined

by the launching optics and fiber perturbations. This can result in non-reproducible tests as the received optical power by the photoreceiver can be dependent of the curbs in the fiber. In this case, a mode scrambler is used to distribute the light into a distribution of modes that will remain stable over long distances. It exhibits a uniform output intensity profile independent of the input mode volume or modal excitation condition. A cheap and simple way to perform mode scrambling is by introducing small bends in the fiber (Figure 5.4) [1]. The result of mode scrambling is given in Figure 5.5 [2]. This is used in this test setup.
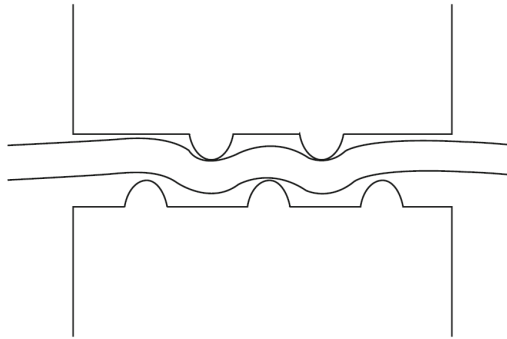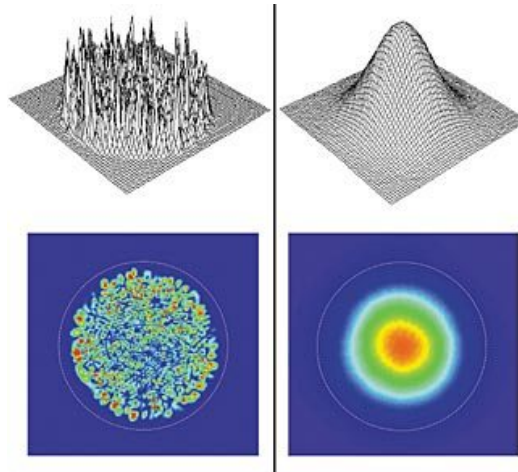

Figure 5.4: Mode scrambler

Figure 5.5: Before (left) and after mode scrambling (right)

As perfect alignment can be expected at the photoreceiver side due to the used FC connector, misalignment can only occur at the VCSEL-side of the

fiber. The effect of lateral and angular misalignment at this interface is discussed below. To simplify this discussion, the laser beam is assumed to be perfectly perpendicular to the laser plane and no beam divergence is taken into account. Beam divergence is then afterwards added to the discussion.

Lateral and angular misalignment between fiber and VCSEL are displayed in Figure 5.6. In the following calculations, it is assumed that the laser light is unpolarised and that a silica fiber, with a refractive index of 1.45, is used in an airy environment. At both interfaces, at both ends of the fiber, only one reflection is taken into account. It is assumed that this reflected amount of light will never find its way to the photoreceiver. This results in a higher boundary on the power loss.
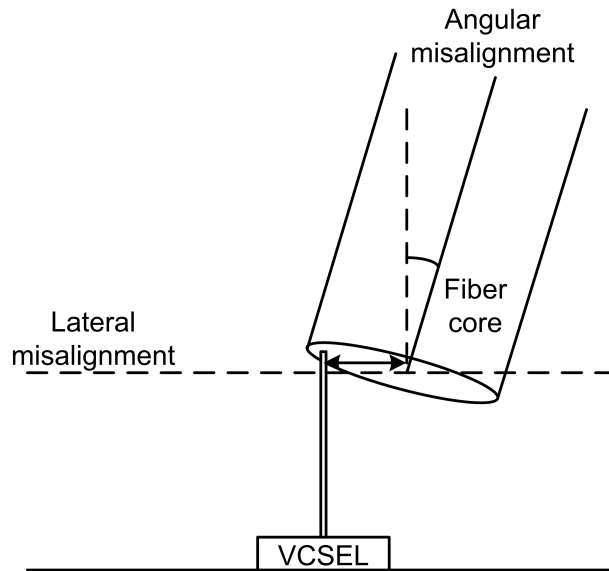

Figure 5.6: Angular and lateral misalignment errors

5.1.2.1   Angular misalignment

Angular misalignment can result in two types of power loss:

- power loss at the air-fiber-interface due to reflections

- power loss in the fiber itself

At first, power loss at the air-fiber interface is discussed. Reflection and refraction can be described by Snell's law and the Fresnel equations [3].

Snell's law defines the angle of the refracted beam as:

$$\frac{sin\theta_1}{sin\theta_2} = \frac{n_1}{n_2}$$

(5.5)

with θ_1 the angle of the incident beam in medium 1, θ_2 the angle of the refracted beam in medium 2 and n_X the refractive index of medium X. The angle of the reflected beam is given by:

$$\theta_R = -\theta_1$$

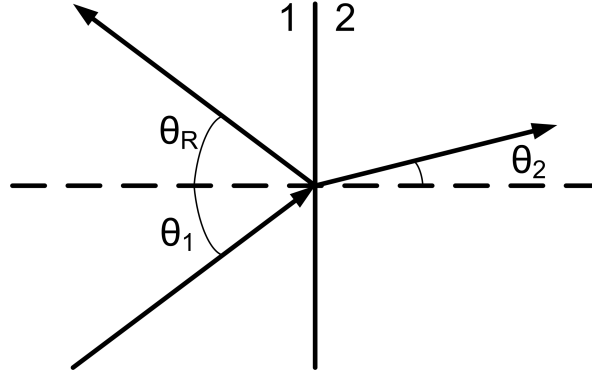(5.6)

This is illustrated in Figure 5.7.

Figure 5.7: Snell's law

The Fresnel equations provide the relationship between the power of incident, reflected and refracted optical signals. The media are assumed to be non-magnetic, which is the case in this application. The reflectance R and transmittance T are the fractions of the incident power which are respectively reflected and refracted by the interface. These properties are angle and polarisation dependent. For s-polarised light, the reflectance R_S is given by:

$$R_S = \left(\frac{n_1 cos\theta_1 - n_2 cos\theta_2}{n_1 cos\theta_1 + n_2 cos\theta_2} \right)^2$$

(5.7)

or

$$R_S = \left[\frac{n_1 cos\theta_1 - n_2 \sqrt{1 - \left(\frac{n_1}{n_2} sin\theta_1 \right)^2}}{n_1 cos\theta_1 + n_2 \sqrt{1 - \left(\frac{n_1}{n_2} sin\theta_1 \right)^2}} \right]^2$$

(5.8)

For p-polarised light the reflectance R_P is given by:

$$R_P = \left(\frac{n_2 cos\theta_1 - n_1 cos\theta_2}{n_2 cos\theta_1 + n_1 cos\theta_2} \right)^2 \qquad (5.9)$$

or

$$R_P = \left[\frac{n_2 cos\theta_1 - n_1 \sqrt{1 - \left(\frac{n_1}{n_2} sin\theta_1 \right)^2}}{n_2 cos\theta_1 + n_1 \sqrt{1 - \left(\frac{n_1}{n_2} sin\theta_1 \right)^2}} \right]^2 \qquad (5.10)$$

As unpolarised light consists of an equal amount of s- and p-polarised light, the reflectance R is given by the average value of R_S and R_P. Due to conservation of energy, the transmittance of unpolarised light T is given by $1 - R$. In Figure 5.8, the power loss at each interface and cumulated power loss is given for various incident angles.
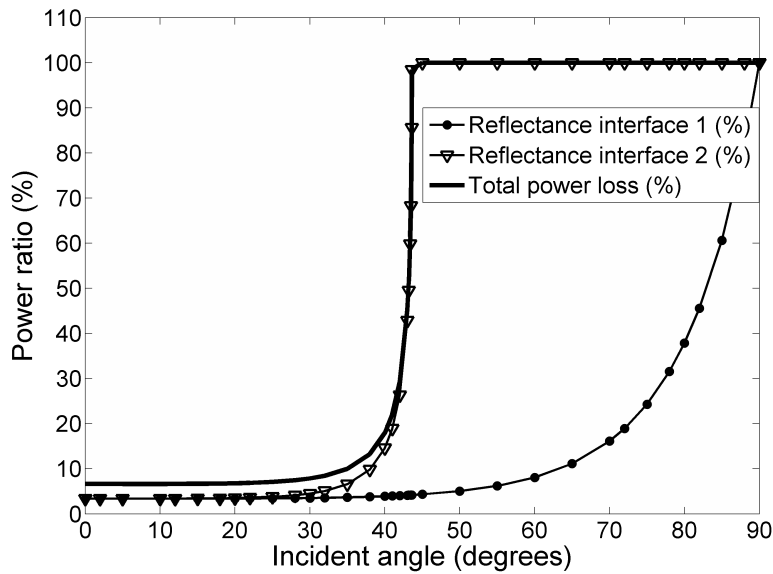

Figure 5.8: Power loss due to reflections at the two fiber interfaces

There is a minimal power loss of 6.6% which can be achieved with perfect angular alignment. At 30 degrees of misalignment there is 7.8% power

loss, which rapidly grows to full power loss at 44 degrees, as the area of total internal reflection is entered at the second interface. For negligible extra power loss, the maximum incident angle is set at 30 degrees.

As has already been mentioned before, there is a second type of power loss due to angular misalignment. This can pose an extra restriction. If an optical beam enters the fiber with a low incident angle, it is fully reflected at the sides of the fiber as it is right in the total internal reflection angle range of the fiber core cladding interface at the fiber sidewall. This way it can propagate through the fiber with very low losses. If this incident angle becomes too large, the fiber starts to leak light. There is no total internal reflection anymore at the sidewalls, greatly increasing the optical power loss in the fiber. The acceptance angle θ_{max} is a function of the refractive index of the fiber core n_1, the fiber cladding n_2 and of the test environment n. It can be calculated via the numerical aperture NA of the fiber.

$$NA = \sqrt{n_1^2 - n_2^2} = n sin\theta_{max} \qquad (5.11)$$

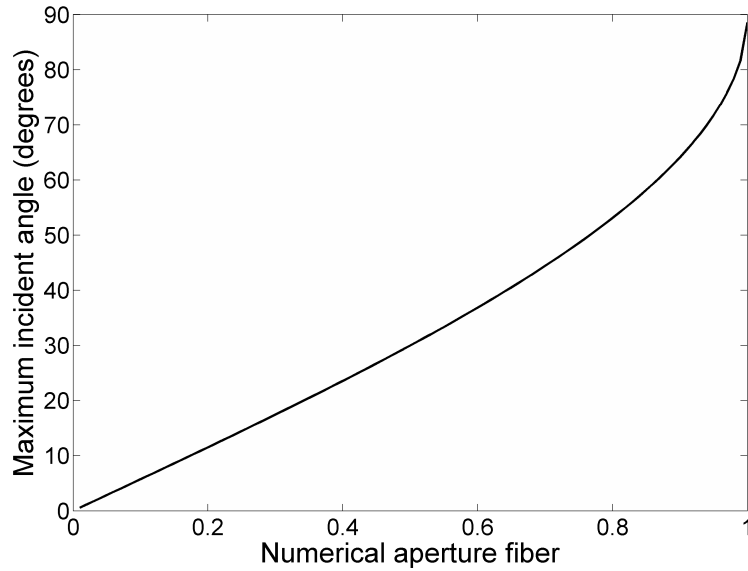In Figure 5.9 the acceptance angle is displayed for a fiber surrounded by air (n = 1.0003).

Figure 5.9: Acceptance angle for a fiber surrounded by air (n = 1.0003)

If the fiber coupled to the photodetector has a numerical aperture of 0.27, the input angular misalignment limitation becomes 15.6 degrees. As in an optical system, the numerical aperture of a cascade is equal to the smallest numerical aperture in the cascade, the use of another fiber in cascade to the used fiber, will result in the same angular misalignment limitation. The maximum angular misalignment becomes 15.6 degrees, which corresponds to a power loss of 6.7%.

5.1.2.2 Lateral misalignment

Another source of signal power loss is lateral misalignment of the fiber and the VCSEL. The ideal lateral position of a fiber is reached when the laser beam is directed at the center of the fiber core. If this fiber core is large compared to the beam width, the core is illuminated by the complete optical beam. This results in maximum signal propagation. If the fiber shows a large lateral misalignment, the beam can partially or completely miss the fiber core, which can result in complete power loss. A small lateral misalignment can still lead to maximum signal propagation if the complete beam is still directed into the fiber core. The maximum lateral misalignment error that can be made without extra power loss is

$$E_{lateral} = \frac{D_{FiberCore}cos\theta_{incident} - D_{VCSEL}}{2} \qquad (5.12)$$

where D_{VCSEL} is the diameter of the active area of the VCSEL, which approximates the beam diameter and $\theta_{incident}$ is the angular misalignment of the setup. For the application at hand, the core and VCSEL active area have a diameter of respectively 65 μm and 9 μm. This results in a maximum lateral misalignment error of 26.8 μm with an incident angle of 15.6 degrees.

5.1.2.3 Beam divergence

In the previous discussion, beam divergence wasn't taken into account. This is further discussed in this paragraph.
Each optical beam will at some point diverge. Although laser beams are known for their low divergence, they will still diverge. This divergence is characterised in the beam divergence angle laser property. This is the angle at which the field intensity drops at 1/e^2 of its axial value. As the effect of extra angular misalignment due to beam divergence is hard to describe analytically, the results that have been mentioned earlier can be used as estimation of the received power. The reason is the laser beam, which can

be approximated by a Gaussian beam, contains the majority of its power near its axis of symmetry.

The maximum lateral misalignment error including beam divergence can be described as:

$$E_{lateral} = \frac{D_{FiberCore}cos\theta_{incident} - D_{VCSEL}}{2} - Htan\theta_{Div} \quad (5.13)$$

with H the height of the fiber interface center above the VCSEL plane and θ_{Div} the laser beam divergence angle. In Figure 5.10, the lateral misalignment tolerance is presented as a function of H for 17 and 30 degrees of beam divergence angle and both 0 and 15.6 degrees of maximum angular mismatch. These beam divergence angle values have been chosen as the VCSEL has a beam divergence angle between 17 and 30 degrees.
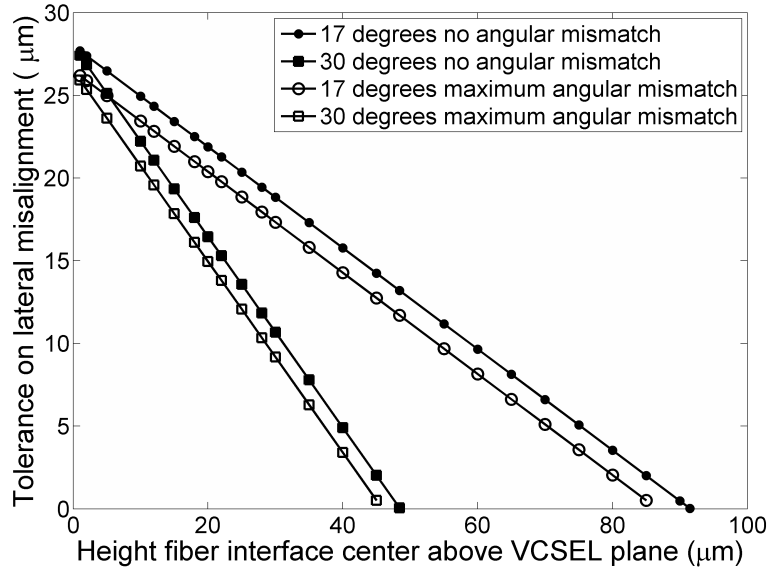

Figure 5.10: Lateral misalignment tolerance as function of the height of the fiber interface center above the VCSEL plane

Although it is possible to meet the mechanical alignment requirements mentioned above, the use of a pigtailed VCSEL is preferred. The main advantages of in-house alignment are limited cost for high numbers and multiple fiber alignment. As the cost of pigtailed lasers is low and only one fiber will be used at the same time, a pigtailed VCSEL is preferred.

5.1.3   Electromagnetic coupling

The measurement probe is to operate in an EMC-hostile environment, more specifically nearby ESD signals. Therefore, it is important to determine how well the probe will withstand interference from these ESD signals. In the paragraphs below, both the amount of magnetic coupling as the effect of shielding are discussed.
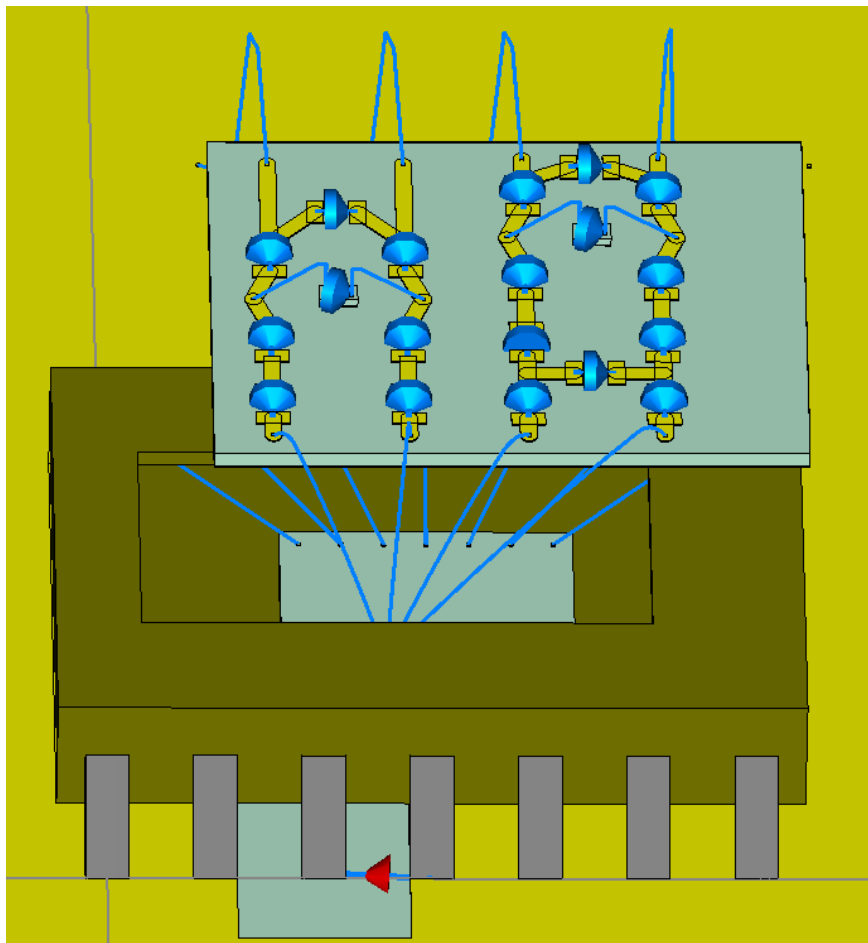

Figure 5.11: Module with two wave sampling solution circuits and a test structure in a SOIC-14 package

The electromagnetic field of most devices can be regarded as a combination of fields generated by electric and magnetic dipoles. In the near field of such

a device both the electric and magnetic field vary with $1/r^x$ with $2 < x < 3$ and r the distance between the device and the point-of-interest, depending on the structure-under-test. In the far field, both the electric and magnetic field are directly proportional to $1/r$. Also, the amount of crosstalk between two devices is highly dependent on the orientation of both devices [4]. Because of these reasons, the interference from ESD signals on the measurement probe was determined by means of a 3D-EM field simulation of the probe structure. The simulated probe structure is presented in Figure 5.11.

In this figure, a module with two measurement solution circuits is depicted together with a test structure in an SOIC-14 package. Both measurement solutions are connected to the test structure via bondwires. The blue arrows represent passive components that make the measurement solution circuits. These circuits differ in the number of attenuator stages. The VCSEL is represented by an 80 Ω resistor, and is connected via bondwires. As VCSEL geometry, the geometry of one VCSEL of the Raycan VCSEL array has been used. The power supply is represented by bondwires to the setup ground plane, while decoupling is added on the module. The module itself is implemented on a double layer board with a ground plane on the bottom and the two measurement solution circuits on the top layer.
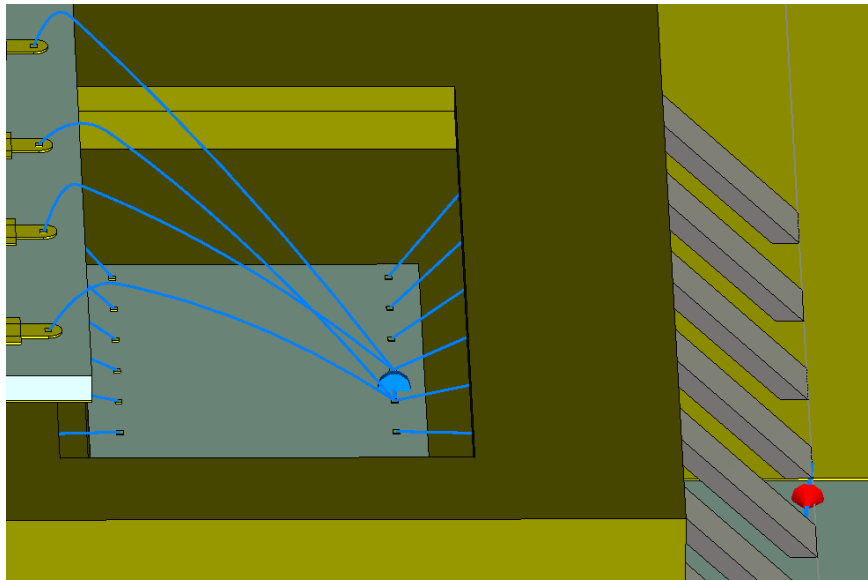

Figure 5.12: Close-up of the device-under-test, ESD-path and bondwire connections

In Figure 5.12, a close-up of the DUT, the ESD-path and the bondwire connections is shown. The current source, represented by the red arrow, generates the ESD-pulse, which is transported via the package pin and the attached bondwire to the DUT. This DUT is the passive component represented by the blue arrow. Then this pulse is led back to the setup ground plane via another bondwire and package pin. Each wave sampling circuit is connected to the DUT by two bondwires of 4 mm length with a loop height of 0.2 mm. This way, the voltage across the DUT can be probed.

5.1.3.1 Inductive coupling

Before using this setup to estimate the inductive coupling between ESD-path and measurement module, the transient simulator was tested by simulating this circuit with an ESD-signal on a DUT of 2 Ω and 1.3 nH. The used attenuators have a voltage attenuation of about a factor 55 (left) and a factor 1000 (right). The resulting waveforms are depicted in Figure 5.13 to Figure 5.16. In Figure 5.13 and Figure 5.14, the current and voltage pulse across the DUT is shown, while Figure 5.15 and Figure 5.16 present the voltage waveforms at the VCSEL inputs.
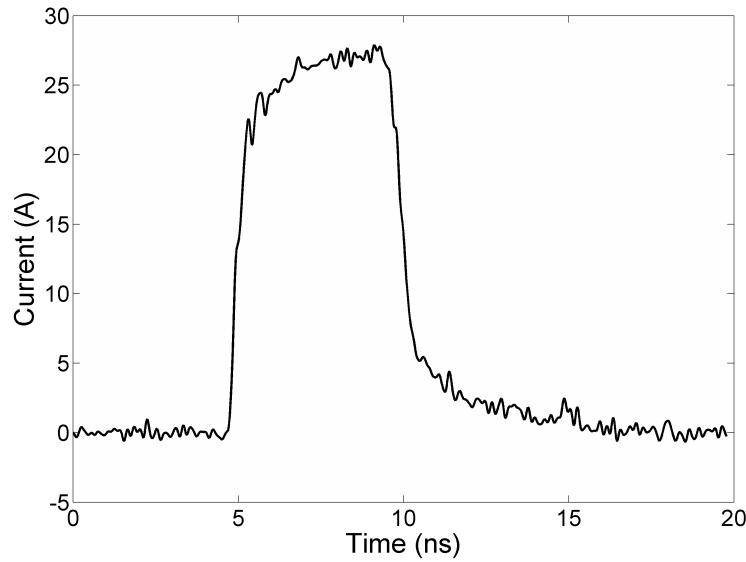

Figure 5.13: Current signal through the DUT

The shape of the measured voltage pulses resembles to a large extent the voltage waveform across the DUT. This resemblance is also visible in the
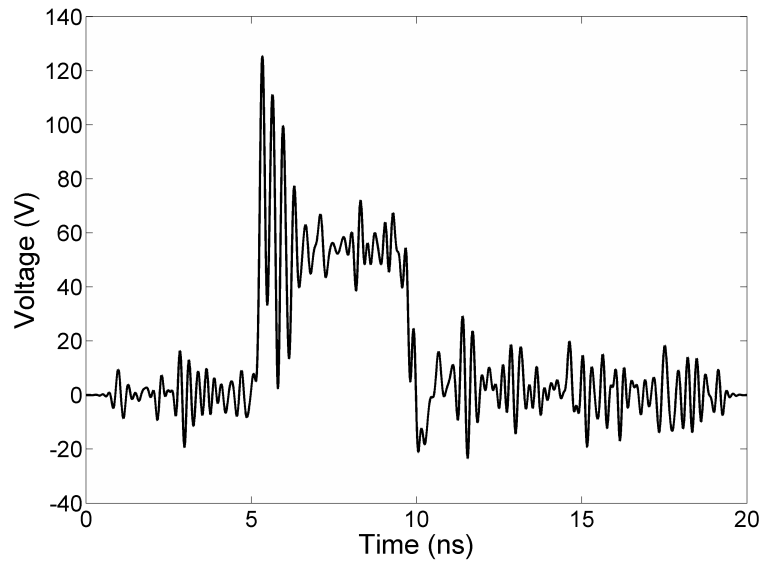
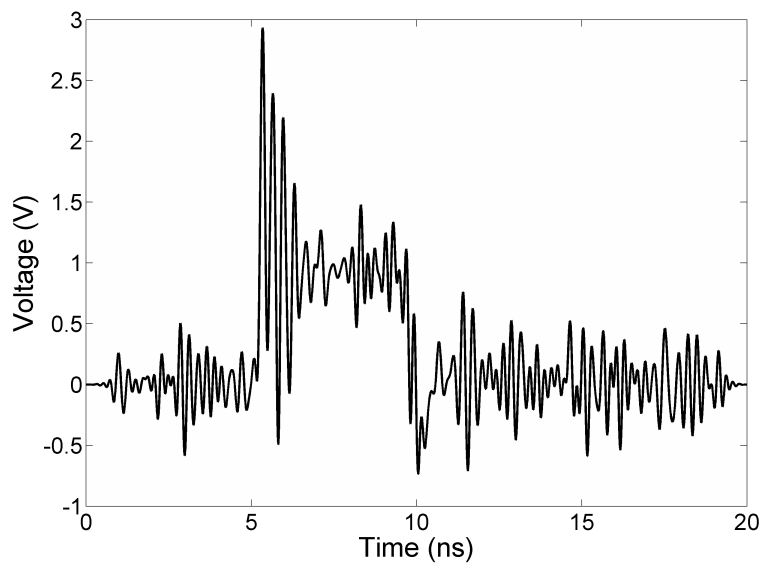Figure 5.14: Voltage signal across the DUT

Figure 5.15: Voltage signal across measurement solution circuit VCSEL with voltage attenuation 55
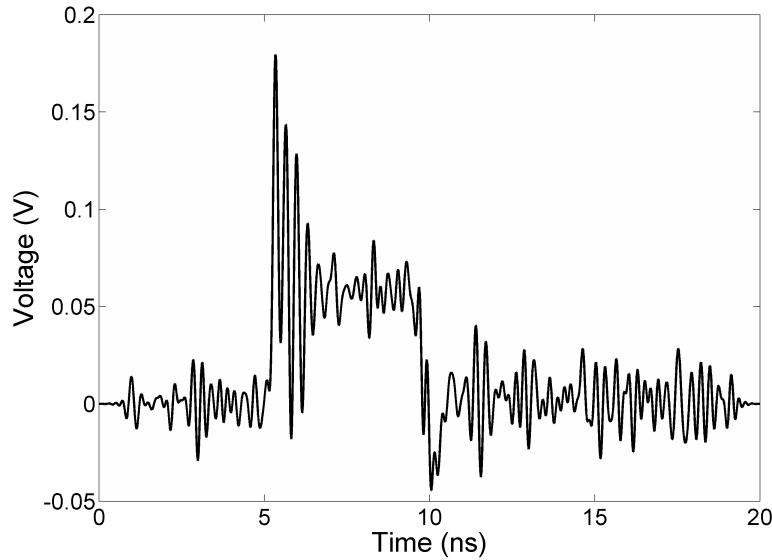
Figure 5.16: Voltage signal across measurement solution circuit VCSEL with voltage attenuation 1000

frequency domain (Figure 5.17), where the main difference between the voltage signals is the attenuation. This demonstrates the correct operation of both simulator and voltage probe.

Still there is an extra inductive component visible in the output. This can be clearly visualized if the obtained waveforms are rescaled until the same peak value is reached. This is shown in Figure 5.18. In this figure, the original voltage pulse across the DUT is shown as a thick line, while the obtained measurement signals are represented as thin lines.

It can be seen that the voltage waveforms obtained at the two VCSELs are similar, while there is a large difference with the original voltage wave-form. This is due to an extra inductive component situated near the DUT, as inductive components near the attenuators would result in different mea-surement waveforms across both VCSELs. This inductive component can be mainly imputed to the test setup and the simulator. In CST microwave studio, passive components are modelled as infinitely small, ideal com-ponents that are connected to their respective interfaces via bondwires [5]. This means that the earlier used voltage across the DUT is actually the volt-age across the infinitely small, ideal component, excluding the connecting bondwires. These bondwires are included in the obtained waveforms across the VCSELs, and have a total inductance of about 300 pH. This can explain
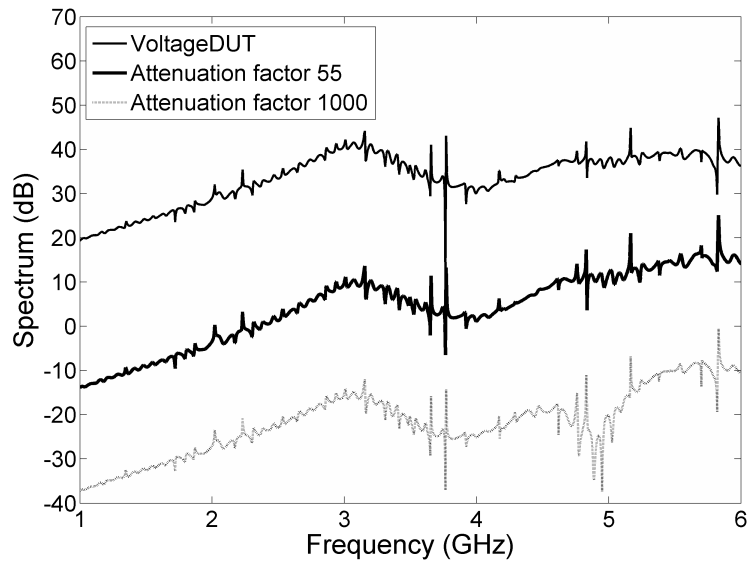
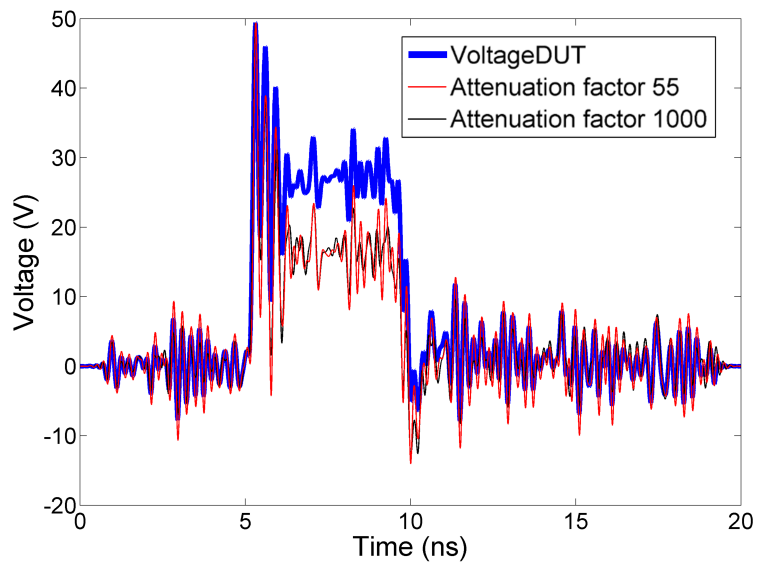Figure 5.17: Spectra of voltage signals

Figure 5.18: Rescaled voltage signals

the difference in waveform. The magnetic coupling can be obtained by connecting both input pins to the same DUT-interface. The voltage pulses across the VCSELs are then directly caused by coupling.
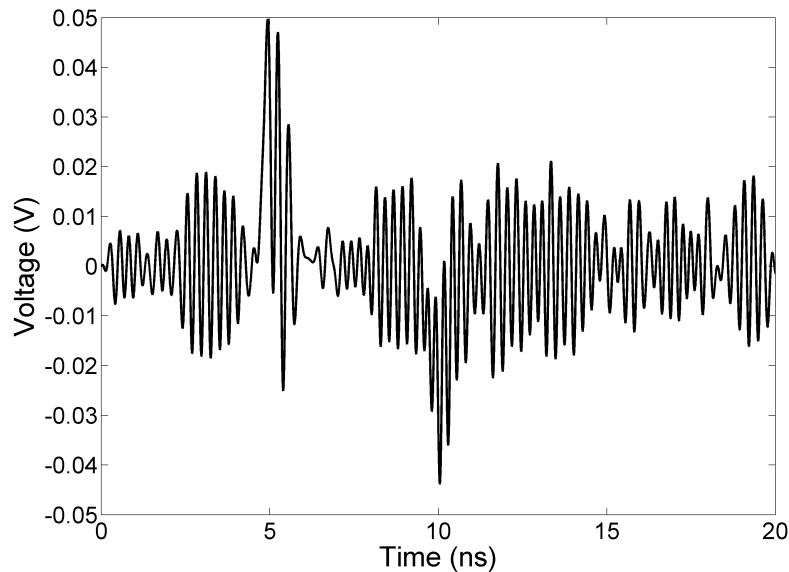

Figure 5.19: Voltage signal across the VCSEL caused by coupling (attenuation: 55)

When this signal (Figure 5.19) is referred back to the input, this corresponds to a signal with a peak voltage of 3 V in series with the DUT for the current pulse depicted in Figure 5.13. This makes an inductive coupling of 40 pH. As this depends on the geometry of the DUT, this effect can't be reduced by calibration. Only a smaller differential probe tip will reduce the amount of inductive coupling. Although this effect is visible in ESD-measurement results with high currents, this is a vast improvement in comparison with the currently used measurement systems as this mutual coupling (order tens of pH) is negligible to the inductance of the bondwires of the DUT, which is in the order of nH.

5.1.3.2   Shielding

The main focus of the previous discussion was the inductive coupling from DUT to the measurement probe. Another source of interference is capacitive coupling. As is the case with a magnetic field, the electric field reduces

with the distance to its source. In contrast with this magnetic field, there is another popular way to greatly reduce the electric field over multiple decades: shielding. In the test setup described in the previous paragraphs, a conducting plane has been used at the bottom side of the module PCB. This has its effect on the measurement results as the total amount of coupling reduces with 30%. To further reduce the amount of capacitive coupling between DUT and probe, the shield presented in Figure 5.20 has been added to the setup.
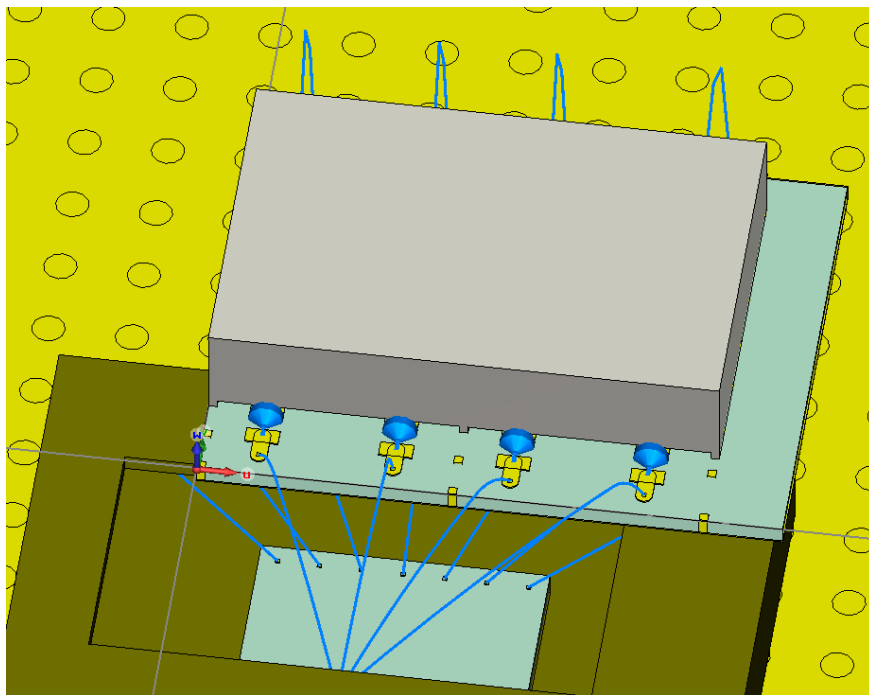

Figure 5.20: Module with two measurement solution circuits and shield

This shield is made of a perfect conductor and is connected at multiple points to the conducting plane at the bottom of the test setup. Although the sensitive parts of the measurement circuits are now situated in a Faraday's cage, the amount of coupling isn't reduced any further at the measurement frequencies. Only at higher frequencies, this cage makes a difference of a factor 4. Although simulation results show that this cage has no effect in the measurement range in this setup, the use of a cage is encouraged as it reduces the electric fields that are generated by other sources in the test area and by multiple reflections and as it allows a higher manoeuvrability of the

probe (e.g. reducing the coupling if the probe is turned upside down).

5.2   Measurement probe integration

In the previous section, three main problems have been addressed. This information can be used in design of the measurement probe. As the development of the measurement probe is currently ongoing, no further realisation details will be revealed in this work.

5.3   Conclusion

In this chapter, the miniaturisation step has been studied. This resulted in the isolation of three problems: the measurement reference, laser alignment and electromagnetic coupling. These have been discussed in-depth. The obtained results are currently used in development of a measurement probe with a minimal amount of electromagnetic interference for voltage and current waveform characterisation of ESD pulses.

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[3] B.E.A. Saleh and M. C. Teich. *Fundamentals of Photonics.* Wiley-Interscience, 2007.

[4] J. J. Goedbloed. *Elektromagnetische compatibiliteit.* Kluwer, 1996.

[5] *CST - Computer Simulation Technology website.* http://www.cst.com/.

6

Conclusion and future work

6.1 Conclusion

On-chip ESD protection circuit design is an integral part of the development of almost every single IC chip. With faster IC technologies, the need for successful protection devices grows further in importance. In the last decades, there has been an essential evolution in ESD measurement tools to support the ESD design engineer.

In this work, the research foundations were laid for the development of a new type of measurement probe, able to characterize ESD voltage and current pulses directly on the input pads of the ESD protection device. To cope with the challenges of performing accurate, single-shot waveform measurements in an EMC-hostile environment, a 'divide and conquer' technique was presented; Instead of using direct digitization, the waveform of interest is captured and transported to a commercial oscilloscope located in an EMC-clean environment. This resulted in a measurement architecture based on an optical link, as optical signals are immune to electromagnetic interference. In this work, it was proven that VCSEL-based optical links can be made with a more than sufficient bandwidth and dynamic range to succesfully reproduce the signal of interest in an EMC-clean environment. Simulations indicated that a probe based on this measurement architecture would result an inductive coupling in the order of tens of pH, which is a vast improvement over the nowadays available measurement methods. Another

advantage is that low power and low cost probes can be designed due to the use of VCSEL diodes, which have a low cost and high efficiency compared to other laser diodes. Also, this optical link is a galvanic isolation between the low cost probe and the high cost photoreceiver and oscilloscope. This way, should the low cost probe be destroyed during ESD-measurements, the expensive measurement instruments at the other side of the link are still protected. Furthermore, these probes are independent of the chip technology of the device-under-test, resulting in maximum reusability.

The voltage waveform is applied to the laser by means of a miniature, differential, resistive attenuator with a high input impedance. The current waveform can then be derived from the measured voltage waveform via the presented software algorithm. It is demonstrated that this architecture can be used to measure the voltage waveforms on the input path of a real ESD protection device with the required specifications. To obtain an unscaled, accurate measurement result, a probe calibration procedure was presented, and more information was given on the problems that come with the miniaturisation step needed to make a miniature ESD measurement probe. This probe will provide more accurate information on the response of the protection device and bring invaluable insights in future ESD problems.

6.2   Future work

This dissertation presents a new measurement architecture that can be used to perform single shot, on-chip ESD waveform measurements in an accurate way. Nonetheless, some further development needs to be done before this architecture is realized in a complete commercial ESD measurement system. Next to the mechanical work, there are improvements that can be made to the measurement probe. In this work, a fixed attenuator is used to obtain the measurement results. If another input range is required, this results in a new probe with another attenuator. This could be avoided by using a miniature differential variable attenuator with a high bandwidth, input impedance and common-mode rejection ratio to drive the laser. These attenuators are best custom designed on chip as nowadays there are no integrated differential attenuators that meet the high bandwidth and input impedance requirements commercially available. A next improvement can be made in the power supply of the probe. The output signal is directly proportional to the bias current and therefore the power supply. Although this power supply is decoupled, the coupling between ESD pulse and measurement probe can be further reduced by again using optical signals to empower the probe. As a VCSEL diode needs a very limited amount of bias current, this current can be delivered by a photodiode that is driven by

another laser. Once the measurement probe has been realised, the probe needs to be calibrated. Therefore, a calibration structure needs to be designed to correctly compensate the voltage-to-voltage transfer function of the measurement probe, using the procedure presented in chapter 4. This way, the probe can be calibrated independent of the DUT and used as calibrated measurement probe.