# Poly-Ge/poly-CdSe dunne-filmcircuits voor op glas geïntegreerde aansturing van vlakke beeldschermen

# Poly-Ge/poly-CdSe thin-film circuits for on-glass integrated driving of flat-panel displays

## English Summary

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1.1 Context ..... 13
Flat-panel displays and active matrix addressing ..... 13
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Interconnection problems and integrated drivers ..... 19
*The problem of connecting a display to its peripheral electronics becomes more serious with increasing display resolution. Different traditional methods are discussed and the concept of integrated drivers is introduced, along with the pros and cons. The advantages of CTFT vs. nTFT logic are summarized and a brief overview of the current realisations in this field is given.*
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*The final aim of this doctoral research project is to show the feasibility of an active matrix display with integrated thin-film driver circuitry. The originality is the use of the semiconductors CdSe and Ge, which we expect to be superior — for this purpose — compared to poly-Si. Some subtasks can be defined, such as converting the existing top gate poly-Ge/poly-CdSe technology to a bottom gate technology and optimizing the circuit performance in this new technology.*
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Design of the technology (see chapter 2) ..... 24
*A bottom gate Ge-TFT, compatible with the existing CdSe active matrix technology has to be designed.*
Circuit design (see chapter 3) ..... 24
*Knowing the achievable TFT characteristics we can design a suitable circuit. The literature shows some possible ways to go. The essential building blocks can be realized and characterized first. They can also be simulated.*
Mask design (see chapter 5) ..... 24
*It is necessary to design 3 mask sets : one to optimize the Ge-TFT's, one to study the building blocks and a final one to show the operation of the integrated drivers. We cannot use most of the powerful CAD-tools that were designed for the Si technology.*

Processing ..... 25
*Most of the work, but not much to say about.*
Evaluation (see chapter 6) ..... 25
*The realised devices and circuits will be evaluated in several ways.*

Chapter 2 : Technology design ..... 27
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The existing technology for CTFT circuits ..... 27
*Igor De Rycke and Jan Doutreloigne have used a top gate technology for realizing nTFT resp. CTFT circuits. This had certain advantages for optimizing the semiconductor properties. The technology of Doutreloigne is described.*
The standard poly-CdSe active-matrix technology ..... 30
*This technology is described and it is explained that a bottom gate (plus a partial top gate) is essential because of the light sensitivity of CdSe.*
Incompatibilities between the two technologies. ..... 31
*It is shown that it is virtually impossible to join the existing CTFT and pixel technology on the same substrate.*
2.2 Proposed new technology ..... 32
*The initially proposed unified technology is described. The number of lift-off steps is minimized to avoid problems with micro-burs and the total number of mask steps is kept low.*
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*Several technological problems have necessitated alterations of the new technology. There were problems with the Al gates. Using Cr created new problems. TiW proved to be a good alternative. The complicated combined semiconductor/source/drain etching step also caused problems, which were solved by re-introducing some non-critical lift-off steps. A curious problem was the fact that InAu no longer made good contact on Ge, which it did in the past. I was not able to explain this in a short term and for pragmatic reasons I had to find another source/drain-material for both CdSe and Ge. Ti works on Ge, but not on CdSe. TiW works on both, provided some thermal annealing steps are carried out.*
2.4 The $V_T$-problem of Ge ..... 36
*Another mysterious problem is the fact that bottom gate Ge-TFT's have a totally different threshold voltage behaviour than their top gate equivalents. A lot of time was invested in tuning several process parameters in order to obtain the same characteristics as in the top gate technology. Unfortunately this did not lead to success. Some interesting conclusions can however be drawn from these experiments. There are also some ideas that could not be worked out, because of the time scheme that had to be followed.*
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*Just what the title says.*
2.6 The eventual TFT-characteristics ..... 41
*MOSFET parameters that fit best with the resulting TFT characteristics.*

Chapter 3 : Circuit design ..... 43
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*Almost all driver circuits can be catalogued as commutators, scanners or SLB-drivers (Shift,Latch,Buffer). The difference between these is explained, as well as their typical (dis)advantages. We can also discriminate between two and multi grey level drivers, digital and analogue drivers, nMOS and CMOS drivers, ... Now follows a discussion of some interesting driver schemes that*

*have been published. [Note : it is almost impossible to summarize this discussion any further, because it is already very compact. Therefore I refer to the paper I have presented on the 1st CdSe workshop, which was in fact the base for this chapter.]*

Morin et al., 1981 ..... 45

*Oldest poly-Si driver circuit. Typical scanner. Uses memory capacitor for each column. Prone to image bending. As far as I know it was never realised.*

Malmberg et al., 1986 ..... 47

*MiniGraphics displays. Typical commutator. Analogue driver, analogue grey levels. Driver can be used for fault location. Uses CdSe as semiconductor. Was realised and works.*

Tizabi et al., 1986 ..... 47

*First CTFT driver using CdSe (and Ge). Uses sample-and-hold modules in column driver. Disadvantage is hysteresis in buffer characteristics, which limits number of grey levels. Very low number of TFT's. Row driver probably not powerful enough to prevent image bending. I suspect the circuit was never realised.*

De Rycke et al., 1988 ..... 49

*SLB with CdSe. Clocks up to 2 MHz. Digital line memory. Needs parallelism for high resolution.*

Ohwada et al., 1988 ..... 51

*Commutator with 4 grey levels. TFT's only used as switches. Lots of cross-overs in column driver. Powerful but complicated row drivers.*

Matsueda et al., 1989 ..... 51

*Hybrid scanner-commutator. 8-fold parallelism. Extremely redundant design (all pixels addressed via 2 totally independent ways). Driver circuit can be used for fault detection.*

Emoto et al., 1989 ..... 53

*Very sophisticated design. Uses parallelism without requiring pre-processing of video data. Analog RGB input. Surprisingly low number of TFT's per column.*

R. Stewart et al., 1990 ..... 54

*SLB driver with 32 grey levels. 100-fold parallelism. Uses chopped ramp type DAC's. Complicated circuitry to be realised in thin-film technology.*

Others ..... 55

*Some references to other interesting papers.*

Summarizing table ..... 55

*This table systematically summarizes the most interesting features of the referenced driver circuits.*

Solutions for the image bending problems with scanners ..... 56

*Leaving more time between consecutive lines is the classic way to do this.. A more elegant approach would be to cut the gate lines in half and use two line scanners. the right one being delayed by half a line period compared to the left one. The only disadvantage is the fact that redundancy by two-sided addressing is no longer possible.*

Methods for implementing grey levels ..... 57

*7 different methods for creating grey levels are discussed. One of them is original and uses ON/OFF subframes with different illumination intensity in order to avoid viewing angle dependence. Other methods use intermediate voltages, ON/OFF subframes with different select voltages, resulting in intermediate RMS voltages or (with fast responding LC materials) intermediate light impressions, N equivalent subframes resulting in N+1 possible grey levels, halftoning with extra TFT's or halftoning with capacitive voltage dividers.*

3.3 Discussion of chosen driver scheme ..... 60
*I have chosen a SLB-type circuit, comparable to the De Rycke type, but with complementary invertors or with depletion load invertors. Pass-TFT's are used instead of CMOS switches, because of the bad ON/OFF-ratio of the p-type TFT's. The operation of the driver is discussed in more detail. Especially the operation of the latch circuit (sense amplifier) requires some explanation.*
3.4 Simulations ..... 63
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*After choosing a driver scheme, the components have to be dimensioned in order to optimize performance. A pure heuristic way, in which all possible combinations of gate width and length, etc. are actually realised and tried out, is far too expensive and too slow. Therefore, preliminary circuit simulations are necessary. Because of the large number of simulations that have been carried out, only some of the results are presented here.*
Static invertor characteristics ..... 64
Terminology ..... 64
*The notions `stable operating points', `astable operating point', `noise margins' and `gain' are introduced. Different invertor types are shown.*
Simulation results ..... 65
*It is shown that, given our depletion type Ge-TFT's, the depletion-load invertors yield the best static invertor characteristic.*
Dynamic shift registers ..... 67
Terminology and criterion for proper operation ..... 67
*A quantity Δ that describes the `goodness' of the operation of a dynamic shift register is introduced. This allows us to use a limited number of simulations to predict the maximum operation frequency of the shift register.*
Simulation results ..... 68
*Dynamic shift registers with different invertor types and transistor geometries are simulated at different frequencies.. The resulting Δ's of all these simulations are summarized in a number of graphs. This leads to an optimum value for the transistor geometries and it predicts a maximum clock frequency of 5 MHz for the depletion-load type shift register.*
Conclusion ..... 71
*The depletion-load invertor behaves best in static both as dynamic circuits. A first indication of the ideal geometries can be given.*
3.5 Other application : SSR for bargraph-display ..... 72
*A possible application for thin-film circuits where speed is not the primary demand, is the addressing of multi-pixel guest-host LC displays, such as the bargraph-type displays. Passive multiplexing can not be used because of hysteresis in this type of LC material. Direct addressing becomes too expensive because of the high number of interconnections. Active addressing and an integrated static shift register can be fabricated with a high yield for such a low number of pixels and is therefore an attractive solution.*

Chapter 4 : A better TFT-model for simulations. ..... 75
4.1 Introduction ..... 75
*All simulations until now were performed using the SPICE Level 1 Schichmann & Hodges MOSFET model. In this chapter I propose a new, semi-heuristic, model that is an extension of this simple model, but with which the subthreshold behaviour and the superlinear `linear' region can be described.*

4.2 Static current equation ..... 75
*The Schichmann & Hodges current equations are written on one line, using the step function to account for the transitions between the different operating regions. A term representing the shunt resistance $R_0$ of a TFT is added. Then, a hyperbolic function with one parameter $V_c$ (curvature voltage) is introduced to smooth the transitions between the regions. Finally, the squares in the current equation are replaced by the exponent $\kappa$ in order to model the superlinear behaviour. The transconductance $\beta$ is replaced by B, the `preterconductance', and $\kappa$ is called the `preterconductance exponent'. The resulting equation is a single-line formula describing the current in all operating regions (including sub-threshold) and requiring only 5 device parameters.*
4.3 Dynamic behaviour ..... 78
*If we assume that the quasi-stationary approximation is valid, the dynamic effects can be described by introducing nonlinear terminal capacitances $C_{GD}$ and $C_{GS}$. These capacitances are also written as single-line formulas, requiring only three device parameters : $V_c$, $V_T$ and $C_i$, the geometric gate insulator capacitance.*
4.4 Implementation in simulation program. ..... 80
*The new TFT model was implemented as a macro circuit with 6 parameters in a modern simulation program.*
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*Some algorithms are derived to extract the 6 model parameters from measurements of $I_{DS}(V_{GS})$ characteristics. It is illustrated that in this way, it is possible to achieve excellent agreement between model calculations and measurement over a large range of voltages.*
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*Simpler than Spice level 2 or 3; better than level 1; good subthreshold description, including shunt resistance; single-line formula, easy to implement in macro circuit; continuously derivable formulas, enhancing convergence speed of calculations; only 6 well-defined parameters, no parameter redundancy; easy parameter extraction from measurements; TFT modelled as a real 3-terminal device, no need to play tricks with the substrate potential.*
Disadvantages ..... 87
*Physical interpretation of $V_c$ and $\kappa$ is not immediately clear, temperature dependence is not taken into account; often not usable for MOSFET's, because there is no substrate terminal; the hyperbolic function was arbitrarily chosen for reasons of simplicity, probably another function could yield even better results; calculations are more complicated than with the SPICE level 1 model and require more CPU time.*

Chapter 5 : Mask design ..... 89
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*4 mask sets were designed. The first one was kept very simple so no time was lost considering details which were not important yet. With this set, a usable bottom gate technology was constructed, as seen in chapter 2. The second mask set was used to test the possible building blocks of the driver circuit. Several values of the geometric TFT parameters were tried out. This design was already more complicated because I tried to vary as many parameters as the limited substrate space (2"x2") would allow. Maskset 3 was a 64x64 pixel matrix. It was a by-product of maskset 4, which comprised complete driver circuits as well as two small 8x8 pixel matrices with integrated drivers, for demonstration purposes.*
5.2 Design tools and realisation of masks; future of our mask design. ..... 90
*All masksets were designed using in-house developed CAD tools. Because the follow-up of this software can no longer be guaranteed and because the available computer*

*platforms are changing rapidly, new solutions have to be found. I give on overview of the different possibilities. The realisation of the masks was done by laser plotting (4000 dpi) on a photographic foil and subsequent photolithographic copying onto TiW coated 5"×5" glass plates.*

5.3 Detailed description of the mask sets ..... 92

*In this section the mask sets are rather thoroughly described. This is especially useful for reference during future designs of new mask sets or adaptions of the present sets. I will only comment on those paragraphs that seem interesting enough for a `normal' reader of this manuscript.*

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Herbert De Smet, November 10, 1993