A highly linear VCO for use in VCO-ADC's

Amir Babaie-Fishani, and Pieter Rombouts,

This document is an author's draft version submitted for publication to Electronics Letters.
The actual version was published as [1].

REFERENCES

[1] A. Babaie-Fishani and P. Rombouts, "Highly linear VCO for use in VCO-ADCs," *Electron. Lett.*, vol. 52, no. 4, pp. 268–269, FEB 18 2016.

A highly linear VCO for use in VCO-ADC's

Amir Babaie-Fishani, and Pieter Rombouts,

This brief presents a very simple Ring-Oscillator VCO structure for use in VCO-ADC applications. It has a greatly improved linearity compared to previously published VCO's. Measurement results of a 1Volt, 65nm CMOS prototype confirm the effectiveness of the proposed approach.

Introduction: VCO based Analog to Digital conversion has recently gained a lot of interest, because it allows relatively easy implementation of multi-bit noise shaping A/D conversion. Both closed-loop as well as open-loop implementations have been presented [1, 2, 3, 4, 5, 6]. However, whichever overall architecture is used, a key issue is the overall linearity of the actual VCO that is used as the quantiser. Most researchers have tried to solve this issue at the architectural level e.g. by calibration, feedback or signal swing reduction [4, 5, 6]. In this work, we follow a complementary approach, in the sense that we have performed a circuit level optimization of the VCO core. The resulting VCO is typically an order of magnitude more linear than prior VCO designs [2, 3, 4]. As a result further linearity correction at the architectural level may have become unnecessary or can significantly be simplified.
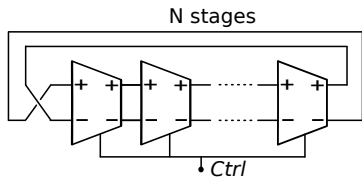
N stages

Fig. 1. Ring oscillator with N differential delay elements.

Ring oscillator input circuit: Our starting point is the well known ring oscillator (RO), shown in Fig. 1. It consists of N differential delay elements placed in a ring. For the delay element, the circuit of Fig. 2 was used [2]. It consists of 2 main inverters and 2 small auxiliary inverters. The task of the auxiliary inverters is to allign the edges of both main inverters, such that both main inverters will switch at (almost) the same time stamp (one will have a rising edge and the other a falling edge). The circuit can be tuned through its control terminal (Ctrl).
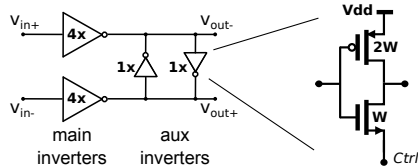

Fig. 2. Delay cell used in the ring oscillator.

For this circuit, we investigated the overall linearity. Surprisingly, the available literature guidelines are completely contradictory. Some authors claim that the oscillation frequency f_{RO} is proportional to the voltage $V_{RO} = V_{dd} - V_{Ctrl}$ over the inverters in the ring [7, eq.14]. This leads to the conclusion that direct voltage mode control is the optimal choice. Other authors claim that the oscillation frequency is proportional to the current driven into the control terminal [5, fig.4] [2, fig.4]. This suggests that direct current mode control is best. And finally some other authors claim that the oscillation frequency is proportional to the ratio of the two [7, eq.10] [5, eq.2], which does not directly lead to a simple drive strategy.

Upon investigation, it turns out that all these claims are approximately valid in a certain operation range of the RO. But the actual curves exhibit (depending on how large the tuning range is) nonlinearities of several percents. The current control performs best, but, since in most cases the input signal is available as a voltage rather than a current, this control strategy imposes the need of an additional voltage to current conversion. This voltage to current conversion adds to the power budget and introduces additional nonlinearity.

In this work we propose the simple novel mixed input structure shown in Fig. 3. The structure can be considered as a go-between of
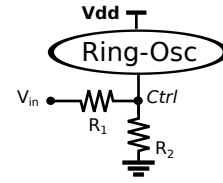

Fig. 3. Ring oscillator with resistive input stage

the current mode control and the voltage mode control. This structure has several attractive features. First, the input circuit is much simpler than transconductor based circuits that are widely used. Due to this, it has significantly better noise performance and power efficiency than transconductor based circuits. Second, the linearity of this resistive input circuit is better than the linearity of an RO with an ideal current control. To understand this, the (simulated) frequency tuning curve with ideal current control is shown in Fig. 4(a). It is clear that the curve exhibits a negative curvature. In the proposed circuit the ring current I_{RO} will be:

$$I_{RO} = -\frac{V_{in}}{R_1} + V_{Ctrl}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \qquad (1)$$

The term $-\frac{V_{in}}{R_1}$ is linear in the tuning voltage, but the term proportional to V_{Ctrl} is nonlinear. A simulation of the relation between V_{tune} and V_{Ctrl} for the case of a supply voltage $V_{dd} = 1V$ is shown in Fig. 4(b). It is clear that this curve exhibits the opposite curvature of the current mode tuning curve of Fig. 4(a). By appropriately sizing the resistors R_1 and R_2, both nonlinear effects will cancel out.
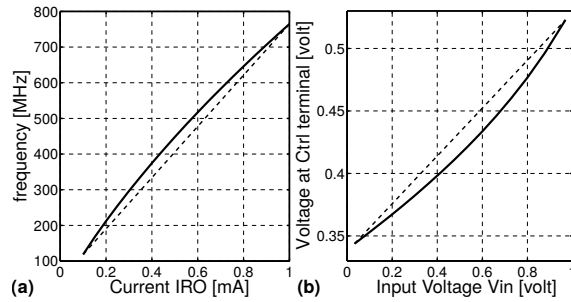

Fig. 4 *(a) Tuning curve with current control exhibiting a negative curvature and (b) Control voltage V_{ctrl} vs the input voltage curve exhibiting a positive curvature.*

In sizing the resistors there are 2 degrees of freedom: the value of R_1 and the value of R_2. The ratio R_1/R_2 should be chosen such that both nonlinear contribution cancel. In the family of circuits that we examined (where the supply voltage was 1 Volt) the optimum was very close to the case of matched resistors: $R_1 = R_2 = R$. Then, there only remains 1 degree of freedom: i.e. the value of R. This value should be sized to satisfy the desired input referred noise of the VCO.

Oscillator core design: The final step in the VCO design is the sizing of the inverters of the delay cells and the choice of the number of elements in the loop. In the case where the ring is current controlled (as is roughly the case here), the propagation delay of each cell will be more or less inversely proportional to the current and and to the total capacitive load C_{tot} seen by each delay cell. This capacitive load will consist in part of wiring capacitance C_{wire}, in part of C_{inv}, the input capacitance of the next inverter loading it and also of C_{load} the load formed by VCO phase readout circuits. This way, we can see that the oscillation frequency will behave according to:

$$f \propto (C_{tot} \cdot N)^{-1} \quad , \quad C_{tot} = C_{inv} + C_{wire} + C_{load} \qquad (2)$$

In prior work, it has been shown that it is beneficial to design the delay stages so as to achieve a minimal delay [3]. This allows to have simultaneously a relatively high oscillation frequency and at the same time a high number of stages, which leads to improved quantisation noise and bandwidth performance of the ADC. The conclusion is that the inverters should be sized as small as possible (minimizing C_{inv}). However, in a low-voltage context (as we have today), there is an

additionally important constraint: i.e. the voltage over the ring should remain sufficiently small (definitely sufficiently smaller than the supply voltage). The smaller the inverters are sized, the larger the voltage over the ring will be. The conclusion is that the inverters should be sized with the minimal size that still keeps the voltage over the ring acceptable and that the number of stages N should be chosen to obtain the desired oscillation frequency.

Measurement Results: As a proof of concept, a test circuit of the proposed RO was manufactured in the low power flavour of a 65nm CMOS technology (on a die with other test circuitry). The circuit was designed for a 1V power supply and an oscillation frequency centered around 300MHz. The resistors in the input network were $R_1 = R_2 = 770\Omega$, which were arbitrarily sized in this test circuit, which focuses on linearity and not on noise. The resulting number of stages in the design was $N = 18$ stages. The measurements reported here are for a 1 volt supply but the circuit remained operational for supply voltages as low as 0.8 volt. The measured voltage to frequency conversion curve of the VCO for a rail-to-rail input voltage sweep is shown in Fig. 5(a). Clearly, the curve is visually linear. The deviation of this curve from a best fit line (i.e. the nonlinearity error) is shown in Fig. 5(b). The worst case nonlinearity over the entire tuning range from 100 to 500MHz is ± 2.2MHz, corresponding to 0.6% of the full scale.

Fig. 6. Output spectrum of the pseudo differential VCO ADC experiment.

Fig. 7 *SNR and SNDR vs. the normalized rail to rail input level (of 2Vpp differentially).*
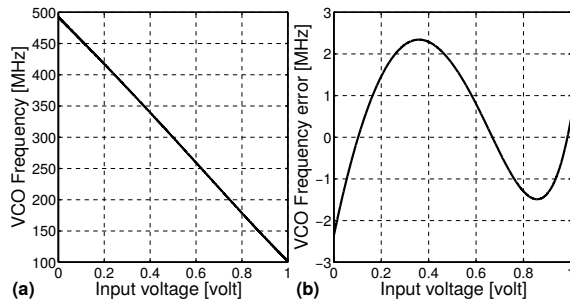
Fig. 5 *(a) the voltage to frequency conversion curve of the proposed VCO and (b) the nonlinearity of its frequency error.*

In another set of measurements, two VCO's (each on a different die coming from the same wafer) were configured as a pseudo dfferential ADC. For this, they are driven by a differential input signal with a midscale common mode voltage (of 500mV). In our test circuit only one of the phases of the VCO was accessible (instead of the 18 phases as would be in an actual VCO ADC). Now, for each VCO, this output phase was captured by a 10 GS/s sampling oscilloscope and converted into a bitstream, and differentiated in the digital domain. Then the results for both VCO's were subtracted form each other. This way we obtain a configuration that is similar to an actual (pseudo-differential) first order noise shaping VCO-ADC (only with reduced performance because we are only using 1 out of the 18 phases) [3]. The corresponding output spectrum for the case of a 100kHz, 400mV$_{pp}$ differential input sine wave is shown in Fig. 6. Note that this is -14dB below the absolute maximum signal level which whould be $2V_{pp}$. The third harmonic is clearly visible at -74dBc. The second harmonic distortion is also visible at -85dBc but is so small that it almost does not affect the overall THD. This is due to the pseudo differential configuration. In the case where only 1 of the two VCO's was used (corresponding to a single-ended configuration), the second harmonic was -51dBc, indicating that over 30dB rejection of even order harmonics is easily achieved (even in this non-optimal configuration, where both VCO's are on a different die).

The high frequency noise roll off of 6dB/octave corresponds to the expected first order noise shaping. In this configuration, this noise contribution dominates above a few MHz, but as explained above this is due to the fact that only 1 of the 18 VCO phases is used here. Then there is a white noise floor (related to the thermal noise of the resistors). At low frequencies there is also some 1/f noise. For this case, the SNR and SNDR over a bandwidth of 2MHz were equal to 71dB and 69dB respectively.

Similar experiments were performed for varying input levels. The corresponding results for the SNR and SNDR in a 2MHz bandwidth are shown in Fig. 7. It is clear that for large input signal levels the performance is limited by distortion, leading to a peak SNDR of 69dB at 400mVpp (the case shown in Fig. 6). The result for the case where

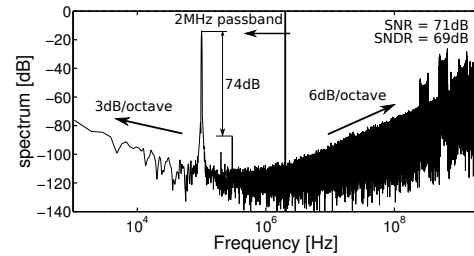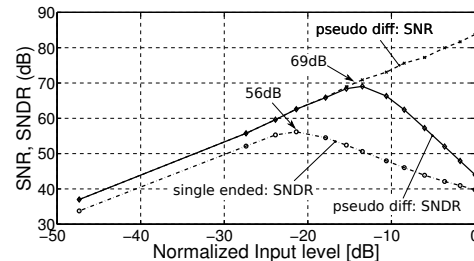only 1 VCO is read out (in a single ended configuration), is shown as well. Here, at high signal levels the distortion is dominated by the second harmonic, leading to a peak SNDR of 56dB (much worse than the pseudo differential case).

The power consumption of a single VCO was $0.65mW$. This power consumption is almost entirely determined by the choice of the resistors R_1 and R_2 (which were 770 Ω in this case). As explained above, the power can easily be reduced by using larger resistors, but this is at the expense of a higher white noise level. The area for a single VCO is $60\mu m \times 25\mu m$.

Conclusion: We have proposed the new resistive input stage for ring oscillator VCO's shown in Fig. 3. With this input stage, greatly improved VCO linearity can be achieved. In a pseudo differential configuration, for a rail-to-rail input swing of 2Vpp almost 8-bit linearity was obtained. For a more common input swing of 400mVpp even 12-bit linearity was demonstrated.

A. Babaie Fishani and P. Rombouts (*CAS, ELIS, UGent*)

E-mail: amir.babaiefishani@elis.ugent.be

References

1 Straayer, M., and Perrott, M.: 'A 12-Bit, 10-MHz Bandwidth, Continuous-Time ADC With a 5-Bit, 950-MS/s VCO-Based Quantizer,' *J. Solid-State Circuits*, 2008, vol. 43, no. 4, p. 805–814.
2 Lee, K., Yoon, Y., and Sun, N.: 'A 1.8mW 2MHz-BW 66.5dB-SNDR $\Delta\Sigma$ ADC using VCO-based integrators with intrinsic CLA', *Custom Integrated Circuits Conference (CICC)*, 2013, p. 1-4.
3 Kim, J., Jang, T.-K., Yoon, Y.-G., and Cho, S.: 'Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter', *Circuits and Systems I, Transactions on*, 2010, vol. 57, no. 1, p. 18-30
4 McNeill, J. A., Majidi, R., and Gong, J.: '"Split ADC" Background Linearization of VCO-Based ADCs', *Circuits and Systems I, Transactions on*, 2015, vol. 62, no. 1, p. 49-58
5 Voelker, M., Pashmineh, S., Hauer, J., and Ortmanns, M.: 'Current feedback linearization applied to oscillator based ADCs', *Circuits and Systems I, Transactions on*, 2014, vol. 61, no. 11, p. 3066-3074
6 Xing, X., and Gielen, G.: 'A 42 fJ/Step-FoM Two-Step VCO-Based Delta-Sigma ADC in 40 nm CMOS,' *J. Solid-State Circuits*, 2015, vol. 50, no. 3, p. 714–723.
7 Drost, B., Talegaonkar, M., and Hanumolu, P.K.: 'Analog Filter Design Using Ring Oscillator Integrators', *J. Solid-State Circuits*, 2012, vol. 47, no. 12, p. 3120-3129