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Flip-chip integration of tilted VCSELs onto a silicon photonic integrated circuit

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Abstract: In this article we describe a cost-effective approach for hybrid laser integration, in which vertical cavity surface emitting lasers (VCSELs) are passively-aligned and flip-chip bonded to a Si photonic integrated circuit (PIC), with a tilt-angle optimized for optical-insertion into standard grating-couplers. A tilt-angle of 10° is achieved by controlling the reflow of the solder ball deposition used for the electrical-contacting and mechanical-bonding of the VCSEL to the PIC. After flip-chip integration, the VCSEL-to-PIC insertion loss is −11.8 dB, indicating an excess coupling penalty of −5.9 dB, compared to Fibre-to-PIC coupling. Finite difference time domain simulations indicate that the penalty arises from the relatively poor match between the VCSEL mode and the grating-coupler.

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1. Introduction

The last decade has seen the emergence of silicon photonics as a potential platform for low-cost sensing and point-of-care medical applications, based on re-deploying established complementary metal oxide semiconductor (CMOS) technologies, at volume, for photonic applications [1,2]. The high index-contrast in the silicon-on-insulator (SOI) architecture allows for photonic integrated circuits (PICs) with very small footprints, while CMOS lithography, implantation and deposition processes allow for the implementation of a rich catalogue of passive and active components available through multi-project wafer foundry services [3]. The most significant roadblock to realizing fully functional Si-PICs is the lack of an intrinsic light source in silicon. Despite some recent work towards CMOS-compatible Ge-based lasers [4], most research has focused on the integration of III-V materials and devices on silicon, to unlock its full photonic potential. One approach is heterogeneous integration, where III-V material is bonded or transfer-printed to the Si-PIC, and then etched to create a cavity condition for on-PIC lasing [5]. Several architectures for heterogenous III-V laser on the Si photonics platform have been successfully demonstrated [6,7], but issues around the process compatibility with a CMOS foundries remain to be resolved, in order to optimize yields and reliability still need to be resolved.

An alternative approach is hybrid integration, where stand-alone "known good" laser devices are opto-mechanically coupled to the Si-PIC, using either an edge- or grating-coupling scheme. Although it is the simplest approach, hybrid integration by butt-coupling a laser into the edge-coupler of a Si-PIC often has sub-µm alignment tolerances, and requires an optical interposer [8], making volume-packaging a challenge. Hybrid laser integration using a grating-coupler to launch light into the Si-PIC brings more relaxed alignment tolerances

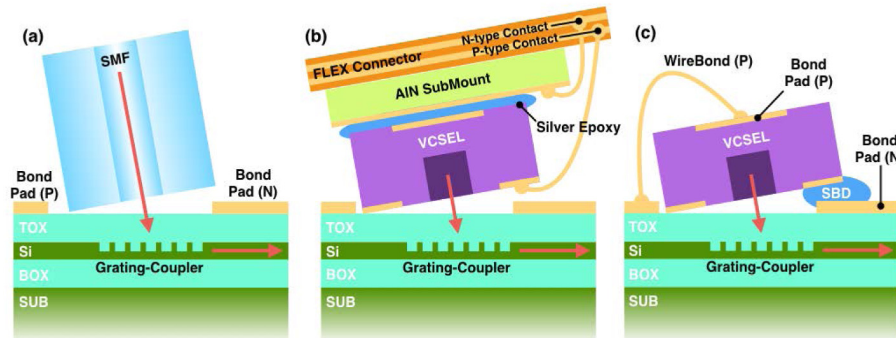

Fig. 1. (a) Schematic of a single-mode fibre (SMF) grating-coupled to the test Si-PIC, showing the near-normal angle-of-incidence of approximately 10°, The top-oxide (TOX) layer, the SOI layer, the bottom-oxide layer (BOX) and the substrate (SUB) of the sample. (b) Schematic of the sample used for active-alignment measurements, where the VCSEl is bounted on an AlN sub-mount, bonded to an electrical FLEX connector that provides power to the VCSEL and offers a means of translating and tilting the sample above the grating-coupler. **(c)** Schematic of the tilted-VCSEL flip-chip bonded above a grating-coupler on a Si-PIC, showing the solder ball deposition (SBD) and wire-bond used to make the n- and p-type electrical-connections to the on-PIC contact-pads and tracks.

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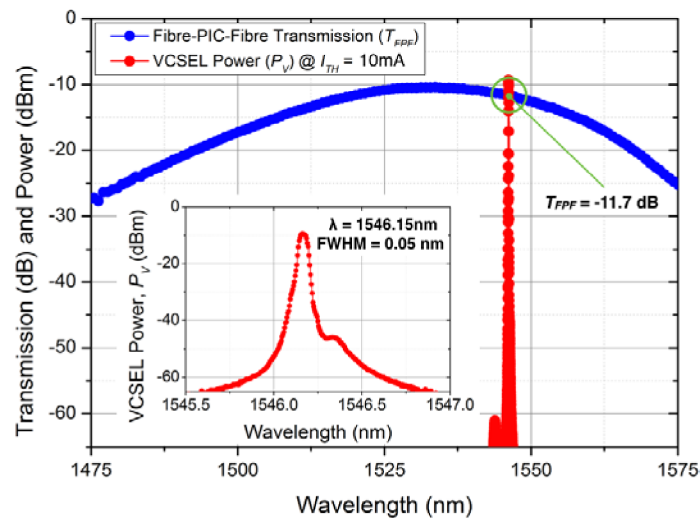

Fig. 2. The Fibre-PIC-Fibre transmission (T_{FPF}) spectrum at AOI = 10°, and VCSEL power (P_V) spectrum, with a drive-current of I_D = 10 mA and a tilt-angle of 10°. The threshold wavelength, FWHM line-width, and suppression of the VCSEL are 1546.15 nm, <0.05 nm, and and 37 dB, respectively. The value of T_{FPF} at the emission wavelength is −11.7 dB.

(typically ± 2.5 µm for 1 dB), and can be implemented using a micro-optical bench (MOB) scheme [9,10]. Although a MOB for hybrid integration brings great flexibility in terms of laser-type and additional functionality (i.e. optical-isolators), it occupies a relatively large footprint (typically 2 mm^2) on the Si-PIC. Direct hybrid integration of vertical cavity surface emitting lasers (VCSELs) to the grating-coupler on the Si-PIC allows for an order-of-magnitude reduction in footprint (250 µm x 250 µm). Planar VCSEL-to-PIC integration (where the surfaces of the VCSEL and PIC are co-planar) has already been demonstrated, but requires either post-processing to deposit photoresist based "wedges" that refract the VCSEL mode onto the grating-coupler at the correct angle-of-incidence [11], or a special bi-directional coupler that launches light into a pair of wave-guides, and which cannot be trivially re-combined into a single-channel, without phase-compensation [12,13].

In our new approach, a tilted-VCSEL is bonded directly to the PIC, without any post-processing layers, such that the VCSEL mode is correctly aligned for optical insertion into a standard grating-coupler [14] - see Fig. 1. The desired tilt-angle (10°) is achieved by controlling the reflow of the solder ball deposition (SBD) for the electrical-contacting and mechanical-bonding of the VCSEL to the PIC. Essentially, this approach allows the VCSEL bond-pads, which are originally designed for wire-bond connections, to be repurposed into a means of creating a direct VCSEL-PIC electrical connection. This approach is compatible with existing flip-chip alignment and bonding technologies, and the absence of surface treatment or post-processing ensures maximum compatibility with bio-sensing applications, because it leaves functional-layers uncontaminated, and allows them to be brought into close proximity with on-PIC waveguide and resonator structures [15]. The passive-alignment of the VCSEL on the PIC is made using alignment markers, allowing for very high-speed assembly and packaging, leading to a cost-effective method of hybrid-integration of lasers on Si-PICs.

2. Active alignment benchmark

To benchmark the results of the passively-aligned and flip-chip bonded samples, the limits of the VCSEL-PIC insertion-loss (L_{VP}) were first measured using an active-alignment set-up, and compared to the Fibre-PIC insertion loss (L_{FP}). The value of L_{FP} may be calculated directly from the Fibre-PIC-Fibre transmission (T_{FPF}) values in Fig. 2, measured using the scheme illustrated in Fig. 3(a), and by assuming that the Fibre-PIC and PIC-Fibre insertion losses are

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the same: $T_{FPF} = L_{FP} + L_{PF} = 2\ L_{FP}$. At the VCSEL emission wavelength of 1546.15nm, $T_{FPF} = -11.7$dB, see Fig. 2. The values of L_{VP} were measured using a 1550 nm long-wavelength VCSEL (225 µm x 225 µm) from VERTILAS GmbH [16] was mounted onto the Au contact-pad of a 250 µm-thick AlN sub-mount using silver epoxy. The submount was then bonded onto a two-line polyimide flexible electrical (FLEX) connector, using non-conducting thermal epoxy. A pair of wirebonds, one from the N-type bondpad on the VCSEL, and the other from the Au contact-pad of the sub-mount, were used to make the electrical connection to the FLEX – see Fig. 1(b). While the Si- PIC was securely held in place by a vacuum-chuck, the translation and tilt of the VCSEL was controlled by Newport AutoAlign system, with electrically insulating grippers holding the FLEX connector immediately beside the AlN sub-mount. The AutoAlign system allows 6-axis optimization of the position and tilt of the VCSEL during active-alignment.

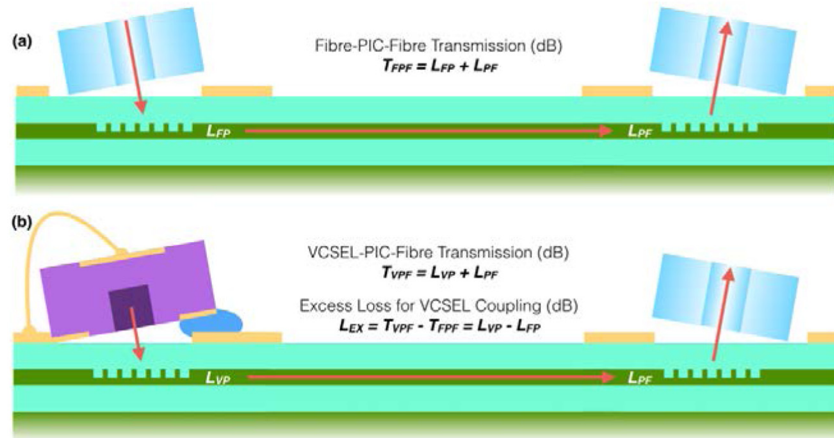

Fig. 3. Schematics of the (a) Fibre-PIC-Fibre transmission measurement, and (b) VCSEL-PIC-Fibre transmission measurement, used to determine the Fibre-PIC insertion loss (L_{FP}), the VCSEL-PIC insertion loss (L_{VP}), and so the excess coupling penalty for VCSEL coupling (L_{EX}).

The VCSEL power (P_V) and spectrum were measured as a function of drive-current (I_D), by collecting the emission into a multi-mode fibre (MMF) - see Fig. 2. To avoid thermal drift and damage during the alignment, the VCSEL was driven by a low duty-cycle (<1% at 10 kHz) pulsed power-supply. All values and figures in this article are scaled to the equivalent DC power. The VCSEL emission was centered at 1546.15 nm, with over 35 dB of polarization/side-band suppression. After optimizing the alignment and tilt of the VCSEL above the input grating-coupler, and aligning a standard SMF-28 telecom-fibre above the output grating-coupler, the VCSEL-PIC-Fibre (P_{VPF}) power and VCSEL-PIC-Fibre transmission (T_{VPF}) were measured as a function of I_D, using the geometry illustrated in Fig. 3. The VCSEL-PIC-Fibre transmission (T_{VPF}) is calculated in units of dB and dBm by $T_{VPF}(I_D) = P_{VPF}(I_D) - P_V(I_D)$, and is illustrated in Fig. 4. As expected for a normalized transmission value, $T_{VPF}(I_D)$ is almost completely independent of the drive-current, and has an average value of -16.2 dB. The excess insertion-loss of the VCSEL with respect to the Fibre (L_{EX}) is given by $L_{EX} = T_{VPF} - T_{FPF} = -16.2$ dB $+ 11.7$ dB $= -4.5$ dB. The total VCSEL-PIC insertion loss is the sum of this excess and the intial Fibre-PIC insertion loss: $L_{VP} = L_{EX} + L_{FP} = -4.5$ dB $- 5.9$ dB $= -10.4$ dB.

The -4.5 dB excess insertion-loss of the VCSEL is considerable. 3D finite difference time domain (3D-FDTD) simulations indicate that it is mainly due to footprint and numerical aperture mis-match between the VCSEL-mode and the grating-coupler. As shown schematically in Fig. 4, the MFD of the fibre-mode incident on the grating-coupler is approximately 11 µm, while that of the the VCSEL-mode is 15µm. The larger spot-size of the

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VCSEL on the PIC is due to the greater divergence of the VCSEL-mode and subsequent refraction at the VCSEL-Air interface, compounded by a larger offset above the PIC surface, owing to the greater size of the VCSEL (225 µm x 225 µm) compared to the fibre (125 µm diameter). As shown in Fig. 5, the FDTD simulations predict a higher insertion-loss for the larger, more divergent VCSEL-mode on a standard 1D focusing grating-coupler (220nm SOI, 70nm Etch-depth, 630nm Pitch, 0.50 Duty-Cycle, and an approximately 11 µm x 11µm footprint). The calculated excess insertion-loss is $L_{EX} = -3.7$ dB, which is a good match to the experimentally measured value of –4.5 dB. After re-optimizing the grating-coupler design to a15 µm x 15 µm footprint (and increasing the Pitch to 640nm, while reducing the Duty-Cycle to and 0.45), the excess insertion-loss can be reduced to −1.5 dB. Completely eliminating the excess-loss is not possible for uniform grating-couplers, because the larger divergence of the VCSEL-mode acts to widen the coupling-spectrum, reducing the peak coupling-efficiency. Non-periodic apodized grating-coupler designs based on genetic optimization may offer even lower VCSEL-PIC insertion losses.

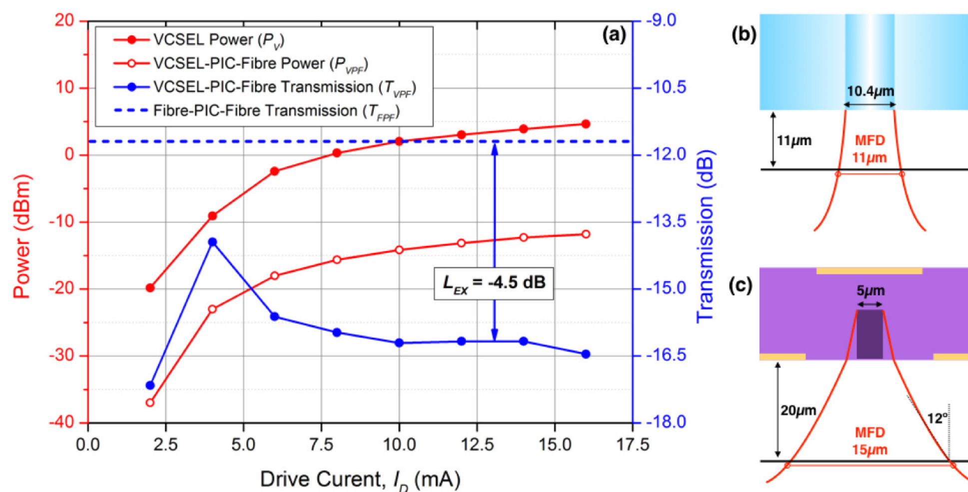

Fig. 4. (a) The VCSEL power (P_V), VCSEL-PIC-Fibre (P_{VPF}), VCSEL-PIC-Fibre transmission (T_{VPF}), and Fibre-PIC-Fibre transmission (T_{FPF}) as a function of drive-current (I_D). As expected, for drive-currents higher than approximately twice the threshold, the VCSEL-PIC-Fibre transmission is independent of I_D. Given that the average value of T_{VPF} is −16.2 dB and that $T_{FPF} = -11.7$ dB at the emission wavelength, the VCSEL-PIC insertion-loss (L_{VP}) is −10.4 dB. This corresponds to an excess coupling-penalty of (L_{EX}) of –4.5 dB, compared to the Fibre-PIC insertion-loss of the same grating-coupler. (b) and (c) Schematic of the mode-field diameter (MFD) of the fibre- and VCSEL-mode reaching the grating-coupler on the PIC surface

The alignment tolerance of the VCSEL with respect to PIC was determined by scanning the VCSEL along and across the symmetrical axis of the grating-coupler - see Fig. 6. In both directions, the 1dB alignment tolerance of the VCSEL is ± 1.6 µm, which is comparable to the Fibre-PIC alignment tolerance of a grating-coupler, and within reach of passively-aligned flip-chip alignment tools.

3. Flip-chip integration

For the previous actively-aligned measurements, the emphasis was on determining the minimum VCSEL-PIC insertion-loss and alignment tolerances, without a permanent bonding. However, for the actual hybrid integration process, the alignment and bonding are critically important. The Si-PIC was prepared for electrical routing to the VCSEL by the post-process deposition of Au bond-pads and tracks. Note that for real applications, CMOS-compatible AlCu bond-pads and tracks would be used. A pair of 50 µm solder balls were jetted onto the Au bond-pads, to provide the n-type electrical connection to the VCSEL, as well as a mechanic connection between the VCSEL and PIC. To ensure that the tilted-VCSEL has the

correct tilt-angle after flip-chip bonding, the height of the SBD after solder reflow must be controlled. As shown in Fig. 7, this was achieved by controlling the area of the Au bond-pads that are "wetted" during the solder reflow. Since the volume of the SBD is fixed, an increase in the area of the bond-pad gives a decrease in the solder height. The ± 3µm tolerance of the 50 µm solder ball diameter introduces a small uncertainty in (i) the vertical offset and (ii) the angle of the VCSEL-mode incident on the grating-coupler. Using FDTD simulations, we find that the combined impact of these effects on the VCSEL-PIC insertion-loss is on the order of0.5 dB. A second source of fabrication tolerance is the ± 10 µm tolerance on the nominal size of VCSEL die. This also translates to an analogous uncertainty in vertical offset and angle-of-incidence for the VCSEL-mode on the PIC. Again, FDTD simulations indicate that dicing tolerances impact the VCSEL-PIC insertion-loss on the order of 0.5 dB, giving a total fabrication-related tolerance (in addition to the alignment tolerance) of approximately 1 dB.

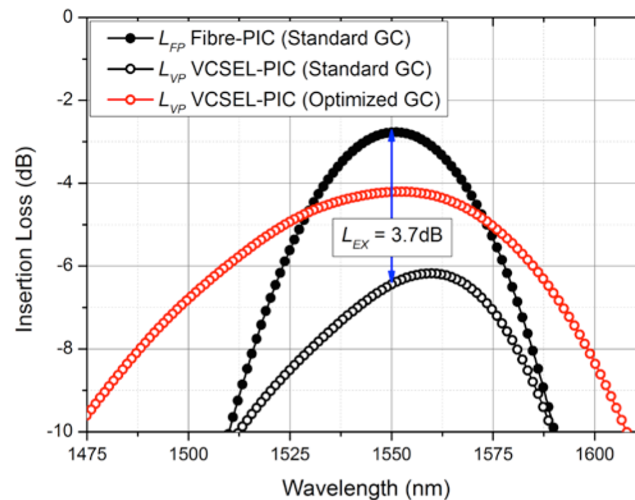

Fig. 5. 3D-FDTD simulations of the Fibre-PIC and VCSEL-PIC insertion losses to the standard grating-coupler used in the experimental measurements, and the reduced VCSEL-PIC insertion-loss for coupling to an optimized large-footprint grating-coupler.

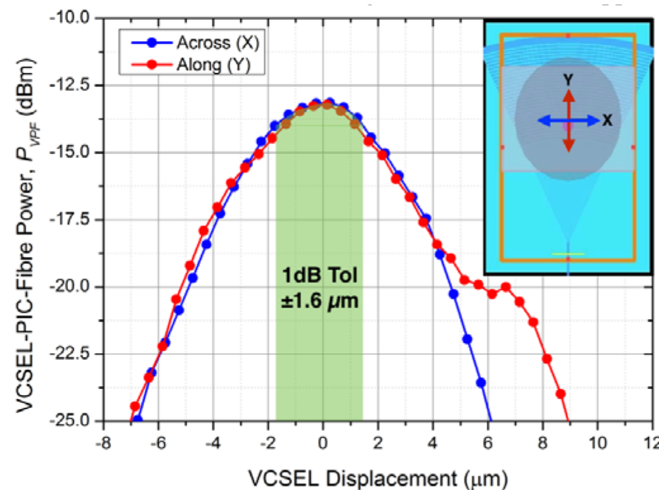

Fig. 6. Alignment tolerance of the VCSEL across (X) and along (Y) the symmetrical axis of the grating-coupler, made using active-alignment VCSEL-PIC-Fibre (P_{VPF}) measurements at I_D = 10 mA. The 1dB alignment tolerance is ± 1.6 µm in both directions. The inset shows a plan-view of the corresponding grating-coupler structure studied in the 3D-FDTD simulations.

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After process optimization, the flip-chip bonding, carried-out at a peak temperature of 270 °C for 30 s on a *FineTech* system, could achieve a tilt-angle of 10° with a high degree of reproducibility. For the bonding, the VCSEL and Si-PIC were not actively-aligned, but brought into coincidence using beam-splitter imaging on the flip-chip system - see Fig. 8. Coarse alignment is made using paried alignment marks on the VCSEL and PIC, and fine alignment is made by centering the VCSEL aperture on the grating-coupler, and making a small compensation to allow for beam-travel due to the 10° tilt-angle.

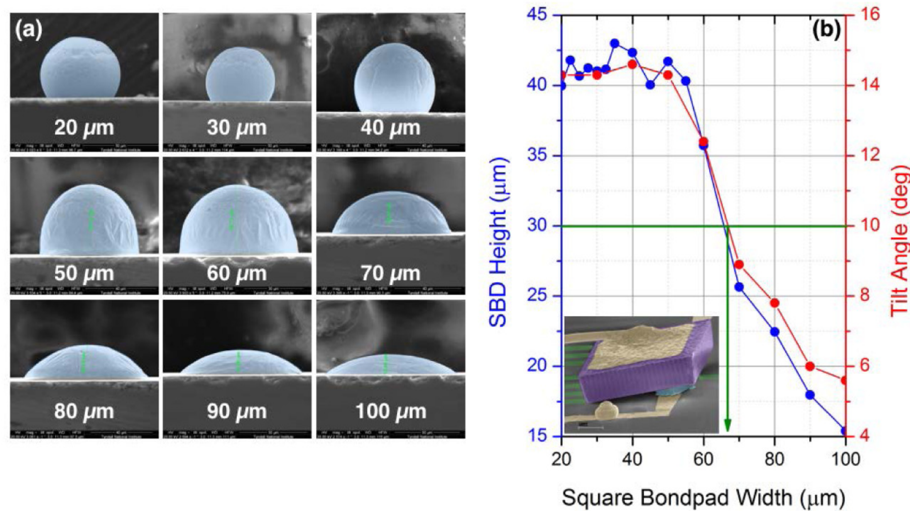

Fig. 7. (a) A series of SEM images showing solder ball deposition (SBD) deposited on test-structures, to calibrate the height of the SBD-reflow as a function of the contact-pad area. **(b)** Plot showing the SBD-reflow height as a function of square contact-pad width, and the corresponding tilt-angle of the VCSEL on the PIC.

After the flip-chip bonding, a wire-bond is added between a track on the PIC and the rear of the VCSEL, to make the p-type connection. The p-contact pads on the top side of the VCSELs and the integrated gold heatsink which covers the entire back side of the VCSEL are connected by via-holes through the Benzocyclobutene material that covers most of the n-side of the structure. In principle, an index-matching epoxy under-fill could be added between the VCSEL and PIC, to improve mechanical adhesion and increase thermal conduction from the laser, but that was not carried-out for this work.

Using the same procedure as for the active-alignment measurements, the typical VCSEL-PIC insertion loss for the passively-aligned and flip-chip bonded VCSEL was determined as $L_{VP} = -11.8$ dB, corresponding to an excess coupling-penalty of $L_{EX} = -5.9$ dB. Note that this penalty is just 1.3 dB higher than that achieved with the active-alignment, demonstrating that the coupling performance is not significantly limited by the alignment tolerances of the assembly process. Based on the tolerances measured in Fig. 6, the flip-chip bonding system has an alignment tolerance of approximately ± 2 μm. The normalized VCSEL-PIC power (L_{VP}) spectrum and LI-curve are shown in Fig. 9, and give an indication of the laser power and performance that can currently be achieved using this new cost-effective hybrid integration approach. At roll-over, the maximum optical power injected into the PIC was −8.6 dBm = 138 μW. As mentioned previously, with grating-couplers optimized for the VCSEL-mode, future insertion-losses can be further reduced.

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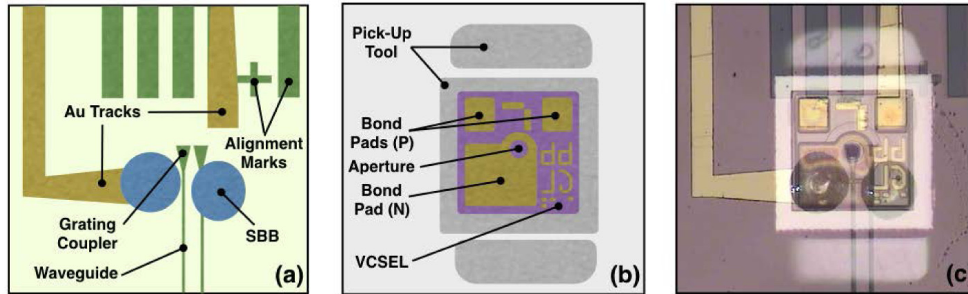

Fig. 8. (a) Schematic of the relevant area of the Si-PIC, showing the grating-coupler, and waveguide, the solder ball deposition (SBD), and the Au-tracks and bond-pads for contacting the VCSEL. (b) Schematic of the VCSEL, mounted on the flip-chip pick-up tool, showing the bond-pads for electrical-connection and the aperture for laser emission. **(c)** Combined image of the Si-PIC and VCSEL from the flip-chip bonder, which uses a beam-splitting mirror to simultaneously image both components, to allow for precision alignment.

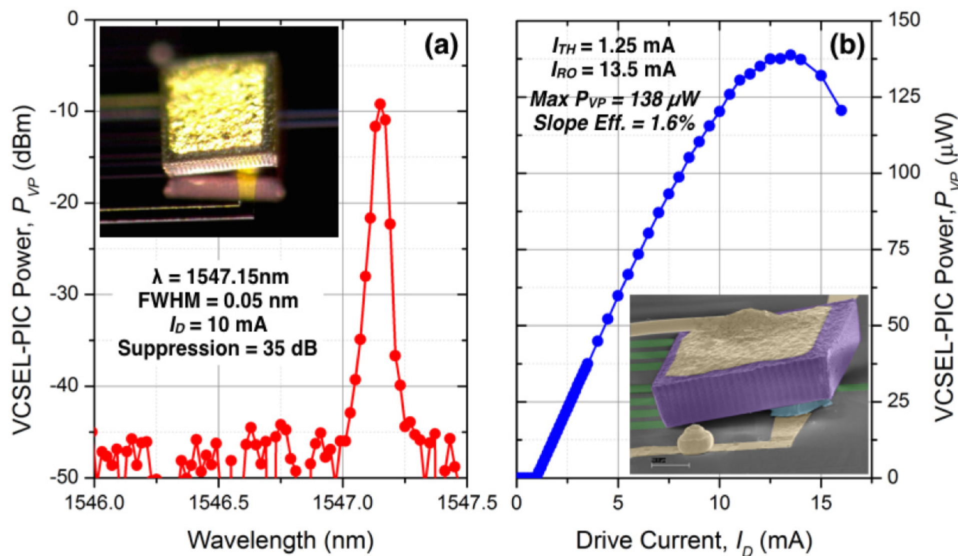

Fig. 9. (a) Power spectrum (P_{VP}) and (b) LI-curve of a flip-chip bonded and packaged tilted-VCSEL on the Si-PIC. The emission is centered at 1547.15 nm, and has a polarization/side-band suppression of 35 dB. At roll-over, the maximum optical-power injected into the PIC is 138 μW = −8.6 dBm. The slope-efficiency of the injected power is 1.6%.The inset of (a) shows a microscope image of the VCSEL bonded onto the PIC, before the top-side wire-bond was added, and the inset of (b) shows an SEM image of a 10° tilted-VCSEL on a PIC, with false colors to more easily identify the VCSEL (purple), electrical contacts (gold), SBD (blue), and waveguide structures (green).

4. Conclusions

We have shown that it is possible to flip-chip bond a tilted-VCSEL above the grating-coupler, for cost-effective hybrid integration of a laser-source on a Si-PIC. We have demonstrated a VCSEL-PIC insertion loss of −11.8 dB after passive-alignment and flip-chip bonding, which is only 1.3 dB higher than that possible using active-alignment. The relatively high VCSEL-PIC insertion loss, compared to the Fibre-PIC loss of −5.9 dB, is mainly due to a mismatch between the modes of VCSEL and the grating-coupler, and can be addressed in future with optimized grating-coupler designs.

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