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Continuous time delta sigma modulation with PWM pre-coding and binary g_m blocks

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We present a very simple technique to implement the first integrator of a continuous-time delta sigma modulator (CT-DSM). In the approach, the CT-DSM is preceded by a pulse-width modulator to convert the input signal to a pseudo-digital continuous time waveform. As a result, the first integrator of the DSM can be implemented with a capacitor and a switched current source, with inherent linearity. To illustrate the concept, it has been applied to the design of a 2nd order CT-DSM in 65nm CMOS technology.

Introduction: Recently, various A/D conversion techniques that employ some kind of Pulse Width Modulation (PWM) have been presented [1, 2, 3]. Such a PWM converts a baseband signal into a two-level continuous time waveform. Here, the information is stored in the transitions of this 2-level waveform. If properly designed, no information is lost in this process. The two-level signal that comes out of the PWM can be easily processed by other circuit blocks. This way, a PWM is sometimes used in front of other blocks in the system's signal path. This technique is referred to as PWM pre-coding. In prior work, PWM pre-coding has been used to linearize a VCO-based ADC [1]. Alternatively, in [2] a time-to-digital converter was combined with a PWM pre-coding to convert the PWM signal into the digital domain. The former approach [1] achieves a 1st order quantization noise shaping, while the latter [2] exhibits no noise shaping at all.

In this letter we present a new method for utilizing PWM pre-coding in the design of an ADC. In this work, the PWM is followed by a Continuous-Time Delta-Sigma modulator (CT-DSM) which, in contrast with previous works, can have quantization noise-shaping of any arbitrary order.

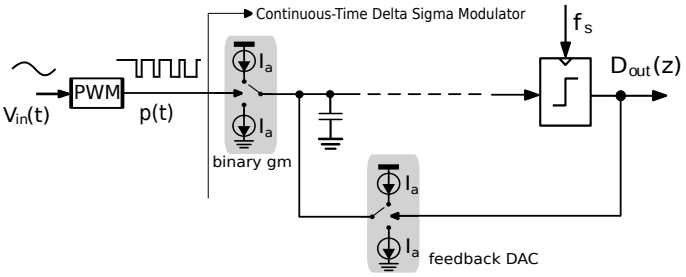

Fig. 1. The proposed architecture for linearizing CT ΣΔ Modulators.

Proposed Architecture: Fig.1 shows the proposed ADC concept. Here, the input signal of the ADC is first applied to a PWM, then the output signal $p(t)$ of the PWM is used to drive a switched current source. This switched current source can be viewed as a two-level transconductor or a "binary g_m". This binary g_m is combined with a capacitor and these two simple elements together build an integrator which is used as the first integrator of a CT-DSM. The binary g_m is very similar to the switched current source which is used as the feedback DAC. The combination of the switched current source and the capacitor of the first integrator also looks like the charge-pump structure which is commonly used as the loop-filter in a PLL.

The main advantage of this approach over a conventional DSM is the simplicity in design and implementation of the first integrator in this approach. The first integrator of a DSM has to satisfy several criteria mostly with regard to linearity and noise, because all the non-idealities of this block directly corrupt the desired signal. For this reason, the first integrator of a DSM is usually responsible for most of the power consumption of the whole modulator and is the most challenging part of a DSM to be designed. In the proposed concept, on the other hand, the first integrator is implemented by a binary g_m and a capacitor, that can be designed very easily.

The Pulse-Width Modulator is also an easy-to-design block [1]. In its simplest version, it consists of a schmitt-trigger and a passive loop filter. However, a potential problem with a PWM signal is that it contains many harmonics of fc, the carrier frequency of the PWM. If these harmonics fall near integer multiples of fs, where fs is the clock frequency of the DSM, after sampling in the DSM loop, they might alias to the baseband and corrupt the desired signal [1]. Fortunately, this problem is alleviated in this architecture, because anti-aliasing filtering is one of the inherent qualities of a Continuous Time DSM and as the order of the modulator increases, the anti-aliasing filtering will improve. As a result, the carrier frequency of the PWM can be chosen relatively freely in the sense that fs can be an integer multiple of fc while the aliasing effects are still modest.

Obviously, the concept presented in Fig.1 can easily be extended to multi-bit conversion by using a multi-bit quantizer and multiple switched current sources in the DAC. It is also clear that the proposed method can be applied to a CT-DSM of arbitrary order.

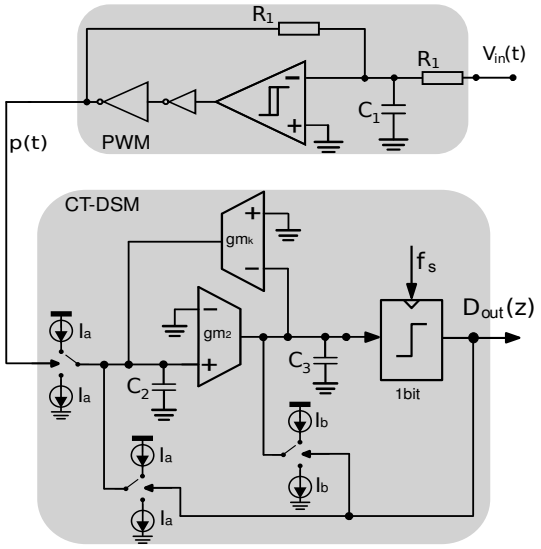

Fig. 2 *Top-level schematic of the Design Example ADC, consisting of a Pulse-Width Modulator and a gm-C CT-DSM.*

Design Example: To illustrate the effectiveness of the proposed concept, we have applied it in the design of a second-order CT-DSM for a bandwidth of 16 MHz with an OSR of 64 (corresponding to a clock frequency around 2 GHz) in a standard 65nm CMOS process. Fig.2 shows the corresponding circuit diagram. The upper part of the figure is the pulse-width modulator. Conceptually, it consists of a feedback loop with a 1st-order passive loop filter and a schmitt-trigger. In the actual implementation, a tapered inverter buffer is added to make the rising and falling edges of the PWM signal steeper. As mentioned in the previous section, the carrier frequency of the PWM, fc, doesn't need to be accurately controlled. Nevertheless, there are some considerations on the choice of fc. If fc is too close to the baseband, modulation sidebands may fall partially into the baseband. A high value of fc, on the other hand, increases the power consumption. Considering the targeted bandwidth, a carrier frequency of 500MHz is chosen for the PWM.

The lower rectangle in Fig.2 shows the CT-DSM that follows the PWM. The first integrator is implemented by a binary g_m and is driven by the pseudo-digital waveform $p(t)$, as explained above. The requirements on the design of the second integrator, with transconductor g_{m2}, are heavily relaxed because the non-ideal effects of this block are reduced by the high gain of the first integrator and are therefore negligible. For this block a simple source-degenerated differential-pair transconductor was chosen. The local feedback, implemented with the transconductor g_{mk}, has a very small transconductance and has little impact on the overall linearity, noise or power of the modulator. The overall power consumption of the designed circuit is as low as 2.5 mW from a single 1.2V supply.

The resulting output spectrum of a transistor level simulation of this circuit is shown in Fig.3. The corresponding SNR and SNDR are both equal to 66dB for a 16MHz bandwidth. As expected, the PWM carrier and its sidebands are visible around 500MHz. These tones are safely away from the baseband and they can easily be filtered in the digital domain. The theoretical noise spectrum (calculated from the designed NTF) is also shown in the figure. It matches the simulation very well, apart from the fact that the notch in the noise spectrum is 'filled' in the simulated spectrum. This is due to the finite output impedance of the current sources in the first integrator, which can not easily be made arbitrarily large in this 65 nm CMOS technology (because of leakage effects). Due to this, the DC-gain

of the first integrator is not infinite. If this effect is taken into account in the theoretical plot, it matches the experiment nearly perfectly.

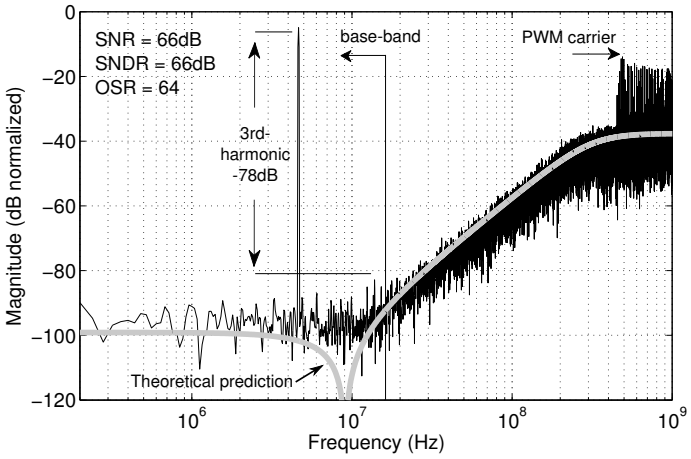

Fig. 3 *Transistor-level simulation result of the Output spectrum of the design example.*

Conclusion: This letter presents a simple technique to implement the first integrator of a continuous-time delta sigma modulator with low complexity and power consumption. The approach uses a PWM to convert the input signal into a two-level signal so that a switched current source together with a capacitor can be used as the first integrator in a CT-DSM. The idea can be applied to a CT-DSM arbitrary order that can have a single-bit as well as multi-bit quantizer.

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