Ultra-thin DVS-BCB adhesive bonding of III-V wafers, dies and multiple dies to a patterned silicon-on-insulator substrate

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Abstract: Heterogeneous integration of III-V semiconductor materials on a silicon-on-insulator (SOI) platform has recently emerged as one of the most promising methods for the fabrication of active photonic devices in silicon photonics. For this integration, it is essential to have a reliable and robust bonding procedure, which also provides a uniform and ultra-thin bonding layer for an effective optical coupling between III-V active layers and SOI waveguides. A new process for bonding of III-V dies to processed silicon-on-insulator waveguide circuits using divinylsiloxane-bis-benzocyclobutene (DVS-BCB) was developed using a commercial wafer bonder. This "cold bonding" methods ignificantly simplifies the bonding preparation for machine-based bonding both for die and wafer-scale bonding. High-quality bonding, with ultra-thin bonding layers (<50 nm) is demonstrated, which is suitable for the fabrication of heterogeneously integrated photonic devices, specifically hybrid III-V/Si lasers.

References and links

1. W. Bogaerts, R. Baets, P. Dumon, V. Wiaux, S. Beckx, D. Taillaert, B. Luyssaert, J. Van Campenhout, P. Bienstman, and D. Van Thourhout, "Nanophotonic waveguides in silicon-on-insulator fabricated with CMOS technology," J. Lightwave Technol. **23**(1), 401–412 (2005).
2. O. Boyraz and B. Jalali, "Demonstration of a silicon Raman laser," Opt. Express **12**(21), 5269–5273 (2004).
3. G. Roelkens, L. Liu, D. Liang, R. Jones, A. Fang, B. Koch, and J. Bowers, "III-V/silicon photonics for on-chip and intera-chip optical interconnects," Laser Photonics Rev. **4**(6), 751–779 (2010).
4. D. Liang and J. E. Bowers, "Recent progress in lasers on silicon," Nat. Photonics **4**(8), 511–517 (2010).
5. T. Mitze, M. Schnarrenberger, L. Zimmermann, J. Bruns, F. Fidorra, J. Kreissl, K. Janiak, S. Fidorra, H. Heidrich, and K. Petermann, "Hybrid integration of III/V lasers on a silicon-on-insulator (SOI) optical board," in *2nd IEEE International Conference on Group IV Photonics, 2005* (IEEE, 2005), pp. 210–212.
6. D. Fehly, A. Schlachetzki, A. S. Bakin, A. Guttzeit, and H.-H. Wehmann, "Monolithic InGaAsP optoelectronic devices with silicon electronics," IEEE J. Sel. Top. Quantum Electron. **37**(10), 1246–1252 (2001).
7. M. Lamponi, S. Keyvaninia, C. Jany, F. Poingt, F. Lelarge, G. de Valicourt, G. Roelkens, D. Van Thourhout, S. Messaoudene, J.-M. Fedeli, and G. H. Duan, "Low-threshold heterogeneously integrated InP/SOI lasers with a double adiabatic taper coupler," IEEE Photon. Technol. Lett. **24**(1), 76–78 (2012).
8. S. Stanković, R. Jones, J. Heck, M. Sysak, D. Van Thourhout, and G. Roelkens, "Die-to-die adhesive bonding for evanescently-coupled photonic devices," Electrochem. Solid-State Lett. **14**(8), H326–H329 (2011).
9. S. Palit, J. Kirch, G. Tsvid, L. Mawst, T. Kuech, and N. M. Jokerst, "Low-threshold thin-film III-V lasers bonded to silicon with front and back side defined features," Opt. Lett. **34**(18), 2802–2804 (2009).
10. S. Famenini and C. G. Fonstad, "Integration of edge-emitting laser diodes with dielectric waveguides on silicon," IEEE Photon. Technol. Lett. **24**(20), 1849–1851 (2012).
11. F. J. Blanco, M. Agirregabiria, J. Garcia, J. Berganzo, M. Tijero, M. T. Arroyo, J. M. Ruano, I. Aramburu, and K. Mayora, "Novel three-dimensional embedded SU-8 microchannels fabricated using a low temperature full wafer adhesive bonding," J. Micromech. Microeng. **14**(7), 1047–1056 (2004).

12. H. C. Lin, K. L. Chang, G. W. Pickrell, K. C. Hsieh, and K. Y. Cheng, "Low temperature wafer bonding by spin on glass," J. Vac. Sci. Technol. B **20**(2), 752–754 (2002).
13. F. Niklaus, P. Enoksson, E. Kalvesten, and G. Stemme, "Low-temperature full wafer adhesive bonding," J. Micromech. Microeng. **11**(2), 100–107 (2001).
14. D.-H. Choi, C.-H. Yeo, J.-T. Kim, C.-W. Ok, J.-S. Kim, Y. Kwon, and Y.-H. Im, "Study on bisbenzocyclobutene bonding for the development of a si-based miniaturized reformer of fuel cell systems," J. Micromech. Microeng. **19**(7), 075013 (2009).
15. F. Niklaus, G. Stemme, J.-Q. Lu, and R. J. Gutmann, "Adhesive wafer bonding," J. Appl. Phys. **99**(3), 031101 (2006).
16. S. Keyvaninia, M. Muneeb, S. Stankovic, G. Roelkens, D. Van Thourhout, and J.-M. Fedeli, "Multiple die-to-wafer adhesive bonding for heterogeneous integration," in *16th European Conference on Integrated Optics* (2012), paper 186.
17. S. Stanković, R. Jones, M. Sysak, J. Heck, G. Roelkens, and D. Van Thourhout, "1310nm Hybrid III-V/Si Fabry-Perot Laser Based on Adhesive Bonding," IEEE Photon. Technol. Lett. **23**(23), 1781–1783 (2011).
18. S. Keyvaninia, G. Roelkens, and D. Van Thourhout, "Engineering the heterogeneously integrated III-V/SOI tunable laser," in *Proceedings of 2009Annual Symposium of the IEEE Photonics Benelux Chapte r*(ASP—Academic & Scientific, 2009), pp. 141–144.
19. S. Keyvaninia, S. Verstuyft, F. Lelarge, G. H. Duan, S. Messaoudene, J. M. Fedeli, T. De Vries, B. Smalbrugge, J. Bolk, M. Smit, D. Van Thourhout, and G. Roelkens, "Heterogeneously integrated III-V/Si multi-wavelength laser based on a ring resonator array multiplexer," in *Asia Communications and Photonics Conference*, OSA Technical Digest (Optical Society of America, 2012), paper PAF4A.3.
20. D. Van Thourhout, S. Keyvaninia, G. Roelkens, M. Lamponi, F. Lelarge, J. M. Fedeli, S. Messaoudene, and G. H. Duan, "Optimization of taper structures for III-V silicon lasers," in *2012 International Conference on Solid State Devices and Materials* (2012), pp. 524–525.
21. P. De Heyn, S. Verstuyft, S. Keyvaninia, A. Trita, and D. Van Thourhout, "Tunable 4-channel ultra-dense WDM demultiplexer with III-V photodiodes integrated on silicon-on-insulator," in *Asia Communications and Photonics Conference*, OSA Technical Digest (Optical Society of America, 2012), paper ATh2B.1.
22. "Processing procedures for CYCLOTENE 3000 series dry etch resins," http://www.dow.com/cyclotene/prod/302235.htm.
23. J. Pello, P. Saboya, S. Keyvaninia, J. J. G. M. van der Tol, G. Roelkens, H. P. M. M. Ambrosius, and M. K. Smit, "Post-bonding fabrication of photonic devices in an Indium phosphide membrane bonded on glass," in *Proceedings of the 16th Annual symposium of the IEEE Photonics Benelux Chapter* (2011), pp. 213–216.
24. J. Pello, J. van der Tol, S. Keyvaninia, R. van Veldhoven, H. Ambrosius, G. Roelkens, and M. Smit, "High-efficiency ultrasmall polarization converter in InP membrane," Opt. Lett. **37**(17), 3711–3713 (2012).

1. Introduction

SOI is an emerging platform for photonic integrated circuits; it offers the potential of realizing low-cost a nd co mpact o ptical ci rcuits. Mo reover, s tandard co mplementary metal o xide semiconductor (CMOS) processing infrastructure can be used to process these optical components [1]. This a llows h igh-yield f abrication a nd a r eduction o f t he c omponent c ost through eco nomies o f s cale. H owever, t he f abrication o f ef ficient l ight s ources i n s ilicon photonics is challenging due to silicon's indirect bandgap. Because of this indirect bandgap, the probability for a n excited electron-hole pair to recombine and emit a photon is strongly reduced as a result of the much higher non-radiative recombination rate. Advances are being made to achieve light emission from silicon, either by modifying the silicon on a nanoscale or by exploiting its nonlinear optical properties [2]. However, those devices are not good enough for use in high-performance sensing and communication systems. In order to create photonic integrated c ircuits c omprising b oth o pto-electronic a nd passive o ptical co mponents, t he heterogeneous integration o f p assive s ilicon-on-insulator waveguide c ircuits and a ctive InP/InGaAsP components has been proposed [3,4], for applications in the telecommunication wavelength range.

There are three main routes to the integration of III-V material on top of SOI, namely flip-chip integration [5], hetero-epitaxial growth [6], and bonding technology [3,4,7,8]. In the first approach, individual laser diode dies are flip-chipped on and c oupled to an SOI waveguide circuit. While flip-chip integration is the most rugged technology, individual dies need to be aligned with sub-micrometer precision and placed on the surface. Also, the integration density is li mited b y t he p itch a nd s ize o f th e solder b umps. Recently, e dge-emitting la ser d iodes coupled to waveguide circuits were demonstrated using pick and place assembly to position them on the substrate [9,10]. Hetero-epitaxial growth of InP/InGaAsP, the material system of

interest for telecommunication wavelength applications, is hampered by the large lattice mismatch of 8% between the III-V material and the silicon host substrate. Semiconductor wafer bonding on the other hand allows the integration of high-quality III-V epitaxial layers on top of the silicon platform by transferring the III-V layer stack from its original growth substrate to the SOI wafer. Full wafer bonding, multiple die-to-wafer bonding or single die bonding can be envisaged, depending on the application. In all cases, an unprocessed III-V semiconductor epitaxial layer stack is transferred, which reduces the time required to complete the integration process compared to a flip-chip process, as no stringent alignment accuracy is needed, because of the absence of structures on the III-V dies or wafers. After removal of the growth substrate, the optoelectronic components can be fabricated in the bonded epitaxial layer.

While there are various methods to transfer an InP/InGaAsP epitaxial layer structure onto an SOI waveguide wafer (molecular bonding, adhesive bonding, anodic bonding, metallic bonding), adhesive bonding offers some significant advantages over the other bonding methods. The relaxed requirements on surface cleanliness, contamination and surface roughness combined with the planarizing action of the adhesive spin coating process, offer a significant reduction in surface preparation. Moreover, the integration process is a low-temperature process, reducing the stress in the bonded stack due to the difference in thermal expansion coefficients between silicon and III-V semiconductor.

Both thermoplastic polymers, like SU-8 [11] and thermosetting polymers, such as spin-on glass [12], polyimide and DVS-BCB (divinylsiloxane-bis-benzocyclobutene), are used as adhesives [13]. DVS-BCB is a good candidate for hybrid bonding because of its excellent physical properties such as low dielectric constant, low moisture absorption, low curing temperature, high degree of planarization, low level of ionic contaminants, high optical clarity, good thermal stability, excellent chemical resistance, and good compatibility with various metallization systems [13,14]. Early work by Frank Niklaus investigated the influence of different bonding parameters on void formation in low-temperature full-wafer adhesive bonding using DVS-BCB as the intermediate bonding material, both on unpatterned and patterned substrates, using micrometer thick bonding layers [15]. Subsequently, die-to-wafer and die-to-die bonding based on both manual and machine-based DVS-BCB bonding were reported by our group [8,16]. The major challenge in the bonding process is the fact that deep submicrometer layer thicknesses are required to achieve optical coupling from the top active III-V layer into the bottom SOI waveguides. This optical coupling can be achieved in various ways, including the use of hybrid modes [8,17] and the use of a double taper structure, using taper-based mode transformers both in the III-V and silicon waveguides [7,18–20]. Both approaches can be made tolerant to bonding layer thickness variations on the order of tens of nanometer.

In this paper, we describe a new adhesive wafer bonding process scheme that involves partial curing of the DVS-BCB prior to bonding and attaching the III-V substrate at room temperature prior to curing in a vacuum atmosphere. This "cold bonding" method significantly simplifies the bonding preparation for machine-based bonding, both for die and wafer-scale bonding. This approach shows high yield for ultra-thin bonding thicknesses below 50 nm, as well as a good uniformity of the DVS-BCB layer thickness after wafer bonding over the full wafer area. This process was applied to achieve ultra-thin DVS-BCB bonding layers for the fabrication of several photonic devices, such as III-V/SOI lasers [7,18–21].

2. DVS-BCB wafer bonding processes

The bonding process was developed for a wafer level epitaxial layer transfer; however, as will be shown later, it can also be applied to a multiple die-to-wafer bonding and a single-die bonding. A Suss MicroTec ELAN CB6L wafer bonder was used for bonding experiments. Commercial DVS-BCB solutions are limited in available spin-coated layer thicknesses down to 1µm (for Cyclotene$^{®}$ 3022-35 from Dow Chemical) [22]. Since this work deals with

bonding layer thicknesses that are an order of magnitude smaller, mesitylene is added to Cyclotene 3022-35 to reduce the spin-coated layer thickness substantially.

The processing procedure is schematically illustrated in Fig. 1. The bonding process starts with the cleaning of the SOI substrate and the III-V dies. The SOI cleaning is performed by immersing the substrate for 15 minutes into a Standard Clean 1 (SC-1) solution, comprising aqueous ammonia (NH_4OH), hydrogen peroxide (H_2O_2) and deionized (DI) water in volume ratios of 1:1:5, respectively, which is heated to 70 °C. After this, the DVS-BCB:mesitylene solution is spin-coated onto the SOI substrate. The SOI substrate is then baked for 10 min at 150 °C, to let mesitylene evaporate, after which the substrate is slowly cooled down to room temperature. Finally, the SOI is mounted on a carrier wafer made of Pyrex glass (1200 um thick, 100 mm diameter). Meanwhile, prior to bonding, an InP/InGaAs sacrificial layer pair on the III-V wafer/die is removed by selective wet etching using $HCl:H_2O$ and $H_2SO_4:H_2O_2:H_2O$ solutions, in volume ratios of 4:1 and 1:1:18 respectively. This procedure removes particles and contaminants from the III-V die surface. The III-V die is then rinsed with DI water, dried and mounted on the SOI die. Since, in the presented method, the dies are contacted at room temperature, individual dies can easily be pick-and-placed onto the silicon target wafer. They can be aligned manually with an accuracy of 500µm without any extra tools or can be placed more accurately using a flip-chip machine. After that, the SOI substrate on its carrier wafer is mounted on the transport fixture and is loaded into the processing chamber of the wafer bonding tool. The chamber is pumped-down (target pressure 10^{-3} mbar) and heated to 150°C with a ramp of 15 °C/min for 10 min, while applying pressure on the III-V/SOI stack. The actual bonding pressure (the applied force per area of the III-V die) is kept in the range of 200 to 400 kPa. After keeping the pressure on the dies for 10 min at 150 °C, the temperature is increased up to 280 °C, with a ramp of 1.5 °C/min. Upon reaching 280 °C, the dies are kept at this temperature for 60 min in a nitrogen atmosphere. After the curing, the bonded samples are cooled down (at 6-10 °C/min) and unloaded from the processing chamber. The InP substrate of the III-V die is then removed by a selective wet etching using HCl, leaving a thin III-V film with the functional layers bonded to the SOI die, ready for further processing. An alternative method has been reported earlier by our group [8], in which adhesive die-to-wafer bonding was demonstrated in a commercial wafer bonder. In this method spacers are used to keep the die and substrate separate prior to loading the stack in the bonding tool. In this new method no carrier is required to load the top wafer/die into the machine and no vacuum or heating is required prior to contacting the wafers in the bonding chamber. This makes the process more
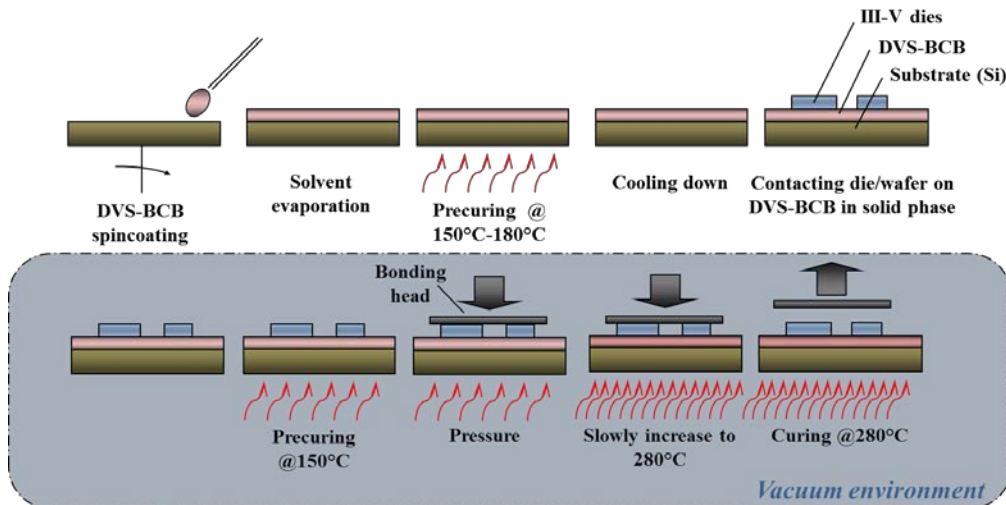

Fig. 1. Developed bonding process, referred to as "cold bonding".

straightforward. Moreover, with the previous recipe, it was not possible to perform multiple die-to-wafer bonding for dies with different thickness. Using this new method, we demonstrate that multiple-die bonding with different die thickness is feasible.

3. Bonding experiments

Several bonding experiments were performed to evaluate the bonding quality and the DVS-BCB thickness uniformity after wafer bonding. The experimental results are discussed in the following sections. Wafer-to-wafer, die-to-wafer and multiple die-to-wafer bonding are reported.

3.1. Wafer-to-wafer bonding

The bonding quality was first assessed by bonding 2 inch InP wafers to 4 inch Pyrex glass wafers (with a thermal expansion coefficient similar to that of silicon). In this way, the bonding interface can be inspected through the Pyrex substrate using a standard microscope with a polarization filter. The InP wafer was etched away after bonding using a selective wet etching solution (HCl) to measure the thickness and uniformity of the DVS-BCB bonding layer. The results of 5 wafer bonding experiments are summarized in Table 1, showing a good uniformity over the wafer (the bonding layer thickness was measured in 18 points all over the wafer area using a profilometer) and a good reproducibility of the nominal bonding layer thickness, even when there is a variation in applied pressure. A DVS-BCB:mesitylene dilution of 1:8 (v/v) was used in the experiment; spin coated at 3000 rpm, this results in a 35 nm DVS-BCB bonding layer thickness. Even with such thin bonding layers, the bonded area is above 99%. The non-bonded parts are due to the presence of particles at the bonding interface. This is related to the fact that bulk InP wafers were used without a sacrificial InP/InGaAs layer pair to remove particle contamination from the surface.

Table 1. Statistical data of measured DVS-BCB thickness for five different full wafers bonded on a Pyrex glass wafer[a]

Sample	t_min (nm)	t_max (nm)	t_avg (nm)	STD	NU (%)	Bonded area (%)	Pressure (KPa)
1	31	39	35.3	1.92	11	99.5	350
2	31	39	36.3	2.2	11	99.5	350
3	33	45	36.5	2.95	16	99	350
4	31	39	35	2.82	11.4	100	370
5	31	41	35.2	2.43	14.2	99	370

[a]STD: standard deviation, NU: non-uniformity.

Additional bonding experiments were carried out, transferring a 300 nm thick InP membrane to a Pyrex handle wafer, to a silicon wafer with a 1.5 μm-thick layer of SiO_x on top and to a silicon-on-insulator wafer with a 220 nm high silicon pattern. For this we used InP-substrates with a 300 nm InP layer grown onto a 300 nm InGaAs etch stop layer, provided by III-V lab, France. The resulting InP membrane after transfer can be used as an optical waveguide layer for ultra-compact III-V membrane photonic integrated circuits [23,24]. A nice and uniform 2 inch diameter film appeared after removing the substrate (Figs. 2(a)-2(c)). To measure the DVS-BCB thickness and uniformity, 4 cross-sections were made through the bonded stack 2 cm away from each other, using a focused ion beam (FIB) tool, and inspected using scanning electron microscopy (SEM). A uniform DVS-BCB thickness for different points distributed over the bonded surface is obtained, with an average bonding layer thickness of 29 nm, varying by ±3 nm over the cross-sections.
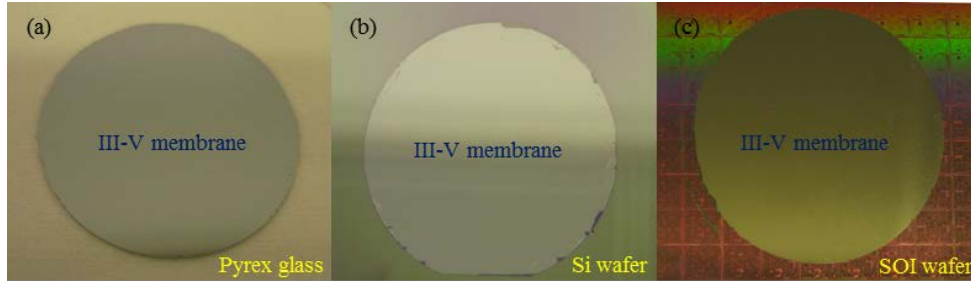
Fig. 2. A full wafer 300 nm InP membrane bonded on a Pyrex glass wafer (a), a 100 mm silicon wafer (b) and a patterned SOI wafer (c) after substrate removal.

Table 2. Statistical data of measured DVS-BCB thickness for five different quarter wafers bonded on a Pyrex glass wafer[a]

Sample	t_min (nm)	t_max (nm)	t_avg (nm)	STD	NU (%)	Bonded area (%)	Pressure (KPa)
1	41.7	49.9	47	3.8	14	99	300
2	45	50.7	48	3.9	13	99	300
3	43	54.1	47	2.6	10	100	300
4	45	51.2	46	3.1	11	99.5	300
5	45	47.7	43	2.3	8	100	300

[a]STD: standard deviation, NU: non-uniformity.

For cost-effective utilization of the expensive III-V semiconductor material, often a full-wafer bonding is not the preferred approach. Therefore, in the subsequent sections we will elaborate on quarter-wafer bonding, multiple die-to-wafer bonding and single die-to-wafer bonding. We will start off with the results obtained on Pyrex glass wafers, after which the application of the developed process to bond onto patterned and planarized SOI waveguide circuit wafers is demonstrated.

3.2. Quarter-to-wafer bonding

To show the reliability of the presented method even for a quarter wafer bonding, 5 bonding experiments were performed by bonding a quarter of an InP wafer to a Pyrex glass wafer. A similar analysis of the bonding quality and thickness uniformity was performed, which is summarized in Table 2. These results illustrate that the uniformity and reproducibility of the process is similar to that of the full wafer bonding. The bonding interface is shown in Fig. 3(a), showing a large bonded surface yield. The interference fringes at the rounded edge of the quarter wafer are due to the tapering of the InP wafer near its edges.

While the bonding recipe was originally developed for ultra-thin DVS-BCB bonding layers, some applications require thicker bonding layers, i.e. several hundreds of nm to micrometers thick. In this case, after choosing the right DVS-BCB dilution, the same method was applied for bonding. To achieve a good bonding uniformity, the DVS-BCB was partially cured at 180° C prior to bonding (instead of at 150° C). Figures 3(b) and 3(c) show two bonding interfaces with partial curing at 150°C and 180°C for 15 minutes respectively. The DVS-BCB thickness in the first bonding has an average thickness of 130 nm and a variation of around 70 nm, while the second pair has average thickness of 113 nm and variation less than 10 nm, clearly illustrating the need to partially cure at higher temperatures for uniform bonding layer thicknesses. The same procedure was applied on two other quarters with less diluted DVS-BCB to achieve a bonding layer thickness around 1000 nm. The results, illustrated in Figs. 3(d)-3(e) show an average thickness around 1050 nm and variation around 250 nm for the first pair and an average thickness of 1050 nm and around 30 nm variation for the second pair. In this case, a 180°C soft-bake was applied for 15 min and 30 min for both
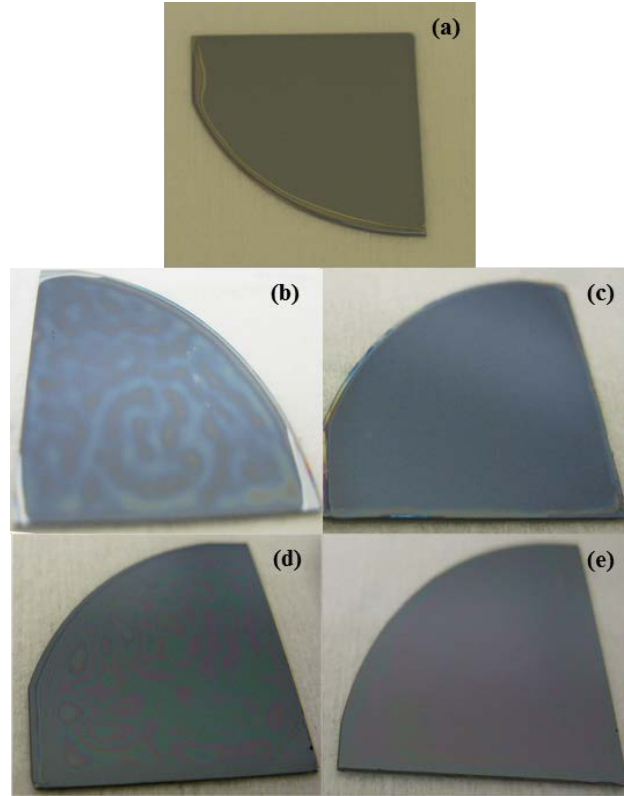
Fig. 3. (a) A quarter InP wafer bonded on a Pyrex glass wafer using a 50 nm thick DVS-BCB bonding layer thickness; (b) A quarter InP wafer DVS-BCB bonded on Pyrex glass using a 130 nm thick DVS-BCB bonding layer using partial precuring at 150°C for 15 minutes; The color fringes result from DVS-BCB thickness variations. c) A quarter InP wafer DVS-BCB bonded on Pyrex glass using a 130 nm thick DVS-BCB bonding layer by partially curing at 180°C, showing no color fringes, resulting in a uniform bonding layer thickness. (d) A quarter InP wafer bonded on a Pyrex glass wafer DVS-BCB bonded on Pyrex glass using a 1050 nm DVS-BCB bonding layer thickness. The color fringes result from DVS-BCB thickness variations by partial precuring at 180°C for 15 min. e) A quarter InP wafer bonded with partially cured DVS-BCB @ 180°C for 30min, without the color fringes, resulting in a uniform bonding layer thickness.

samples respectively. This illustrates again that a well-adapted pre-curing time and temperature is required to obtain a uniform bonding interface.

While the bonding process was developed on Pyrex glass wafers for ease of bonding interface assessment, III-V epitaxial layer transfer in a photonic integrated circuit context is mostly geared towards the integration of the III-V material on a SOI waveguide circuit, as discussed in the introduction, for the realization of hybrid III-V/silicon photonic integrated circuits. For this, the III-V epitaxial layer stack needs to be transferred to the silicon waveguide circuit.

Given the relatively high topography (400 nm) of the silicon waveguide circuit, the waveguide trenches were filled with oxide, in order to obtain a planarized waveguide circuit, to which the III-V layer can be transferred. The DVS-BCB was spin-coated on the III-V side, to avoid the presence of DVS-BCB on the parts of the SOI wafer not covered with III-V. The quasi-planar SOI waveguide circuits were fabricated in a CMOS pilot line in CEA-LETI on 8 inch wafers [7]. The original SOI wafer had 100-150 nm planarized SiO_x on top of the waveguides. However, to achieve an ultra-thin separation between the III-V layer and the silicon waveguide, needed for most III-V/SOI laser structures, the SiO_x was etched back using
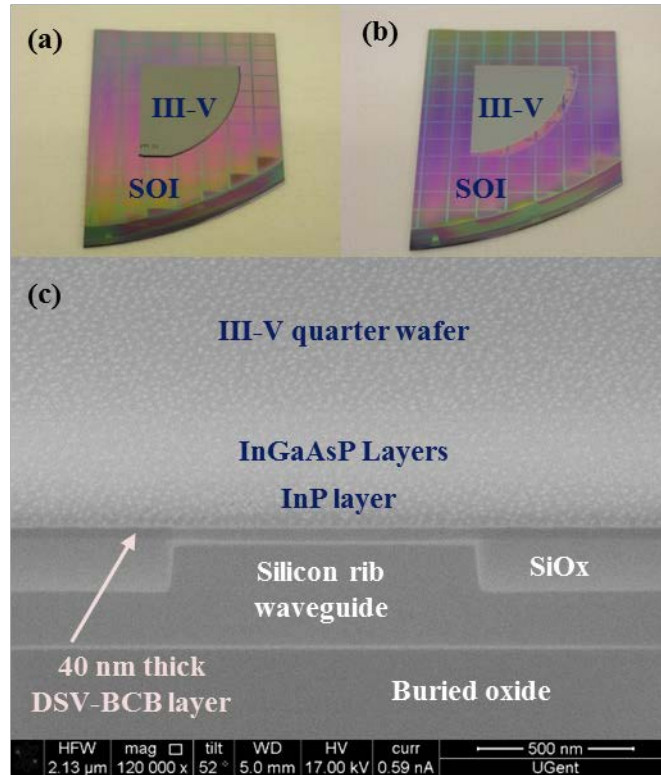
Fig. 4 . E pitaxial q uarter III-V wafer b onded o n quasi-planarized S OI: (a) b efore s ubstrate removal; (b) after substrate removal; (c) SEM image of the bonding interface.

a HF-based wet etching process on a d ie-scale. The results are shown in Fig. 4, showing a well transferred epitaxial layer stack, with bonding layer thicknesses, uniformity and surface yield comparable to those achieved on a P yrex wafer. A gain, the tapering o f the I nP wafers near the edge of the wafer compromises the bonding quality there, which cannot be avoided.
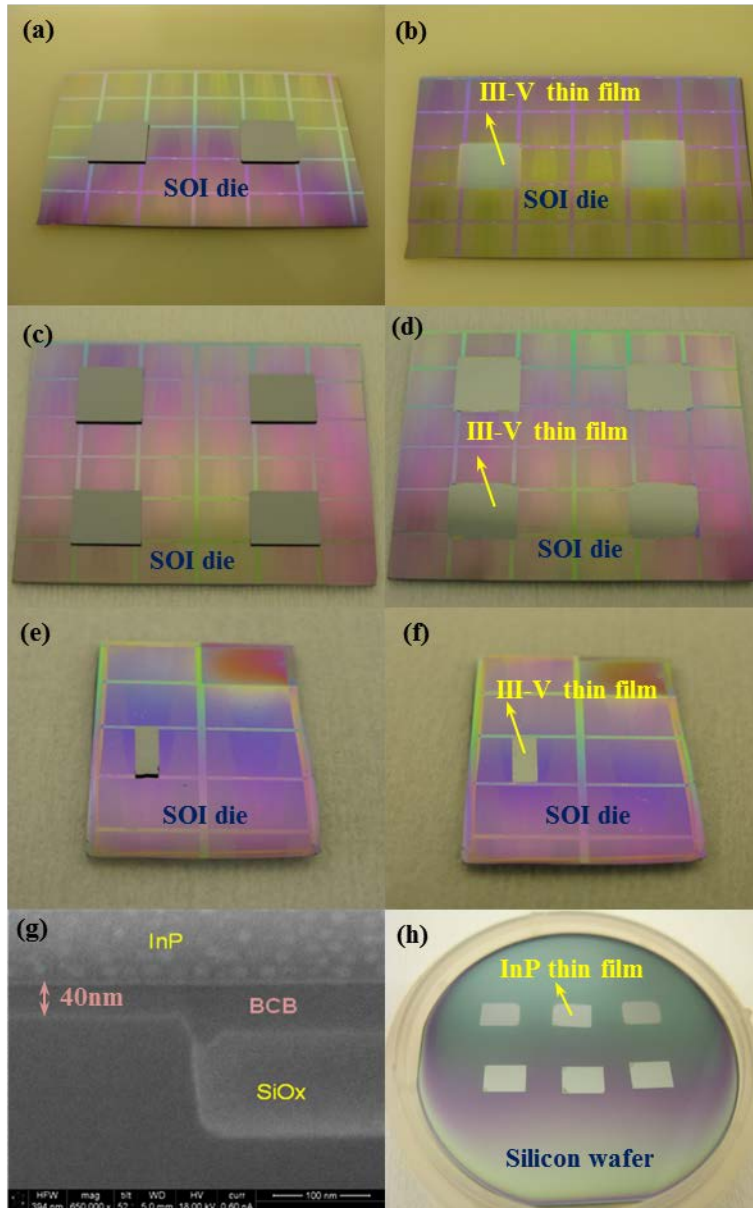
Fig. 5. (a-b) two epitaxial 0.3 cm² III-V dies bonded on a planarized SOI die before and after the substrate removal process; (c-d) four epitaxial 0.3cm² III-V dies bonded on a planarized SOI die before and after the substrate removal process; (e) SEM image of the bonding interface; (f) 6 InP-membranes (with an individual die area of 0.2 cm²) bonded on a 50 mm silicon wafer; (g) cross-section of the bonding interface; (h) 1.3 mm by 4 mm die transferred to a planarized SOI substrate before and after substrate removal.

3.3. Multiple die-to-wafer bonding

Commercial silicon and CMOS production is carried out on wafer diameters of 200 mm and above, while III-V substrates used in photonics applications have typical diameters of less than 100 mm, indicating that wafer-to-wafer bonding will often not be the preferred approach. Moreover, bonding of large III-V areas would result in a waste of material in chip areas were the transferred material is not needed. Therefore, a cost-effective approach in heterogeneous

integration requires III-V material to be bonded in small areas of the SOI photonic wafer. We focus on a multiple die-to-wafer bonding process where III-V dies would be bonded to a SOI die or a full SOI wafer. Since the presented method uses contacting of the dies at room temperature, individual dies can easily be pick-and-placed onto a silicon target wafer. They can be aligned with an accuracy of 500μm without any extra tools or can be placed more accurately using a flip-chip machine.

In order to demonstrate multiple die-to-wafer bonding, 0.3 cm^2 III-V dies were transferred to a quasi-planarized SOI die (fabricated by CEA-LETI), using the ultra-thin bonding recipe. The results are shown in Figs. 5(a)-5(d). Results show a two-die and four-die bonding with a bonding layer thickness less than 50 nm. The III-V dies in this case were still relatively large (0.5 cm^2). In order to demonstrate the true potential of die-to-wafer bonding, dies of 1.3 mm by 4 mm were transferred (which is a typical III-V die space one would need to make a 32 channel laser array), using the ultra-thin bonding recipe. This is shown in Figs. 5(e)-5(f). A cross-section of the bonding interface illustrating the ultra-thin bonding layer thickness is shown in Fig. 5(g). Figure 5(h) shows six III-V dies bonded to a 50 mm silicon wafer with 1.5μm-thick layer of SiO$_x$ on top. The InP films were afterwards etched away using a wet etching solution to measure the thickness and uniformity of the DVS-BCB bonding layer. A DVS-BCB: mesitylene dilution of 1:8 (v/v) was used in the experiment, spin coated at 2500 rpm, resulting in an average bonding layer thickness of 50 nm, varying by ±5 nm over all six dies. This shows the good uniformity over the whole bonding area and a high reproducibility of the nominal bonding layer thickness from die to die.
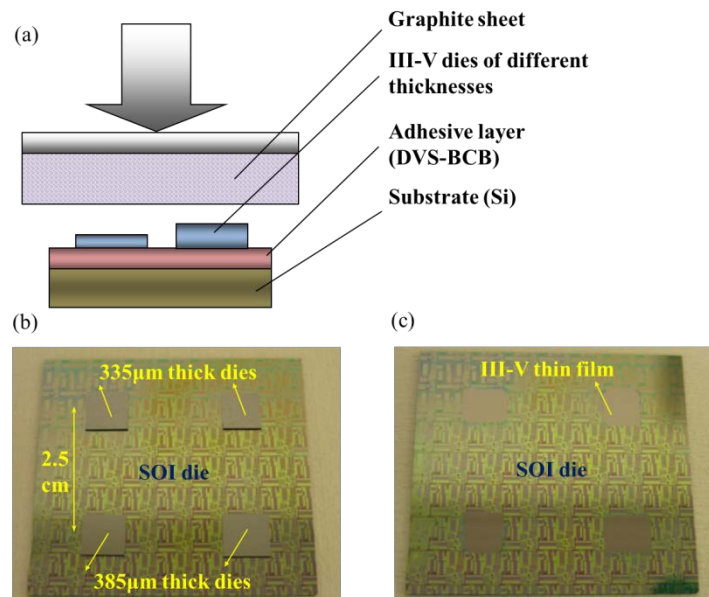

Fig. 6. Four-die bonding on planarized SOI with different substrate thickness, using a graphite foil to compensate for die-thickness variations: (a) schematic; (b) before substrate removal; (c) after substrate removal.

While in the previous experiments nominally identical III-V dies were used, in particular situations there is a need for bonding different types of III-V dies on a single SOI die or wafer (e.g. a die containing laser epitaxy and a die containing photodetector epitaxy). This typically results in dies of different height and size to be bonded, which is difficult to achieve using the classical bonding recipe. Here we show that by applying the new bonding recipe, in combination with a graphite foil between the dies and the bonding head, four-die bonding using two different epitaxial layer stacks (with about 50 μm difference in substrate thickness)

can b e ach ieved. T he g raphite f oil i s used t o co mpensate f or t hese t hickness variations i n order to distribute the pressure evenly over all dies during the bonding, as is illustrated in Fig. 6. R ecently, heterogeneously i ntegrated I II-V/silicon la sers a nd p hotodetectors, u sing th is 'cold bonding' method have been demonstrated [7,19–21]. The results illustrate the robustness and s olid bon ding strength during t he I II-V opt o-electronic co mponent fabrication a nd we believe it can provide a promising alternative to a direct bonding technique for the fabrication of integrated photonic components.

3.4. Characterization of the bonded film

Beside the characterization of the bonding quality, the quality of the transferred epitaxial film also needs to be assessed. This is performed in this work by evaluating the photoluminescence and X-ray di ffraction r ocking c urves of the e pitaxial film before and a fter the bon ding. F or this s tudy, a q uasi-planarized S OI di e with 400 nm silicon h eight was used a nd a III–V epitaxial wafer c onsisting o f an InGaAsP-based M QW laser s tructure was grown on a s emi-insulating InP substrate by metallorganic vapor phase epitaxy (MOVPE).
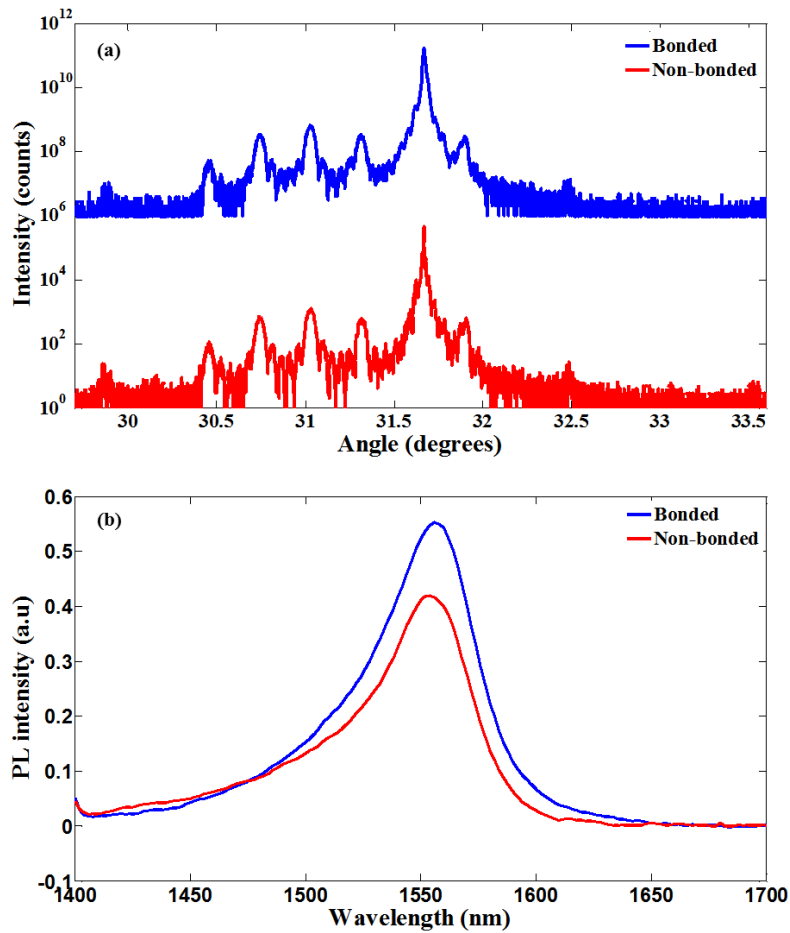

Fig. 7 . (a) X -ray d iffraction ro cking c urves (b oth c urves a re o ffset f or c larity) a nd (b) photoluminescence s pectra o f t he InP/InGaAsP epitaxial l ayer s tack o n its o riginal g rowth substrate (red) and a fter t ransfer t o an S OI waveguide c ircuit (blue) u sing t he c old b onding method.

The structure consists of a 200 nm n-type InP layer, a 6 quantum well $In_{0.81}Ga_{0.19}As_{0.24}P_{0.76}$ (8 nm) active region with $In_{0.76}Ga_{0.24}As_{0.53}P_{0.47}$ (10 nm) barriers, sandwiched in between two 100 nm thick $In_{0.76}Ga_{0.24}As_{0.53}P_{0.47}$ separate confinement heterostructure layers followed by a 1.5 μm thick p-type InP layer and a 100nm thick $In_{0.76}Ga_{0.24}As_{0.53}P_{0.47}$ etch stop layer. Figure 7(a) shows the direct comparison of the measured rocking curves at the center of the as-grown and the bonded epitaxial layer stack. All MQW satellites can be probed at nearly identical positions with no peak broadening, indicating well-preserved crystalline structural integrity.

Photoluminescence (PL) characteristics of the as-grown and transferred epitaxial layers were also compared as a measure for epitaxial layer quality. Measurements were performed at 300 K using a 980 nm, 0.5 mW pump source and each sample was measured three times at different spots, both for the bonded sample (after InP substrate removal) and for the reference as-grown sample. Figure 7(b) shows the photoluminescence spectra for both cases. Compared to the as-grown epilayer, the well-preserved photoluminescence intensity, peak emission wavelength and full width at half maximum (52 nm after bonding and 48 nm before bonding) indicates that the bonding process does not deteriorate the optical performance of the transferred epitaxial layer stack. The different peak intensities in PL measurements is due to the different substrate for the bonded and non-bonded samples. Bonding strength measurements have not been performed in this work; however, in earlier work it has been reported [8], in which shear stress tests were performed on bonded samples. These measurements indicate that there is no significant impact of the DVS-BCB thickness on the maximum shear stress values, which are around 2 MPa, which suggests a high bonding strength.

4. Conclusions

In this paper a new method for the integration of InP-based semiconductor epitaxy onto silicon substrates and silicon photonic integrated circuits is presented. The "cold bonding" method significantly simplifies the preparation process for machine-based bonding in a wafer-to-wafer, die-to-wafer and multiple die-to-wafer adhesive bonding procedure. The demonstrated DVS-BCB bonding layer thickness is very uniform and ultra-thin DVS-BCB bonding layers (<50 nm) can be achieved. Additionally, we developed the process for simultaneous bonding of multiple III-V dies with different thicknesses, suitable for the heterogeneous integration of different types of III-V components on a SOI photonic circuit. While this process was originally developed for InP-based compounds, the bonding of other III-V semiconductors and other epitaxial materials in general can be envisioned.

Acknowledgments