Influence of Jitter on Limit Cycles in Bang-Bang Clock and Data Recovery Circuits

Marijn Verbeke, Pieter Rombouts, Arno Vyncke, and Guy Torfs

***Abstract*—In Bang-Bang (BB) Clock and Data Recovery circuits (CDR) limit cycles can occur, but these limit cycles are undesired for a good operation of the BB-CDR. Surprisingly however, a little bit of noise in the system is beneficial, because it will quench the limit cycles. Until now, authors have always assumed that there is enough noise in a BB-CDR such that no limit cycle occurs. In this work, a pseudo-linear analysis based on describing functions is used to investigate this. In particular, the relationship between the input noise and the amplitude of eventual limit cycles is investigated. An important result of the theory is that it allows to quantify the influence of the different loop parameters on the minimal amount of input jitter needed to destroy the limit cycle. Additionally, for the case that there is not enough noise, the worst case amplitude of the limit cycle (which is unavoidable in this case) is quantified as well. The presented analysis exhibits excellent matching with time domain simulations and leads to very simple analytical expressions.**

***Index Terms*—Modeling, Describing Functions, Bang-Bang (BB) Phase Detector (PD), Charge Pump (CP) Clock and Data Recovery (CDR), jitter, limit cycle.**

I. Introduction

CLOCK and Data Recovery (CDR) using a Phase Locked Loop (PLL) with a Bang-Bang Phase Detector (BB-PD) is an established technique in high speed applications [1]–[5]. These BB-PDs are simple, fast and accurate. However, the behavior of the CDR is highly non-linear which complicates the analysis. Nevertheless, there have been several publications which predict the characteristics of BB-CDR such as jitter transfer, jitter tolerance and jitter generation [6]–[8]. All these papers assume that the CDR operates in its normal working area, which means that the CDR does not have a limit cycle. In most applications, these limit cycles are undesired as they produce unwanted spurious tones or peaking in the recovered clock's output spectrum [9]. Hence, it is necessary to predict whether the CDR has a limit cycle.

The numerous amount of studies performed about the presence of limit cycles, indicate the importance of this research topic. However, most of the previously published work focuses on the domain of digital BB-PLL [9]–[14] and very little research has been conducted about the occurrence of limit cycles in charge pump CDRs.

It is important to note that the analyses applied for digital PLLs cannot be easily mapped to a charge pump CDR: firstly, only PLLs are considered, which use a clock signal as input. In most cases this clock is provided from a very clean reference. This is very different from CDR applications where the reference jitter on the input data is the dominant noise source in the loop [9]. In addition, these analyses are performed in the digital domain. The considered loop filters are usually first order filters, while in CP-PLLs a second order loop filter is typically used.

In recent years, there has been some prior related work on limit cycles in Bang-Bang Clock and Data Recovery circuits: e.g. in [15], a stability analysis of BB-CDRs is performed. But, unlike in our work, no clear distinction is made between the case with or without limit cycles.

An important related work is [16], where describing functions are used to elaborate on the jitter tolerance, the jitter generation and the jitter transfer. Throughout the core of the paper, it is assumed that there are no limit cycles in the system, but also a qualitative analysis about the amount of jitter that is needed to quench limit cycles is already included.

Our work is complementary to [16], and provides an extensive and quantitative analysis of the occurrence of limit cycles in BB-CDR's. For this, describing function techniques as used in [16], are further exploited. The proposed analysis is able to accurately predict the occurrence of a limit cycle as well as its amplitude. This leads to the quantification of the input jitter necessary to quench a limit cycle as well as the worst case limit cycle amplitude, as a function of the different loop parameters.

The paper is organized as follows: the Bang-Bang CDR is reviewed in Section II. In Section III, the pseudo-linear model using describing function theory for a BB-PD is presented. This model is incorporated in the CDR and the analysis is discussed in Section IV. The simulation results are given in Section V and the influence of the CDR design parameters is presented in Section VI. In Section VII, further analytical approximations are made, which result in easy-to-use equations for CDR design. Finally, Section VIII concludes the paper.

II. Bang-Bang CDR

Fig. 1 shows the schematic of a general Charge Pump (CP) Clock and Data Recovery circuit (CDR). The CDR consists of a Bang-Bang Phase Detector (BB-PD), a charge pump, a loop filter and a Voltage Controlled Oscillator (VCO). The BB-PD

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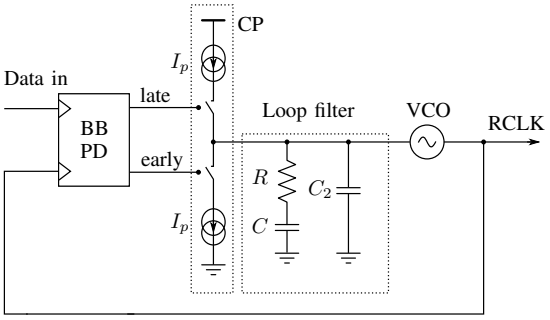

Fig. 1. A Charge Pump Phase Locked Loop based Clock and Data Recovery circuit.

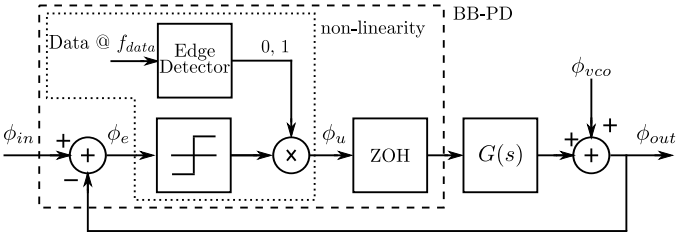

Fig. 2. The behavioral model of a BB-CDR.

compares the edges of the incoming data with those of the recovered clock (RCLK). Depending on the arrival of a new data edge with respect to the edge of the RCLK, an early or late signal will be generated which will switch a current I_p from or to the loop filter respectively. This loop filter adjusts the control voltage of the VCO to reduce the phase error. If no data transition occurs, the BB-PD does not generate any signal (early or late) and the VCO is not adjusted.

This circuit is converted to a behavioral model in the phase domain which is represented by Fig. 2. The BB-PD in the CDR is replaced by an ideal subtraction, a comparator, an edge detector and a zero-order hold (ZOH) block. The phase of RCLK ϕ_{out} is subtracted from the phase of the incoming data ϕ_{in}, followed by an ideal comparator. The edge detector outputs every period $\frac{1}{f_{data}}$ a '1', respectively a '0', when a data transition occurs or not. This signal is multiplied with the value of the comparator and is sent through the ZOH, resulting in a signal ϕ_u that only adjusts the control voltage when a data transition takes place. In [16], the BB-PD is modeled as a slicer with a ternary output, resulting in an equivalent behavior. The combination of the CP, the loop filter and the VCO is equivalent to the linear block $G(s)$:

$$G(s) = \frac{\omega_0}{s} \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}} \exp\left(-sT_{d,l}\right) \tag{1}$$

where ω_z represents the frequency of the zero, ω_p the frequency of the pole, ω_0 the overall amplification factor of the linear block and $T_{d,l}$ the delay of the signal path through the CDR. This loop delay is the sum of all gate and component delays in the loop [17] and also includes any delay introduced by re-timing and demultiplexing the data in the PD [1], [2], [18]. Note that if ω_0 has a value between ω_z and ω_p, ω_0 also represents the unity gain frequency. In this paper the assumption is made that ω_0 and ω_p will always be sufficiently larger than ω_z, such that the zero has little effect. For the sake of completeness, ω_z, ω_p and ω_0 can be written down in terms of their component values (Fig. 1):

$$\omega_z = \frac{1}{RC} \tag{2}$$

$$\omega_p = \frac{C + C_2}{RCC_2} \tag{3}$$

$$\omega_0 = K_{vco} I_p \frac{RC}{C + C_2} \tag{4}$$

In the equations above, K_{vco}, I_p, R, C and C_2 respectively represent the gain of the VCO [Hz/V], the current sources of the CP [A] and the resistance [Ω] and capacitance [F] values of the loop filter. Finally, the phase noise contributed by the VCO is modeled by ϕ_{vco} in Fig. 2.

This model is a good approximation of the real system: it incorporates the early-late signal based on the sign of the difference of input phase and output phase ϕ_e, the update rate f_{data} of the CDR, the transition density of the data, any delay introduced in the CDR and different noise sources. Note that, this model is also a good representation for a standard Phase Locked Loop when a data transition occurs every clock cycle.

Typically, the data period is much smaller than any time constant in the CDR. Therefore the intrinsic sample and hold operation of the BB-PD, represented by the ZOH block in Fig. 2, can be approximated by a delay of $1/(2f_{data})$ [19]. To simplify further calculations, this delay is added to the delay of the linear block $T_{d,l}$, resulting in the total delay T_d:

$$T_d = T_{d,l} + \frac{1}{2f_{data}} \tag{5}$$

As a result, the analysis can be performed in continuous time.

III. Describing functions: pseudo-linear model

The BB-PD is a highly non-linear block. A powerful method to analyze such a system is the describing function quasi-linearization technique [20]. Here, the input signal of the non-linearity is denoted by the phase error ϕ_e on Fig. 2 and can be decomposed in a sum of basic signal components: e.g. a DC bias $\phi_{e,DC}$, a sinusoid $\phi_{e,s}$ or a random Gaussian process $\phi_{e,n}$. For each component a best-fit linear gain is determined in order to minimize the mean-squared difference between the output of the approximation and the output of the non-linearity. Of course, if a large number of these basic signal components is present in the input signal, the complexity of the describing functions will increase.

Fig. 3 visualizes this describing function model in the time domain for the case that the non-linearity is a comparator (Fig. 3(a)). In this example the input of the non-linearity ϕ_e is decomposed in a sinusoidal component $\phi_{e,s}$ and a random Gaussian component $\phi_{e,n}$. For each component there is a corresponding linear gain. The sum of the amplified signal components results in an approximation of the output signal of the non-linearity $\phi_{u,approx}$. This is represented by Fig. 3(b), which is the original describing function model of [20]. To increase the accuracy, the linearization error ϕ_q, which is defined as the difference between the approximated output $\phi_{u,approx}$ and the actual output ϕ_u (Fig. 3(c)), is included in

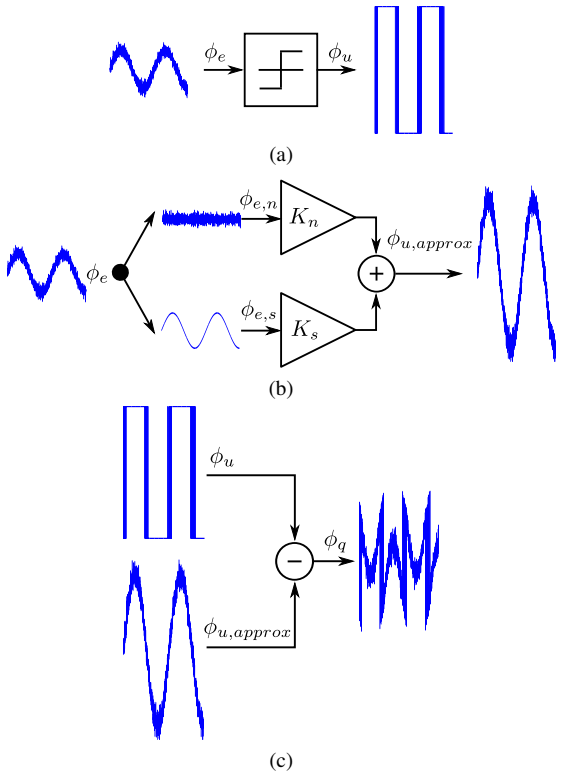

Fig. 3. A time domain example of the describing function model for a non-linearity. (a) The characteristic of a comparator (a non-linearity). (b) The describing function characteristic according to the original approach in [20]. (c) The definition of the linearization error ϕ_q, which is included in [16] and in our pseudo-linear analysis.

our pseudo-linear model. This improvement was also already performed in [16].

A. Random-Input Describing Functions

The simplest possible case to study the behavior of the CDR, correspond to the situation where there is only one signal component present at the input of the non-linearity ϕ_e. As noise is present in every system, this implies that this signal component originates from a random Gaussian process and will be denoted by $\phi_{e,n}$. This signal component $\phi_{e,n}$ is normally distributed with zero mean and variance σ_e^2.

The non-linearity of the BB-PD can now be modeled by a single gain block (Fig. 4), for which the gain K_n is calculated using the Random-Input Describing Function (RIDF). Furthermore, the linearization error ϕ_q is also added to the model in Fig. 4. In [16], it was already proven that in this case the linearization error can be accurately modeled by an independent noise source ϕ_q which is uncorrelated to $\phi_{e,n}$. The values of the gain K_n and the variance of the linearization error ϕ_q are given by [16]:

$$K_n(\sigma_e) = \sqrt{\frac{2}{\pi}}\frac{\alpha}{\sigma_e} \quad (6)$$

$$\sigma_q^2 = \alpha - \frac{2}{\pi}\alpha^2 \quad (7)$$

where σ_e, σ_q and α respectively represent the standard deviation of $\phi_{e,n}$ and ϕ_q, and the transition density of the data.

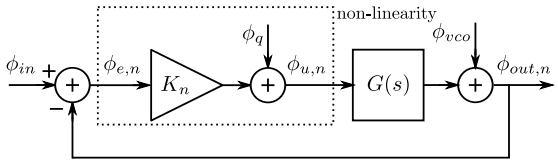

Fig. 4. The RIDF model of a BB-CDR.

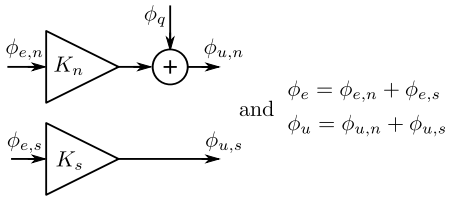

Fig. 5. The GSIDF model of the non-linearity of a BB-PD.

These equations are valid if the bandwidth of the loop filter is much smaller than the data rate and the data transitions occur in a random manner (with probability α)[1]. In our work, we assume that these conditions are also met and therefore Eqs. (6) and (7) are adequate for further analysis.

Note that the gain factor K_n is not a fixed value, but depends on the characteristics of the input signal of the non-linearity, i.e. the standard deviation σ_e. This is a typical property of describing functions.

B. Limit cycles

In some cases, an oscillation can build up and be sustained by the CDR's feedback mechanism. The characteristics of the oscillation are a system property, and are independent on initial conditions. Such an oscillation is called a limit cycle [20].

Further on, the higher harmonics of the limit cycle oscillation, originating from the non-linearity of the BB-PD are neglected. This approach is justified, because the linear block $G(s)$ filters the BB-PD output harmonics such that only a negligible part of the harmonics is fed back to the input of the BB-PD. Hence, the input of the BB-PD is approximated by the sum of a random Gaussian and a sinusoidal component. This way, the Gaussian-plus-Sinusoid-Input Describing Function (GSIDF) has to be applied instead of the simpler RIDF in order to correctly analyze the non-linear system.

C. Gaussian-plus-Sinusoid-Input Describing Function

When a limit cycle with a non-zero amplitude is present, the phase error ϕ_e will consist of the sum of a random Gaussian component $\phi_{e,n}$ and a sinusoidal component $\phi_{e,s}$. $\phi_{e,n}$ is normally distributed with zero mean and variance σ_e^2, while $\phi_{e,s}$ can be written as:

$$\phi_{e,s} = A_e \sin(\omega_s t) = A_e \sin\theta \quad (8)$$

with A_e the amplitude of the limit cycle, ω_s the frequency of the limit cycle and θ the instantaneous phase.

[1]To ensure that this assumption is satisfied, scramblers are typically used to avoid any auto-correlation of the data pattern.

The describing functions of the BB-PD are now determined by the Gaussian-plus-Sinusoid-Input Describing Function. Fig. 5 represents the GSIDF model for the non-linearity in Fig. 2. The sinusoidal $\phi_{e,s}$ and the random Gaussian $\phi_{e,n}$ component are treated separately, each with their corresponding gain factor K_s and K_n. These gain factors are calculated such that the linearization error ϕ_q between the pseudo-linear model and the actual BB-PD is minimized.

For a general non-linear element, denoted by $\phi_u(\phi_e)$, the describing functions can be written down as shown in [20]:

$$K_n(A_e,\sigma_e) = \frac{1}{\sqrt{2\pi}^3\sigma_e^3}\int_0^{2\pi} \mathrm{d}\theta \int_{-\infty}^{\infty} \phi_u(\phi_e)\ \phi_{e,n}\ \exp\left(-\frac{{\phi_{e,n}}^2}{2\sigma_e^2}\right)\ \mathrm{d}\phi_{e,n} \tag{9}$$

$$K_s(A_e,\sigma_e) = \frac{2}{\sqrt{2\pi}^3\sigma_e A_e}\int_0^{2\pi} \mathrm{d}\theta \int_{-\infty}^{\infty} \phi_u(\phi_e)\ \sin\theta\ \exp\left(-\frac{{\phi_{e,n}}^2}{2\sigma_e^2}\right)\ \mathrm{d}\phi_{e,n} \tag{10}$$

where ϕ_e is the input of the non-linearity and is determined by the sum of a random Gaussian component $\phi_{e,n}$ and a sinusoidal component $\phi_{e,s}$.

By substituting the actual BB-PD characteristics in Eq. (9) and Eq. (10), the GSIDFs become:

$$K_n(A_e,\sigma_e) = \frac{\alpha}{\sqrt{2\pi}}\frac{1}{\pi\sigma_e}\int_0^{2\pi}\exp\left(-\frac{1}{2}\left(\frac{A_e\sin\theta}{\sigma_e}\right)^2\right)\mathrm{d}\theta \tag{11}$$

$$K_s(A_e,\sigma_e) = \frac{\alpha}{\pi A_e}\int_0^{2\pi}\mathrm{erf}\left(\frac{A_e\sin\theta}{\sqrt{2}\sigma_e}\right)\sin(\theta)\ \mathrm{d}\theta \tag{12}$$

In the equations above, K_n, K_s, A_e and σ_e respectively represent the noise gain and sinusoidal gain, the amplitude of the sinusoidal component of ϕ_e (limit cycle) and the standard deviation of the noise component of ϕ_e. These equations look complex, but can be easily evaluated with modern mathematical tools: e.g. the sinusoidal gain K_s is plotted in Fig. 6 as a function of A_e for increasing values of σ_e. Fig. 6 clearly shows that the sinusoidal gain converges when the noise at the input of the non-linearity becomes negligible w.r.t. the sinusoidal component. For this envelope, the Gaussian-plus-sinusoid-input describing function is reduced to the (single) Sinusoidal-Input Describing Function (SIDF), for which the gain is inversely proportional to the amplitude A_e [20].

In this analysis the input model of the BB-PD is approximated by a random Gaussian plus a sinusoidal component and the higher harmonics of the limit cycle are omitted. However, the linearization error ϕ_q still contains the harmonics originating from the non-linearity of the BB-PD. In order to simplify further analysis, the linearization error ϕ_q is approximated as random Gaussian noise. This allows to include the linearization error ϕ_q in the random Gaussian component of the output of the BB-PD $\phi_{u,n}$ and makes it possible to decompose the CDR into two GSIDF models: one for the sinusoidal component and another one for the random Gaussian component.

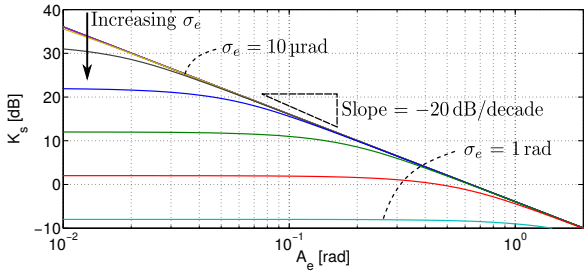

Fig. 6. K_s according to Eq. (12) as a function of the amplitude A_e and the RMS jitter σ_e at the input of the non-linearity. (α = 0.5)

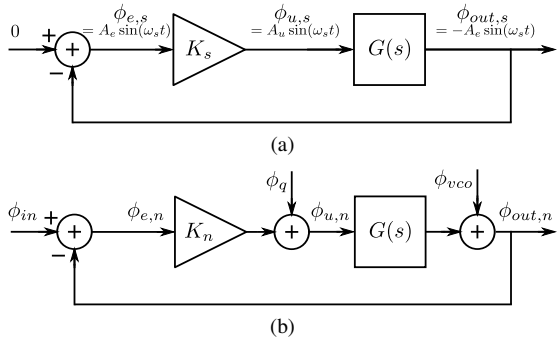

Fig. 7. The GSIDF model of a BB-CDR for (a) the sinusoidal component and (b) the random Gaussian component (identical to the RIDF model in Fig. 4).

The variance of the linearization error σ_q^2 can then be determined as [16]:

$$\sigma_q^2 = \alpha - K_n^2\sigma_e^2 - K_s^2\frac{A_e^2}{2} \tag{13}$$

IV. Pseudo-linear analysis of the CP-CDR

A. System relations

The GSIDF model of Fig. 5 is incorporated in the complete model of the CDR. This results in two block diagrams and is represented by Fig. 7. The phase error ϕ_e, the output of the BB-PD ϕ_u and the output of the CDR ϕ_{out} are the sum of their random Gaussian and their sinusoidal component, i.e. at every node x we can write:

$$\phi_x = \phi_{x,n} + \phi_{x,s}$$

When this system is excited by only a random Gaussian process, any sinusoid appearing in the system would have to be caused by a limit cycle (which, as discussed above, is approximated by its fundamental sinusoidal component). The condition for self-oscillation is given by:

$$K_s(A_e,\sigma_e) = \left|\frac{1}{G(j\omega_s)}\right| \equiv K_s^* \tag{14}$$

with ω_s the oscillation frequency of the limit cycle for which $G(s)$ reaches 180° phase lag, i.e. the Barkhausen criterion.

In addition, the random Gaussian component in the CDR must satisfy the following equations:

$$\phi_{e,n} = H_1(s)\ \phi_{in} + H_2(s)\ \phi_q \tag{15}$$

$$H_1(s) = \frac{1}{1+K_nG(s)} \tag{16}$$

$$H_2(s) = -\frac{G(s)}{1+K_nG(s)} \tag{17}$$

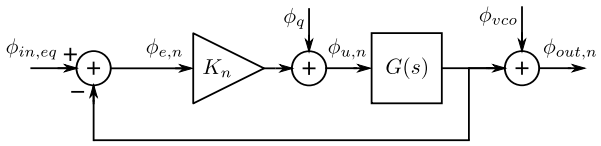

Fig. 8. The altered GSIDF model of a BB-CDR for the random Gaussian component (equivalent to the RIDF model in Fig. 4).

where K_n and K_s are given by Eq. (11) and Eq. (12), and ϕ_q, ϕ_{in} and $\phi_{e,n}$ are respectively the linearization error, the input noise and the random Gaussian component of the phase error. Finally, the variance of the phase error σ_e^2 is calculated by integrating the power spectral density S_{ϕ_e} over the noise bandwidth B:

$$\sigma_e^2 = \int_B S_{\phi_{in}} |H_1(j\omega)|^2 + S_{\phi_q} |H_2(j\omega)|^2 \, \mathrm{d}\omega \qquad (18)$$

where $S_{\phi_{in}}$ and S_{ϕ_q} are the power spectral densities of the input random jitter and the linearization error. The noise bandwidth reaches from DC to $f_{data}/2$, due to the fact that the system only reacts on a data edge and hence implicitly incorporates a sampling operation [16]. To match with the simulations (see Section V-VI), also a narrow band around the oscillation frequency was removed, because (as outlined in Section V-A) resonating noise can not be distinguished from a limit cycle in the simulations.

Without loss of generality, the phase noise of the VCO is incorporated in the input noise ϕ_{in}. This is shown in Fig. 8: the phase noise of the VCO ϕ_{vco} can be split and transferred such that ϕ_{vco} directly adds to the output and also the input of the loop. In this way, the total noise contribution at the input can be written as $\phi_{in,eq}$ where:

$$\phi_{in,eq} = \phi_{in} - \phi_{vco}$$

Furthermore, the addition of ϕ_{vco} at the output is outside the feedback loop and does not influence the limit cycle behavior.

Further on, $\phi_{in,eq}$ is approximated as white noise, which simplifies the pseudo-linear analysis. This simplification is valid in most CDR applications, where the input jitter is the dominant source of phase noise. However, if the phase noise of the VCO is not negligible w.r.t. the input noise than a more accurate model for the phase noise has to be used (see e.g. [21]). But this is outside the scope of this work.

Now, Eqs. (11)–(14) and (18) are combined to constitute a system of equations, where the different parameters are recursively dependent on each other. Every realistic solution of this system with 5 equations and 5 unknowns for a given value of σ_{in} indicates the existence of a limit cycle.

B. Algorithm

Eventually, we want to solve this system of equations such that we obtain the amplitude of the limit cycle A_e as a function of the input jitter σ_{in}. This however requires several calculation iterations due to the recursive dependencies. A way to circumvent this, is described in Algorithm 1. This algorithm calculates the input jitter σ_{in} as a function of the limit cycle amplitude A_e and consists of the following steps: firstly, the assumption is made that a limit cycle exists and hence the GSIDF analysis is applicable.

Algorithm 1: Calculation procedure for obtaining K_s, K_n, A_e, σ_e and σ_q which correspond to σ_{in}^2

Assume limit cycle exists;
Determine ω_s and K_s^* which satisfy the Barkhausen criterion: Eq. (14);
foreach *value* $A_e(i)$ *of* A_e **do**
  $\sigma_e(i) \leftarrow$ invert Eq.(12) for $A_e = A_e(i)$ and $K_s = K_s^*$;
  $K_n(i) \leftarrow$ evaluate Eq. (11) using $\sigma_e(i)$ and $A_e(i)$;
  $\sigma_q(i) \leftarrow$ evaluate Eq. (13) using $\sigma_e(i)$, $A_e(i)$, K_s^* and $K_n(i)$;
  $\sigma_{in}(i) \leftarrow$ evaluate Eq.(19) using K_s^*, $K_n(i)$, $A_e(i)$, $\sigma_e(i)$ and $\sigma_q(i)$;
end

Subsequently, the amplification factor K_s^* that causes a limit cycle is determined according to Eq. (14). Thereafter, the amplitude of the limit cycle A_e is swept. For each value of A_e represented by $A_e(i)$ and given the gain $K_s = K_s^*$, the corresponding standard deviation of the noise component of the phase error $\sigma_e(i)$ is calculated by inverting Eq. (12). This is a numerical procedure, but with contemporary numerical tools this can be easily determined. The obtained value of $\sigma_e(i)$, in addition to the given amplitude $A_e(i)$, gives rise to a sinusoidal gain K_s equal to K_s^*.

Then for each set of $A_e(i)$ and $\sigma_e(i)$, we can immediately calculate $K_n(i)$ and $\sigma_q(i)$ by utilizing Eq. (11) and Eq. (13). Finally, Eq. (18) is rearranged, such that the corresponding $\sigma_{in}^2(i)$ can be determined by Eq. (19):

$$\sigma_{in}^2 = \frac{\sigma_e^2 - \dfrac{\sigma_q^2}{B}\displaystyle\int_B |H_2(j\omega)|^2 \, \mathrm{d}\omega}{\dfrac{1}{B}\displaystyle\int_B |H_1(j\omega)|^2 \, \mathrm{d}\omega} \qquad (19)$$

with $H_1(j\omega)$ and $H_2(j\omega)$ given by Eq. (16) and Eq. (17) respectively.

With the procedure described above, σ_{in}^2 will give rise to the determined values of K_s, K_n, A_e and σ_e. Note that this algorithm requires no iterations in the calculation of σ_{in}^2, K_s, K_n, σ_e and σ_q for a particular value of A_e.

C. Application of the algorithm

Using the algorithm above, the relation between the amplitude of the limit cycle and the corresponding RMS input jitter σ_{in} is calculated. This is done for a BB-CDR with the following parameters: f_{data} = 10 GHz, $\omega_z = 2\pi \cdot 300$ kHz $\omega_0 = 2\pi \cdot 3$ MHz, $\omega_p = 2\pi \cdot 30$ MHz and T_d = 3 ns. These parameters are of the order of the parameters used in a currently developed system in our design group. The large delay is due to the parallelization of the BB-PD and the demultiplexing of the data in the BB-PD. In addition, we assume that random data is received at the input of the BB-PD. The probability that a transition occurs for the data sequence is 0.5 and this is thus equal to the transition density α.

The calculated result is presented in Fig. 9. From the plot it is clear that in the case that no input jitter is present, the CDR

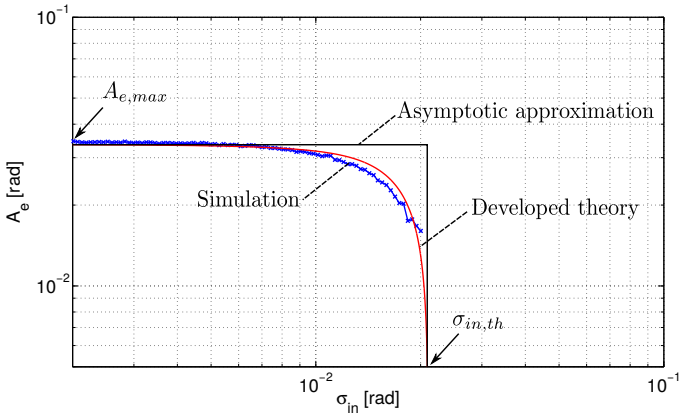

Fig. 9. The limit cycle amplitude A_e as a function of the RMS input jitter σ_{in}. The simulation results where performed with: f_{data} = 10 GHz, $\omega_z = 2\pi \cdot 300$ kHz, $\omega_0 = 2\pi \cdot 3$ MHz, $\omega_p = 2\pi \cdot 30$ MHz and T_d = 3 ns.

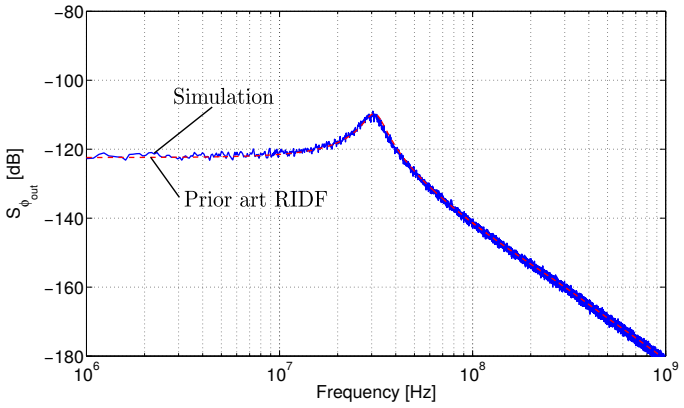

Fig. 10. The power spectrum $S_{\phi_{out}}$ of the same CDR as in Fig. 9 for an input noise level $\sigma_{in} = \sqrt{2} \cdot \sigma_{in,th}$.

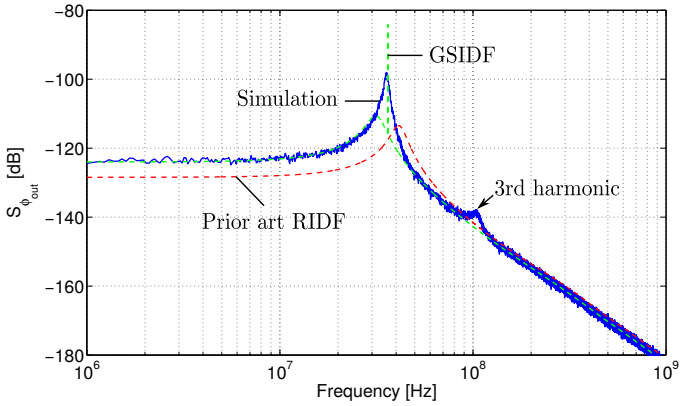

Fig. 11. The power spectrum $S_{\phi_{out}}$ of the same CDR as in Fig. 9 for an input noise level $\sigma_{in} = \frac{\sigma_{in,th}}{\sqrt{2}}$. The simulation results are compared to the prediction where the CDR does not contain any limit cycles: i.e. the RIDF and to the prediction where a limit cycle is present in the CDR: i.e. the GSIDF.

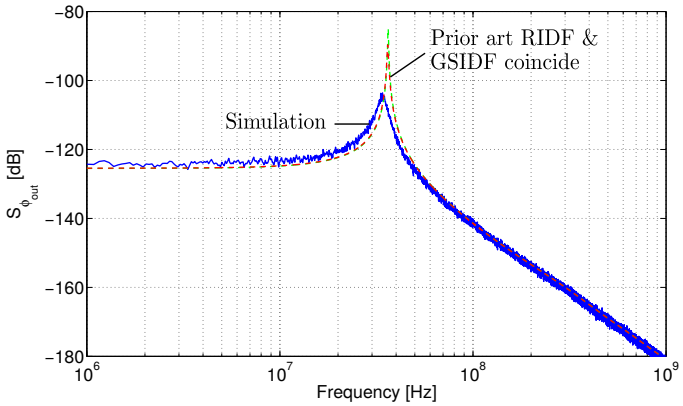

Fig. 12. The power spectrum $S_{\phi_{out}}$ of the same CDR as in Fig. 9 for an input noise level $\sigma_{in} = \sigma_{in,th}$.

has a limit cycle with a worst case amplitude of $A_{e,max}$. In addition, Fig. 9 shows that above a certain value of σ_{in} there is no corresponding solution for A_e. This means that the noise is large enough to destroy the limit cycle. For lower input noise levels the limit cycle is stable. The transition point is called the threshold RMS input jitter $\sigma_{in,th}$. This is the predicted transition point where the CDR stops to have a limit cycle.

V. Simulation Results

A. Spectra

To validate the theory, several time domain simulation were performed. For a first batch of simulations, the same BB-CDR is used as the one that was used for the calculation of Fig. 9. Some resulting power spectra of ϕ_{out} for several values of RMS input jitter are given in Figs. 10, 11 and 12.

In Fig. 10, the RMS input jitter is equal to $\sqrt{2} \cdot \sigma_{in,th}$. According to the theory no limit cycle is present in the CDR and the prior art RIDF prediction [16] should perfectly match the simulation. The calculated RIDF prediction is also shown in Fig. 10 and it is clear that the simulation and the calculation match nearly perfectly. We can thus conclude that our theory correctly predicts that there is no limit cycle present in the BB-CDR. As a result the RIDF theory correctly models the behavior of the BB-CDR.

On the other hand, in Fig. 11, the RMS input jitter is equal to $\frac{\sigma_{in,th}}{\sqrt{2}}$. Now, the theory indicates that a limit cycle is present. We expect that the Random-Input Describing Function model is inadequate and there will be no match between the simulation and RIDF calculation. This is illustrated in Fig. 11, where it is readily observed that the correspondence with the RIDF is poor. In this case however, the Gaussian-plus-Sinusoid-Input Describing Function (GSIDF) prediction should be valid and is also compared to the simulation in Fig. 11. It is clear that it matches much better than the RIDF result. Nonetheless, there is a small discrepancy between the simulation results and the GSIDF prediction. The reason is that the self-oscillation in the GSIDF is modeled as a perfect sine wave (which corresponds to an infinitely narrow line in the spectrum). However, due to the noise in the system, the actual self-oscillation exhibits some phase noise (which corresponds to a wider peak). This effect is well known in the community of oscillator specialists (see e.g. [21], [22]), and is neglected here. Additionally, the simulated power spectrum also shows a small peak around 100 MHz, which is the third harmonic of the limit cycle oscillation. It originates from the non-linearity of the BB-PD, which is lost in the linearized describing function model. Higher harmonics of the limit cycle, however, are

greatly suppressed by the linear block $G(s)$. This is confirmed by the fact that the third harmonic is very small and higher order harmonics are invisible. Apart from these two second-order effects, the GSIDF calculation matches the simulation almost perfectly.

Finally, for values of σ_{in} close to the threshold RMS input jitter $\sigma_{in,th}$ there is a transition region between a false and a correct prediction by the RIDF theory. Fig. 12 shows that the RIDF prediction coincides with the GSIDF prediction. These calculations are compared to the simulated results and Fig. 12 illustrates that the theory closely predicts the simulation results. However, the figures discussed above show that it is difficult to distinguish jitter peaking from a limit cycle. This makes it challenging to determine the actual amplitude of the limit cycle from the simulation results in the frequency domain. Therefore, the amplitude of the limit cycle is measured in the time domain as proposed in the next section.

B. Amplitude estimations of the limit cycle

Here, time domain simulations were performed with the same BB-CDR parameters as those used in the calculations in Fig. 9. A random Gaussian noise source ϕ_{in} is applied to the input of the behavioral model for which the variance σ_{in}^2 is swept over multiple simulations. For each value of σ_{in}^2, the amplitude of the limit cycle A_e is estimated from the simulation results as follows: a curve fitting algorithm is used to match a sine wave to the time domain simulation data. This allows us to calculate the amplitude A_e of the limit cycle component in the signal ϕ_e and the variance of the noise component of the phase error σ_e^2. However, a data transition does not occur every clock cycle and this influences the behavior of the limit cycle. Therefore, for each simulation the entire set of simulated data (2e6 time steps) is divided into small parts which contain 10 limit cycle periods. The amplitude is estimated for each part and is then averaged out.

However, the curve fitting algorithm has a pitfall: even if the limit cycle amplitude is zero, this algorithm will estimate a non-zero (be it small) value for the limit cycle amplitude. This is due to the presence of noise power at the frequency where the amplitude is estimated. To detect this situation, the Signal-to-Noise Ratio (SNR) of the limit cycle is calculated as well. If this SNR is very small, it is concluded that the above described situation occurs and the solution is rejected. A signal-to-noise ratio of -6 dB is taken as decision criterion: simulation results with a SNR lower than -6 dB are rejected.

The results of the simulations are added to Fig. 9. By comparing the simulation results with the calculated values, its is clear that the theory closely predicts the amplitude of the limit cycle. Furthermore, the (numerical) procedure is about three orders of magnitude faster than the simulation approach for an equal number of data points.

VI. Influence of the CDR design parameters

Now that we are able to predict the amplitude of the limit cycle, the next step is to study the influence of the different CDR design parameters. In order to perform a useful study from a designers point of view, an asymptotic approximation is made of the limit cycle amplitude characteristic. This is also added to Fig. 9. The asymptotic approximation is made as follows: if there is a limit cycle, its amplitude is approximately the worst case amplitude $A_{e,max}$ and if the noise is larger than the threshold RMS input jitter $\sigma_{in,th}$, there is no limit cycle. In this way, the limit cycle amplitude characteristic is reduced to two essential, enveloping figures: i.e. the worst case amplitude $A_{e,max}$ and the threshold RMS input jitter $\sigma_{in,th}$. The influence of the different CDR design parameters on these two figures is further examined.

A. Worst case limit cycle amplitude

Firstly, the worst case amplitude of a limit cycle $A_{e,max}$ and its dependence on the gain ω_0, the pole ω_p and the total loop delay T_d is investigated. As already mentioned, the zero ω_z is assumed to be sufficiently small such that it has little influence. Therefore, this parameter is not considered. Also the cases where the bandwidth of the CDR becomes significant w.r.t. the data rate are rejected. This only occurs when both $\frac{1}{T_d}$ and ω_p are very large. Under these conditions, the derived describing functions are no longer valid.

The calculated and simulated results are displayed in Fig. 13. It illustrates the effect of ω_0, ω_p and T_d on the worst case limit cycle amplitude $A_{e,max}$. The plot shows that the worst case limit cycle amplitude $A_{e,max}$ and the gain ω_0 are linearly proportional. The pole ω_p has only a modest effect on the worst case limit cycle amplitude $A_{e,max}$: a large increase of the pole frequency ω_p will only cause a small decrease in $A_{e,max}$. Furthermore for large values of T_d, although not obvious from the figure, there is also a linear relation between the delay T_d and the worst case limit cycle amplitude $A_{e,max}$. However, for small values of T_d, $A_{e,max}$ rises less than proportional with increasing T_d. From Fig. 13, it can be concluded that the theory closely predicts the simulation results.

Now that the influence on the worst case limit cycle amplitude is examined, it is important to investigate whether this limit cycle prevents correct data recovery. To assume successful data recovery, a reasonable threshold for the worst case limit cycle amplitude $A_{e,max}$ is chosen: i.e. $\frac{\pi}{8}$. This threshold is also displayed on Fig. 13, together with the worst case amplitude $A_{e,max}$ of the CDR design discussed earlier (Fig. 9). The plots show that most CDR designs (including the design discussed in Fig. 9) have a worst case limit cycle amplitude $A_{e,max}$ which is sufficiently small to successfully recover the input data. However, an increase in delay and in the gain of the linear block could lead to large amplitudes which can greatly influence the correct operation of the data recovery.

B. Minimal input noise to quench a limit cycle

As shown in the previous section, the worst case amplitude of a limit cycle is sufficiently small in most CDRs. However, a limit cycle causes severe jitter peaking as demonstrated in Fig. 11. As a result, a limit cycle should be avoided in CDR application where the recovered clock is further utilized in the system. Therefore, it is interesting to study how much noise is

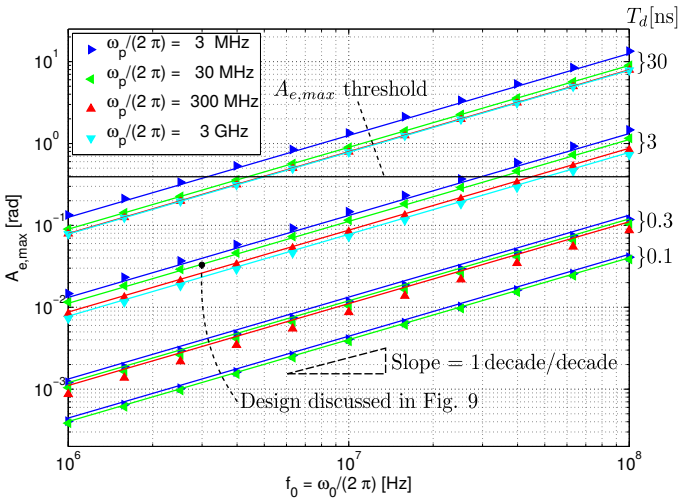

Fig. 13. The worst case limit cycle amplitude $A_{e,max}$ as a function of the gain ω_0 for different pole frequencies ω_p and delays T_d. The corresponding calculated results (solid lines) and simulation results (markers) are represented with the same color.

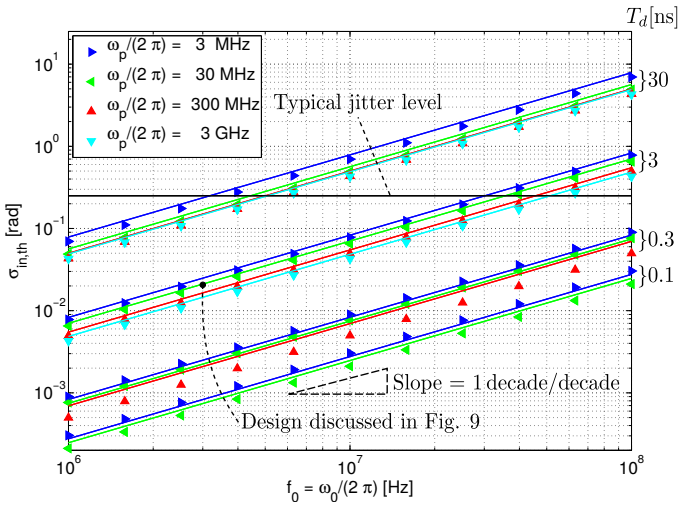

Fig. 14. The threshold RMS input jitter $\sigma_{in,th}$ as a function of the gain ω_0 for different pole frequencies ω_p and delays T_d. The corresponding calculated results (solid lines) and simulation results (markers) are represented with the same color.

needed to quench the limit cycle. The results of this study are shown in Fig. 14. Here, the threshold RMS input jitter $\sigma_{in,th}$ (as defined above) is represented as a function of the CDR parameters. Both the theoretical result (based on the describing function theory) as well as the experimental result (obtained from simulations such as described above) are shown.

The effect of ω_0, ω_p and T_d on the threshold RMS input jitter $\sigma_{in,th}$ is illustrated by Fig. 14. The threshold RMS input jitter $\sigma_{in,th}$ is directly proportional to the gain ω_0. Additionally, the pole ω_p has a modest effect on the threshold RMS input jitter $\sigma_{in,th}$. Fig. 14 also shows the effect of T_d on the threshold RMS input jitter $\sigma_{in,th}$. For large values of T_d, there is a linear relation between the total delay T_d and threshold RMS input jitter $\sigma_{in,th}$. For small values of T_d, the threshold RMS input jitter $\sigma_{in,th}$ rises less than proportional with increasing delay.

Fig. 14 show that the theory accurately predicts the simulation results. Additionally, the CDR used in previous simulations (i.e. Fig. 9) is indicated on Fig. 14. This figure shows that the threshold RMS input jitter $\sigma_{in,th}$ is equal to 21 mrad. In practice, a RMS input jitter of 4 ps is not uncommon for a data rate of 10 Gb/s. This corresponds to 250 mrad, which is more than sufficient to avoid limit cycles in the discussed CDR. Fig. 14 shows that, in general, there is enough noise present to avoid limit cycles. Only in designs where limited input jitter is expected, the loop characteristics should be evaluated to ensure no unwanted or excessive limit cycles arise.

Note that Fig. 14 and the relations described above are very similar to Fig. 13 and the relations w.r.t. $A_{e,max}$. Intuitively, a limit cycle with a higher worst case amplitude $A_{e,max}$ will require more input jitter to quench the limit cycle and thus results in a higher threshold RMS input jitter $\sigma_{in,th}$.

VII. Further Analytical Approximations

While the previously developed theory matches excellently with the simulation results, it does not provide simple design intuition. This is because we still need to solve a system of equations, due to the interdependencies of σ_e, σ_{in}, σ_q, K_n, K_s and A_e, in order to find the results. To overcome this, analytical approximations are made in order to obtain closed form equations both for the worst case amplitude $A_{e,max}$ and the threshold RMS input jitter $\sigma_{in,th}$.

A. Worst case limit cycle amplitude $A_{e,max}$

As shown in Fig. 9, the worst case amplitude occurs for small values of the input noise level ($\sigma_{in} \to 0$). Unfortunately, this does not allow a direct simplification of the describing functions of Eqs. (11) and (12) because they depend on the noise level σ_e at the input of the non-linear block and not on the overall input noise level σ_{in}. According to Eq. (18), the noise level σ_e is a complex function of the describing functions, the input noise level σ_{in} and the standard deviation of the linearization error σ_q.

By taking the limit of Eq. (19) for small loop bandwidths, a spectacular simplification can be obtained: the contribution of the linearization error (i.e. σ_q) will be nearly entirely filtered out. Hence, in this case, the limit $\sigma_{in} \to 0$ corresponds to $\sigma_e \to 0$. Now, the Gaussian-plus-Sinusoid-Input Describing Function collapses to the Sinusoidal-Input Describing Function (SIDF), which equals [20]:

$$\lim_{\sigma_e \to 0} K_s(A_e, \sigma_e) = K_{SIDF}(A_{e,max}) = \frac{4\alpha}{\pi A_{e,max}} \tag{20}$$

According to the Barkhausen criterion (Eq. (14)), this gain K_s has to be equal to K_s^* for a limit cycle to occur. Hence, the oscillation frequency ω_s and K_s^* are described by the following relations:

$$\boxed{\frac{\pi}{2} = \text{atan}\left(\frac{\omega_s}{\omega_p}\right) + \omega_s T_d} \tag{21}$$

$$K_s^* = \frac{\omega_s}{\omega_0}\sqrt{1 + \left(\frac{\omega_s}{\omega_p}\right)^2} \tag{22}$$

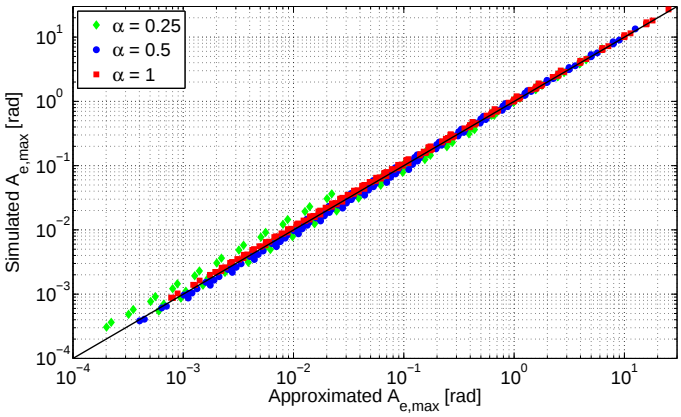

Fig. 15. Scatter plot of simulated $A_{e,max}$ as a function of the approximation according to Eq. (23) for different values of ω_0, ω_p, T_d and α.

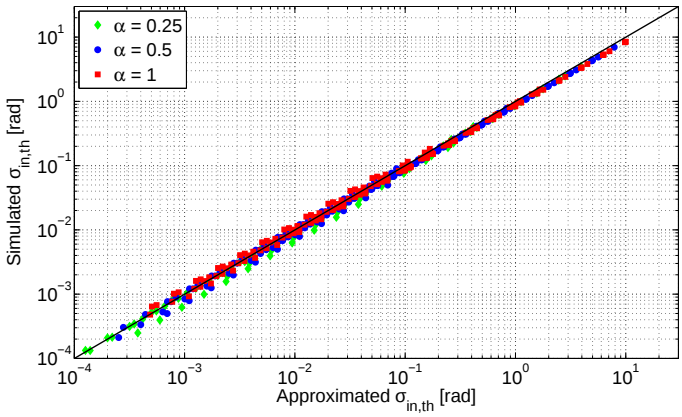

Fig. 16. Scatter plot of simulated $\sigma_{in,th}$ as a function of the approximation according to Eq. (27) for different values of ω_0, ω_p, T_d and α.

Eq. (21) defines the oscillation frequency ω_s implicitly and should be inverted to evaluate ω_s, but this is very simple. Note that K_s^* is fixed and only depends on ω_0, ω_p and T_d.

Substituting Eq. (22) in Eq. (20), yields the maximum amplitude of the limit cycle $A_{e,max}$:

$$\boxed{A_{e,max} \approx \frac{4\alpha}{\pi}\frac{\omega_0}{\omega_s}\frac{1}{\sqrt{1+\left(\frac{\omega_s}{\omega_p}\right)^2}}} \tag{23}$$

If the pole ω_p is at a sufficiently high frequency relative to ω_s, this equation can be further simplified:

$$A_{e,max} \approx \frac{4\alpha}{\pi}\frac{\omega_0}{\omega_s} \approx \frac{8\alpha}{\pi^2}\, T_d\, \omega_0 \tag{24}$$

From Eq. (23) and Eq. (24) it is clear that $A_{e,max}$ is proportional to ω_0 and that there is a linear relation between the T_d and $A_{e,max}$ (if ω_p is at a sufficiently high frequency). This corresponds well to the results of Section VI.

In order to determine the accuracy of the made approximations, a scatter plot is displayed in Fig. 15. This plot shows the approximation of $A_{e,max}$ (Eq. (23)) versus the simulation result of $A_{e,max}$ obtained from many simulation runs. Here, the values of ω_0, ω_p and T_d were varied over the same range as in Figs. 13 and 14. Also, three cases of the transition density α were considered. From this figure it is clear that the approximate expression matches the simulation very well.

B. Minimal input noise to quench a limit cycle

To find a simple approximation for the threshold RMS input jitter $\sigma_{in,th}$, we start from the observation that it corresponds to the case where the amplitude of the limit cycle A_e goes to zero. In this case, the GSIDF for the sinusoidal gain (Eq. (12)) reduces to:

$$K_s(A_e,\sigma_e)\big|_{\sigma_{in}=\sigma_{in,th}} = \lim_{A_e\to 0} K_s(A_e,\sigma_e) = \sqrt{\frac{2}{\pi}}\frac{\alpha}{\sigma_e} \tag{25}$$

Again, we face the problem that σ_e is a complex function of σ_{in}, K_n and σ_q. To overcome this, once more the limit of Eq. (19) for a small loop bandwidth is taken, which results in $\sigma_e \to \sigma_{in}$.

By combining this approximation and Eq. (25) with the Barkhausen criterion, we obtain an explicit equation for $\sigma_{in,th}$:

$$\sigma_{in,th} = \sqrt{\frac{2}{\pi}}\frac{\alpha}{K_s^*} \tag{26}$$

By combining Eq. (23) with Eq. (26), we can cast this in the following form:

$$\boxed{\sigma_{in,th} \approx \frac{1}{2}\sqrt{\frac{\pi}{2}}\, A_{e,max}} \tag{27}$$

which clearly indicates the relation between $A_{e,max}$ and $\sigma_{in,th}$. The equation provides, in combination with Eq. (21) and Eq. (23), a very simple way to assess the possibility of limit cycles in a BB-CDR.

Analogous to Fig. 15, Fig. 16 shows a scatter plot of the approximation of Eq. (27) versus the entire batch of simulation results. It is clear that there is a good matching between the analytical approximation and the simulations.

VIII. Conclusion

In this paper the influence of noise on the BB-CDR operation is investigated using describing function techniques. The results of this mathematical method were found to exhibit very good matching with time domain simulations.

In particular, the occurrence and the amplitude of a limit cycle is determined as a function of the input noise level. Our analysis allows to calculate the worst case amplitude of a limit cycle and to determine the minimal amount of noise necessary to avoid limit cycling as a function of the different CDR loop parameters. For this, the simple analytical approximations of Eqs. (21), (24) and (27) were found, which can be used for a fast assessment of the limit cycle sensitivity of a BB-CDR.

Based on our analysis, it appears that in most CDR systems, there is sufficient noise present to avoid limit cycling. Even in the case that the input jitter level is too small to avoid limit cycling, it is still likely that the amplitude of the limit cycle will be small enough to allow a correct data recovery operation. However, in this case the recovered clock will contain significant jitter peaking, which may be unacceptable. The most dangerous situation occurs when the CDR loop filter has a large delay and a high linear gain.

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