Noviello, Michele; Quintero, Andrés; Paton, Susana (2022). An Unbiased MEMS Capacitance-Controlled Oscillator as a Microphone for HMI Applications. *AUSTROCHIP 2022: 30th Austrian Workshop on Microelectronics, October 11th, Villach, Austria*, pp.: 57-60.

DOI: https://doi.org/10.1109/Austrochip56145.2022.9940675

An Unbiased MEMS Capacitance-Controlled Oscillator as a Microphone for HMI Applications

Michele Noviello
Electronic Technology Dept.
Carlos III University
Madrid, Spain
michele.noviello@ing.uc3m.es

Andres Quintero
Niccolò De Milleri
Andreas Wiesbauer
Infineon Technologies AG
Villach, Austria

Susana Paton
Electronic Technology Dept.
Carlos III University
Madrid, Spain
susana.paton@ing.uc3m.es

***Abstract*—MEMS microphones are usually DC biased with a voltage exceeding 10 V and a large resistance, requiring a charge pump and a high-ohmic link between the ASIC and the MEMS. This DC biasing is needed to obtain enough sensitivity for medium to high quality microphones. This manuscript investigates capacitance-controlled oscillators which allow to directly connect the MEMS sensor to the oscillator; this solution is prone to scaling. A new type of configuration (referred to as Cross-Connected Sensor) is presented and discussed. Its main advantage is the increase in the sensitivity and, when integrated in an ADC architecture, in the achievable SNR. The proposed solution is intended for Human-Machine Interface applications given their moderate SNR requirements.**

***Index Terms*—ADC, VCO-ADC, MEMS microphone, HMI, time-encoding**

I. Introduction

In the last years much research has been focused on Voltage-Controlled Oscillators (VCOs)-based ADCs, which have proved to be adequate to digitize signals coming from MEMS sensors (e.g. microphones). Among their advantages, the main one is the mostly digital nature, which relaxes the constraints related to power consumption and facilitates the scalability to deep sub-micron processes and the read-out electronics implementation [1]. MEMS microphone interface circuitry is usually based on the capacitance-to-voltage conversion. In order to achieve the required sensitivity, a large bias voltage (obtained by a charge pump) and a large bias resistor are needed [2]. The main drawbacks of this approach are clearly explained by [3]. The goal of this work is to analyze whether the combination of charge pump and VCO might be substituted with a MEMS Capacitance-Controlled Oscillator (MCCO) that directly reads the output signal of the MEMS microphone (i.e. capacitance signal) without any biasing circuitry. In general, the performance of open-loop VCO-based ADCs is bounded by the nonlinear voltage-to-frequency conversion accomplished through the VCO. To solve this issue, many authors moved to a closed-loop configuration where a high loop gain shrinks the VCO input signal span [4]. In case of MCCOs, the signal which controls the oscillator is very small and, therefore, the capacitance-to-frequency conversion can be represented with sufficient accuracy by a linear approximation. However, the sensitivity of grounded MEMS capacitance-controlled ring oscillators (cf. Part II-A) is not sufficiently high to detect small capacitance variations and to provide satisfactory SNR results. Our research has been focused on finding a way to increase the sensitivity of MCCOs without increasing chip cost and occupied area. Our strategy involves the connection of the sensor between two nodes of the ring oscillator (RO). This principle improves the capacitance-to-frequency sensitivity and, consequently, the estimated SNR. Although results are not sufficient to be an implementable solution in high-end audio acquisition applications, it might still be valuable for low-power applications demanding moderate SNR. Indeed, in Human-Machine Interface (HMI) applications prominently used in wearable electronics (i.e. voice detection and keyword recognition), a moderate SNR can be sufficient, while power budget and available chip area are critical. In Part II, RO-based MCCOs are described with an emphasis on the Grounded Sensor (GS) configuration compared with the proposed Cross Connected Sensor (CCS). In Part III, CCS configuration is modeled and explained; then, a design example is given and simulated at transistor-level. Conclusions are drawn in Part IV.

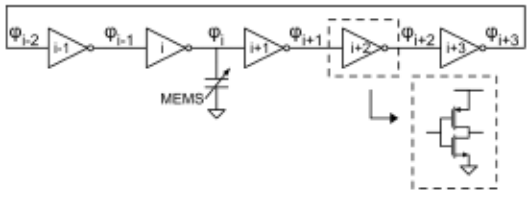
This project has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Sklodowska-Curie grant agreement No 956601

II. MEMS Capacitance-Controlled Oscillator

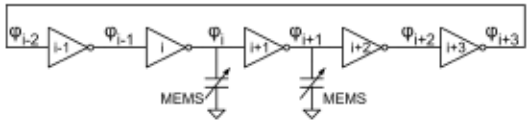
A. Grounded Sensor Configuration

Some authors have already studied the possibility to directly control an oscillator with a MEMS sensor [5]–[7]. Inter alia, ROs are relevant due to their great compatibility with CMOS processes and their ease of scalability. In this manuscript, each tap of the RO is intended as a single-ended CMOS inverter. In GS configuration, the MEMS sensor is connected as shown in Fig. 1(a). The MEMS capacitance C_{MEMS} modulates the propagation delay of just one of the RO taps. Consequently, the oscillation frequency f_{osc} is affected. Following the same approach of [8], it is possible to demonstrate that the oscillation frequency of the circuit in Fig. 1(a) can be approximated as:

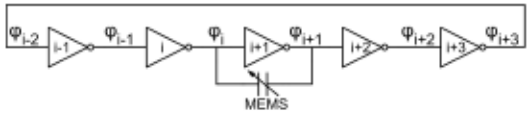
$$f_{\text{osc,1GS}} = \frac{I}{V_{\text{DD}}(C'_{\text{OX}}WLN + C_{\text{MEMS}})} \tag{1}$$



(a) *One grounded sensor*



(b) *Two grounded sensors*



(c) *Cross-connected sensor*

Fig. 1: Different connections of the capacitive sensor to the RO.

where C'_{OX} is the gate capacitance per unit area, V_{DD} the supply voltage, W, L and N are respectively the gate width, the gate length and the number of taps. Current I is the MOSFET drain current which flows during the propagation delay. Assuming that during most of it one of the two transistors is in saturation region, it results that $I \approx \frac{\mu C_{OX}'}{2}\frac{W}{L}(V_{DD}-V_T)^2$ being μ the carrier mobility and V_T the threshold voltage. Equation (1) provides interesting insights on the circuit:

- Oscillation frequency is inversely proportional to the sum of all the load capacitors connected to the RO.
- Many taps or big gate capacitors (compared to C_{MEMS}) reduce the sensitivity to the MEMS capacitance.
- The term $I \cdot (V_{DD}C'_{OX}WLN)^{-1}$ approximates the oscillation frequency if the MEMS capacitor is removed. The insertion of MEMS capacitance can be represented by the term $\left(1+\frac{C_{MEMS}}{C'_{OX}WLN}\right)^{-1}$.

The MCCO sensitivity can be derived from (1) as:

$$k_{1GS} = \frac{\partial f_{osc}}{\partial C_{MEMS}} = -\frac{I}{V_{DD}(C'_{OX}WLN + C_{MEMS})^2} \quad (2)$$

The sensitivity is not constant and depends on the MEMS capacitance, but sound-induced variation is so small that we can just compute sensitivity at the rest value of the MEMS capacitor. The sensor should be dominant over the other load capacitors in the circuit but, at the same time, the total amount of capacitors in the RO should permit a sufficient oscillation frequency and sensitivity to reach the targeted SQNR performance. If more than one grounded sensor is used, sensitivity increases and oscillation frequency decreases; in case of two MEMS sensors (Fig. 1(b)), one obtains:

$$f_{osc,2GS} = \frac{I}{V_{DD}(C'_{OX}WLN + 2C_{MEMS})} \quad (3)$$

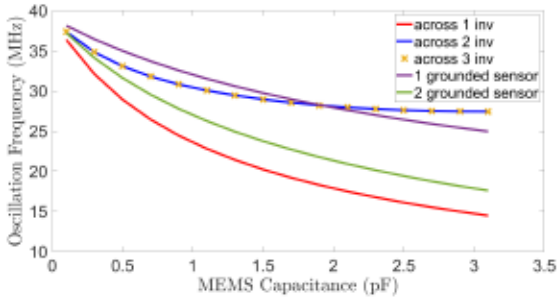


Fig. 2: Oscillation frequency against MEMS capacitance in GS and CCS cases (simulation at transistor-level).

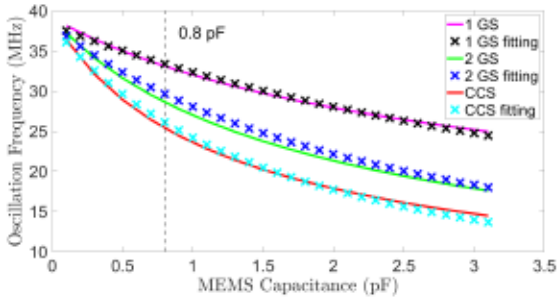


Fig. 3: Comparison between analytical formulae and simulation results.

$$k_{2GS} = -\frac{2I}{V_{DD}(C'_{OX}WLN + 2C_{MEMS})^2} \quad (4)$$

Equations (3) and (4) reveal that the oscillation frequency is equivalent to (1) with double MEMS capacitance; instead, sensitivity is twice the value that would have been obtained if doubling the value of one MEMS capacitance. However, adding more MEMS sensors makes the chip bulkier and more expensive. It is of interest to boost as much as possible the sensitivity considering only one MEMS sensor.

B. Cross-Connected Sensor Configuration

The connection of the sensor between two phases of the RO (cf. Fig. 1(c)) increases the MCCO sensitivity. As shown in Fig. 2, adjacent phases should be chosen to have an improvement. In this way, the sensitivity to the MEMS capacitance is even more than using two different grounded sensors. The working principle behind this is explained in Part III. So far, let us model the CCS capacitance as an equivalent number β of grounded capacitors. This leads to:

$$f_{osc,CCS} = \frac{I}{V_{DD}(C'_{OX}WLN + \beta C_{MEMS})} \quad (5)$$

$$k_{CCS} = -\frac{\beta I}{V_{DD}(C'_{OX}WLN + \beta C_{MEMS})^2} \quad (6)$$

This approximation permits a good fitting of the simulation results, which derive from transistor-level models of the circuit. This is shown in Fig. 3 for the three considered cases. In Fig. 4, the different sensitivity formulae defined by (2), (4) and (6) are plotted in absolute value. The CCS case provides the best sensitivity by using just one MEMS sensor.

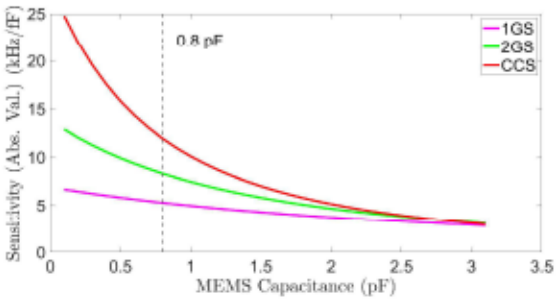


Fig. 4: Absolute value of sensitivity against MEMS capacitance; plots are obtained thanks to analytical formulae.

III. CCS Working Principle

In [9], the influence of a capacitor connected between the input and the output node of a CMOS inverter is analysed. Our aim is to better understand why this effect may be beneficial for the sensitivity and to further detail the working principle with time-dependent subcircuits. The most relevant subcircuits are depicted in Fig. 5; time-domain waveforms representing the phases ϕ_i (i.e. input) and ϕ_{i+1} (i.e. output) are reported in Fig. 6. For the sake of clarity, the i-th NMOS and PMOS are the transistor with the drain connected to the i-th node. Let us analyse the case of a rising edge at the input. At the beginning, the only transistors switched on are the i-th and i+1-th PMOSETs (cf. Fig. 5(a)). CCS capacitance (which is initially pre-charged but with the opposite polarity) forces some current to flow into the output node and this charges the i+1-th load capacitor above the power supply level. As a result, source and drain terminals of the i+1-th PMOS are reversed. This effect (dependent on the cross connected capacitance) creates a pre-shoot on the output voltage waveform and contributes to the oscillation frequency modification. At the same time, input signal faces its own transition with a slope mainly determined by i-th load capacitor. When the input voltage level reaches the NMOS threshold voltage, the i+1-th NMOS turns on in saturation region (cf. Fig. 5(b)). The output voltage starts discharging and the i+1-th PMOS slowly turns off. Short-circuit current is prevented in this way [9]. As soon as subcircuit (b) is valid, the input signal dramatically slows down its growth (cf. Fig. 6); this is due to the Miller effect created by the CCS capacitance and the NMOS in saturation region. This happens after that the input voltage has already crossed the fifty percent of the full scale range; therefore, MEMS influence on the propagation delay of i-th inverter is negligible. Subcircuit (c) starts when the PMOS is turned-off; if the input voltage is approximated as constant, a constant current charges the MEMS capacitor and slows down the output falling edge; in fact, it reduces the discharging current of the i+1-th load capacitance. When the transition is almost over, the NMOS reaches the triode region, as shown in subcircuit (d) and the input signal increase speeds up. If an input falling edge is considered, there is no Miller effect due to the subcircuit topology (cf. subcircuit (e)); as shown in Fig. 6, input falling transition is completed during the pre-shoot on the output voltage. The almost constant current given by the i+1-th PMOS in saturation region will charge the output load capacitance and reverse the voltage polarity across the MEMS capacitance compared to the beginning of the transition. The current flowing into the MEMS reduces the charging rate of the output capacitance. The propagation delay of the i+1-th inverter is strongly related to the MEMS capacitance because of the pre-shoot and the reduced slope of ϕ_{i+1} transitions. The MEMS capacitor introduced in the RO is subject to a charge from $-V_{DD}$ to V_{DD} in the first half of the input switching period and a discharge from V_{DD} to $-V_{DD}$ in the second part (cf. Fig. 6). Overall, it can be assumed that the MEMS sensor is DC unbiased being the average voltage across it equal to zero. Sound pressure is transformed into a frequency modulated signal and can be demodulated and digitized with the help of some counters and auxiliary logic. In order to estimate the current consumption one can add the contribution due to the charge and the discharge of the MEMS capacitor. If we reduce the model to subcircuits (c) and (d) and assume that in each of the two cases the initial charge is fully dissipated and then recharged with the opposite polarity, the average current consumption results in:

$$i_{avg} = f_{osc} V_{DD} \left[C'_{OX} L N (W_n + W_p) + 4 C_{MEMS} \right] \qquad (7)$$

where the oscillation frequency is itself dependent on the MEMS capacitance. Equation (7) is likely to overestimate the average current since a relevant part of the charge and discharge of the CCS capacitor happens during the pre-shoot, where the current consumption is supposed to be reduced. As a design example, a five-stage RO has been simulated in a 130nm CMOS technology node with the following transistor sizes: $L_n = L_p = 2\,\mu m$, $W_n = 15\,\mu m$ and $W_p = 30\,\mu m$. The implemented model for the MEMS sensor including the electrical parasitic elements is shown in Fig. 7(a): it is composed by a nominal MEMS capacitance C_{MEMS}, a series resistance R_s and two parasitic capacitors C_{p1} and C_{p2} between each of the two terminals and the substrate of the MEMS. Since one of the two parasitic capacitors is supposed to be very big (e.g. C_{p2} in the schematic), even bigger than the MEMS capacitor itself, our strategy is to short it out by connecting the MEMS substrate to one of the RO phases (i.e. ϕ_{i+1}). Therefore, the other parasitic capacitor (i.e. C_{p1}) is also connected across a RO tap and will introduce a penalty in the sensitivity and the oscillation frequency. In our simulations we assume that $C_{MEMS} = 0.8\,pF$ (rest value), $R_s = 2\,k\Omega$ and $C_{p1} = 150\,fF$. Resulting average current consumption is slightly affected by the parasitic elements; regardless of their presence, i_{avg} is around $83\,\mu A$ with V_{DD} equal to $1V$. In Table I, the main results are reported. The A-weighted SNR computation relates the input signal (assumed as a sinusoidal MEMS capacitance variation whose amplitude is $9\,fF$ at $1\,kHz$) to the input referred phase noise [10]. Instead, as for the quantization noise, a system-model has been created and all the RO phases are processed by counters and then summed to increase the effective oscillation frequency [11]. Counters are reset at the sampling frequency of $2.75\,MHz$.

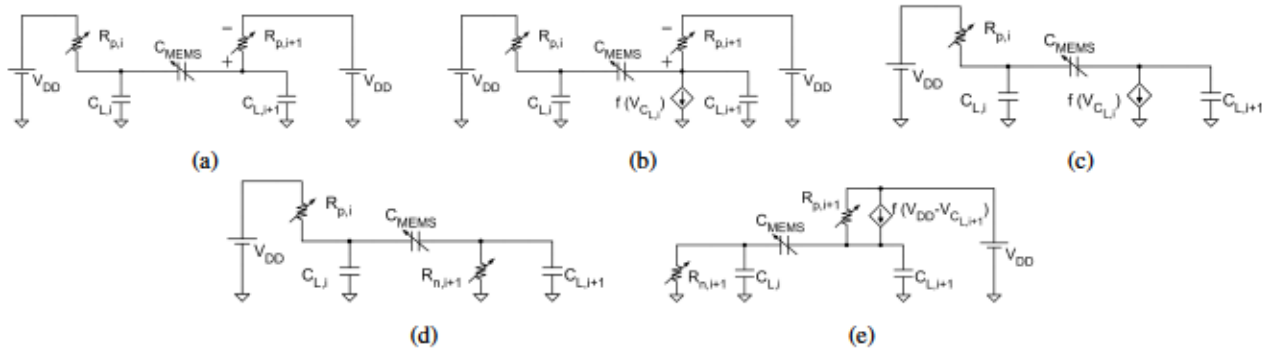


Fig. 5: Subcircuits during commutations; (a), (b), (c) and (d) represent the input rising edge; (e) belongs to the falling edge.

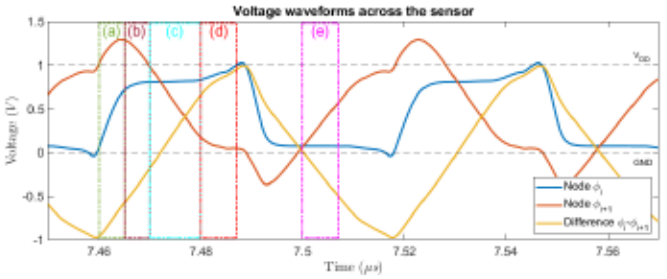
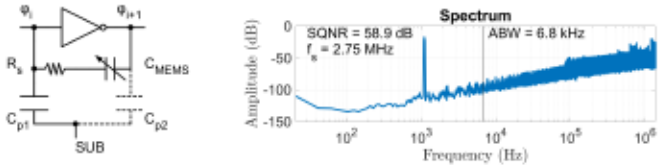


Fig. 6: Time-domain waveforms related to phases ϕ_i, ϕ_{i+1} and the differential voltage across the sensor. Each rectangle is associated to a subcircuit shown in Fig. 5.



(a) *Parasitic model of the MEMS sensor* (b) *Amplitude spectrum of a digitized sinewave*

Fig. 7: Parasitic model and SQNR computation.

Assumed analog bandwidth (ABW) is 6.8 kHz. Resulting first-order noise-shaped amplitude spectrum is shown in Figure 7(b) and resulting SQNR is estimated as 58.9 dB.

IV. Conclusion

The results show that CCS configuration overcomes the performance of GS architecture. The sensitivity is actually improved. Moreover, the analysis of CCS configuration working principle can be easily generalized to all the capacitors connected between the input and the output of a CMOS inverter (e.g. gate-drain capacitance). Previous analyses modeled them with the Miller equivalent by assuming that the gain of the stage is equal to -1. In this manuscript, there is a deeper insight on the time-dependency of the Miller effect and its consequences on the input and output waveform. Concerning to the shown design example, a good power consumption has been reached and the SNR estimate of the MCCO-based ADC confirms that this idea can be considered in case of low or moderate SNR requirements.

TABLE I: Design example results.

Parasitic Elements	Results		
	f_o	k_{CCS}	$SNR_{A\text{-}w}$
no	17.1 MHz	9.8 kHz fF^{-1}	55.6 dBA
yes	15.8 MHz	8.1 kHz fF^{-1}	54.4 dBA

References

[1] Watanabe, T. (2021). All-digital VCO-ADC TAD confirming scaling and stochastic effects using 16-nm FinFET CMOS. In 2021 28th IEEE International Conference on Electronics, Circuits, and Systems (ICECS) (pp. 1-4). IEEE.

[2] Sant, L., Bach, E., Gaggl, R., & Baschirotto, A. (2019, October). A current-feedback amplifier with programmable gain for MEMS microphone read-out circuits. In 2019 Austrochip Workshop on Microelectronics (Austrochip) (pp. 1-5). IEEE.

[3] Ersoy, S., Van Veldhoven, R. H., Sebastiano, F., Reimann, K., & Makinwa, K. A. (2013, February). A 0.25 mm 2 AC-biased MEMS microphone interface with 58dBA SNR. In 2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers (pp. 382-383). IEEE.

[4] Sacco, E., Vergauwen, J., & Gielen, G. (2019, June). From open-loop to closed-loop single-vco-based sensor-to-digital converter architectures: Theoretical analysis and comparison. In 2019 IEEE 8th International Workshop on Advances in Sensors and Interfaces (IWASI) (pp. 29-34). IEEE.

[5] A. Quintero, F. Cardes, L. Hernandez, C. Buffa and A. Wiesbauer, "A Capacitance-to-Digital Converter Based on a Ring Oscillator with Flicker Noise Reduction," 2016 Austrochip Workshop on Microelectronics (Austrochip), 2016, pp. 40-44, doi: 10.1109/Austrochip.2016.019.

[6] Van Rethy, J., & Gielen, G. (2013, November). An energy-efficient capacitance-controlled oscillator-based sensor interface for MEMS sensors. In 2013 IEEE Asian Solid-State Circuits Conference (A-SSCC) (pp. 405-408). IEEE.

[7] Van Rethy, J., & Gielen, G. (2012). Capacitance-controlled oscillator with enhanced tuning range using negative capacitance for time-based sensor interfaces. Procedia Engineering, 47, 21-24.

[8] Abidi, A. A. (2006). Phase noise and jitter in CMOS ring oscillators. IEEE journal of solid-state circuits, 41(8), 1803-1816.

[9] Brzozowski, I., & Kos, A. (2012, September). The miller effect in digital cmos gates and power consumption analysis. In 2012 International Conference on Signals and Electronic Systems (ICSES) (pp. 1-6). IEEE.

[10] Cardes, F., Quintero, A., Gutierrez, E., Buffa, C., Wiesbauer, A., & Hernandez, L. (2018). SNDR limits of oscillator-based sensor readout circuits. Sensors, 18(2), 445.

[11] Kim, J., Jang, T. K., Yoon, Y. G., & Cho, S. (2009). Analysis and design of voltage-controlled oscillator based analog-to-digital converter. IEEE Transactions on Circuits and Systems I: Regular Papers, 57(1), 18-30.