A Boost PFC Converter With Programmable Harmonic Resistance

Koen De Gussemé, *Member, IEEE*, Wouter R. Ryckaert, *Member, IEEE*, David M. Van de Sype, *Member, IEEE*, Jozef A. Ghijselen, *Member, IEEE*, Jan A. Melkebeek, *Senior Member, IEEE*, and Lieven Vandevelde, *Member, IEEE*

***Abstract*—Power factor correction (PFC) converters with low harmonic input resistance are desirable loads to support the reduction of the harmonic distortion on the feeding grid. Therefore, a novel control strategy is proposed. Whereas previously proposed controllers tried to obtain a resistive behavior of the converter with a constant input impedance for all frequencies, including the fundamental, the proposed control strategy allows to set a harmonic input resistance which is independent of the input power level of the converter. Consequently, the harmonic input resistance remains low, even when the input power of the converter is decreased, which adds to the stability of the feeding grid. This paper describes the operation of a digitally controlled boost PFC converter with the new control algorithm. Experimental tests on a 1-kW prototype show that a practical realization of the algorithm is possible and that a programmable harmonic input resistance of the converter is obtained. The converter contributes to the damping in the power system, which is an important feature to mitigate harmonic voltage distortion due to resonances. The damping potential of the converter with the proposed control strategy is demonstrated on a scale model of a distribution system with a parallel resonance.**

***Index Terms*—AC–DC power conversion, digital control, harmonic distortion, power quality.**

I. Introduction

In order to comply with the international standards for electromagnetic compatibility, capacitive diode bridge rectifiers are often replaced by power factor correction (PFC) converters. These PFC converters provide a constant output voltage while their input current waveform is shaped to comply with the standards. Several approaches are in use nowadays, depending on the application type, the cost of implementation, and the required input power. For low power applications, several converter types such as fly-back, Ćuk, SEPIC, and boost that are operating in the discontinuous conduction mode (DCM) are employed [1]–[3]. After all, these converters behave more or less resistive at their input when operated in the DCM. Consequently, only one control loop is required for these PFC converters. Although the power factor of such converters is not unity their input current wave shape meets the standards in most cases.

For applications requiring a higher input power, device stresses and problems with conducted emission limit the use of these DCM converters. Therefore, PFC converters operated in the continuous conduction mode (CCM) are employed [4]–[8]. In these applications, an input current controller is applied in order to obtain either a sinusoidal line current, independent of the line voltage distortion, or a resistive line current behavior. Although both approaches guarantee a high power factor at the input of the converter, their reaction on harmonic components of the grid voltage will be different. Since the converter with resistive behavior contributes to the damping of grid oscillations, the use of converters with a resistive input impedance behavior is more preferable than the sinusoidal approach.

In some recent papers in the field of power quality [9]–[12], a shunt harmonic impedance (SHI) is proposed as a central damper for grid resonances [13]. This is a converter designed to behave as a resistor for harmonics and as an open chain for the fundamental component of the grid voltage. Since such a damper leads to a low grid impedance for harmonics, the propagation of harmonic currents through the grid is mitigated. This attenuation of grid resonances can also be achieved by implementing the resistive input behavior as a secondary control function [9], [14] on all grid-coupled converters. Therefore, a load with such resistive behavior for harmonics is preferable. However, many rectifier loads with a sinusoidal input current behave as an infinite impedance or as a capacitor for harmonics, so there is no contribution to the reduction of grid voltage distortion (damping of resonances) [15]. Converters with a resistive input current control strategy do behave as a resistor, as desired.

For most recently proposed converters with resistive input, this input impedance is equal for both the fundamental component and the harmonics. As a result, the harmonic input impedance of these converters changes with the input power of the converter. Therefore, a new control strategy for a boost PFC converter has been developed in order to have a programmable resistive input impedance for harmonics, which is independent of the fundamental component of the input current, and thus

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K. De Gussemé, J. A. Melkebeek, and L. Vandevelde are with the Electrical Energy Laboratory, Department of Electrical Energy, Systems and Automation, Faculty of Engineering, Ghent University, 9000 Ghent, Belgium (e-mail: degusseme@eesa.UGent.be; Jan.Melkebeek@UGent.be; Lieven.Vandevelde@UGent.be).

W. R. Ryckaert is with the Department of Industrial Sciences, Laboratorium voor Lichttechnologie, Katholieke Hogeschool Sint-Lieven, 9000 Ghent, Belgium (e-mail: Wouter.Ryckaert@kahosl.be).

D. M. Van de Sype and J. A. Ghijselen are with Inverto N.V., 9940 Evergem, Belgium (e-mail: David.Van.de.Sype@inverto.be; Josef. Ghijselen@inverto.be).

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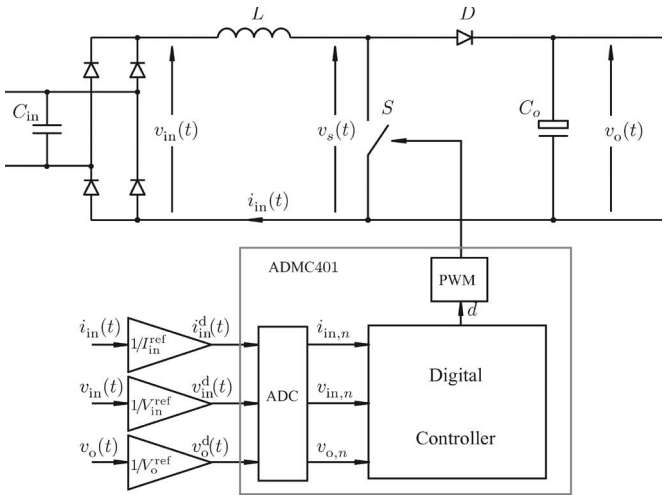

Fig. 1. Typical boost PFC converter with digital controller.

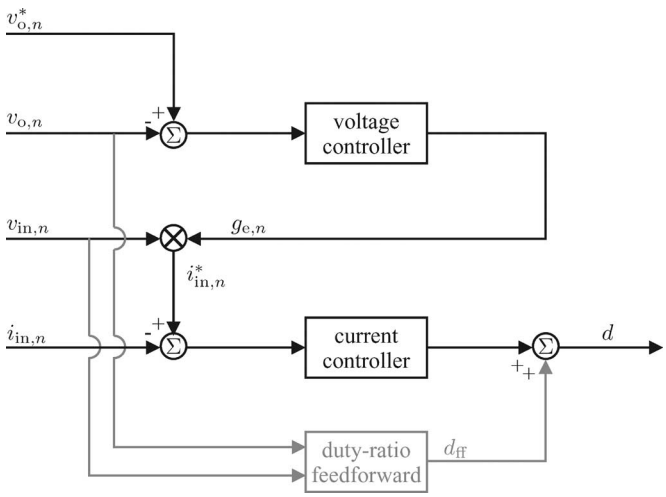

Fig. 2. Black: Typical two-loop control scheme for a boost PFC converter. Gray: Duty-ratio feedforward.

of the power level of the converter. As a result, the converter will keep its potential to damp grid oscillations, even for a low input power of the converter. The algorithm is based upon duty-ratio feedforward, which is a control strategy previously employed to obtain a resistive input behavior for a boost PFC converter [8], [16]. The operation of the converter with a programmable harmonic resistance is experimentally validated, together with the damping potential for harmonic resonances on the grid.

II. Digital Control of Boost PFC Converters

The topology of a boost PFC converter is depicted in Fig. 1. The converter consists of an input filter, a diode bridge, and a boost dc–dc converter containing a switch S, a diode D, an input inductor L, and an output capacitor C. In order to digitally control both the input current and the output voltage, the inductor current $i_{\rm in}(t)$, the input voltage $v_{\rm in}(t)$, and the output voltage $v_{\rm o}(t)$ must be sensed, scaled, and sampled. This way, these control variables are converted into their dimensionless digital samples $i_{{\rm in},n}$, $v_{{\rm in},n}$, and $v_{{\rm o},n}$, respectively. This conversion can be described as a division by a reference value $(I_{\rm in}^{\rm ref}, V_{\rm in}^{\rm ref}, V_{\rm o}^{\rm ref})$, followed by a sampling process [8].

A typical controller for a boost PFC converter with resistive control strategy consists of two control loops, as shown in Fig. 2 (black lines), namely: 1) an input current control loop, which is usually a fast loop, and 2) an output voltage control loop, which is much slower than the current control loop. The output voltage controller balances the input and the output powers of the converter to obtain a constant output capacitor voltage by changing the desired (dimensionless) input conductance $g_{{\rm e},n}$ of the converter. The product of this input conductance and the input voltage of the converter yields the desired input current $i_{{\rm in},n}^*$ of the converter. The input current controller commands the pulsewidth modulation unit which controls the switch S. In many cases, both controllers are implemented as proportional–integrating (PI) controllers.

In [8], a new control strategy for the current control loop was proposed to improve the resistive behavior of the converter. The

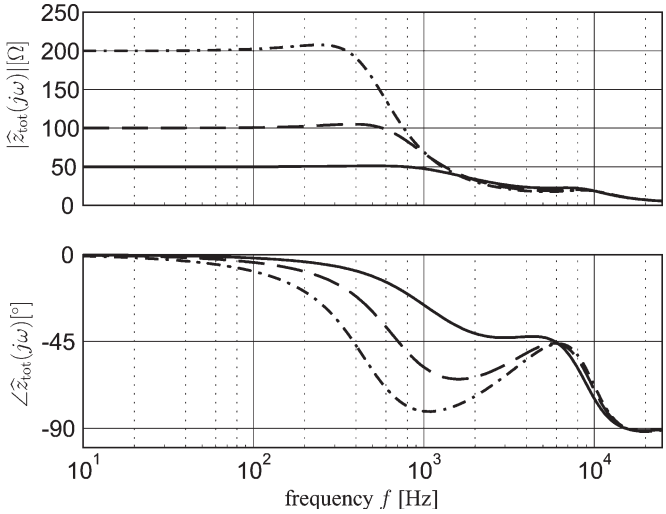

Fig. 3. Small-signal input impedance of a boost PFC converter with duty-ratio feedforward.

control scheme is shown in Fig. 2 (gray lines). The ideal steady-state duty ratio is calculated by using the sampled values of the input and the output voltage, i.e.,

$$d_{\rm ff} = 1 - \frac{v_{\rm in}}{v_{\rm o}} = 1 - \frac{v_{{\rm in},n} V_{\rm in}^{\rm ref}}{v_{{\rm o},n} V_{\rm o}^{\rm ref}}. \tag{1}$$

This steady-state duty ratio $d_{\rm ff}$ is added to the output of the input current controller. As a result, the input current tracking is improved and the frequency range for which the converter behaves resistively is extended to higher frequencies.

In order to quantify the improvements, the small-signal input impedance of a boost PFC converter with duty-ratio feedforward was calculated in [8]. The resulting input impedance of the converter for the different values of the desired input impedance is displayed in Fig. 3. This figure shows that the converter with feedforward has the following resistive harmonic impedance:

$$Z_{{\rm in},h} = \frac{1}{g_{\rm e}} = \frac{Z_{\rm in}^{\rm ref}}{g_{{\rm e},n}}, \qquad \text{with } Z_{\rm in}^{\rm ref} = \frac{V_{\rm in}^{\rm ref}}{I_{\rm in}^{\rm ref}} \tag{2}$$

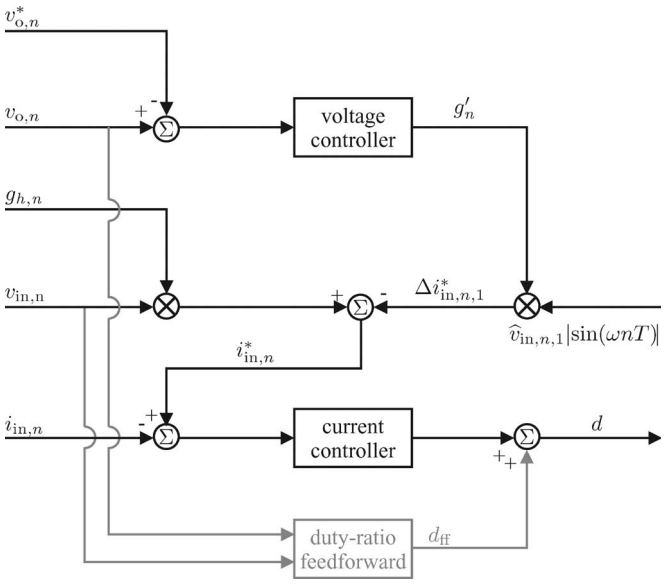

Fig. 4. Control strategy for a programmable harmonic input conductance.

for a frequency range dependent on the programmed value of the input conductance g_e, which determines the input power of the converter. Hence, a resistive impedance can be achieved with this algorithm for frequencies up to 1 kHz (full black lines in Fig. 3). For higher frequencies, the converter will behave as a parallel connection of a resistor and a capacitor, due to the capacitance of the electromagnetic interference filter C_{in}.

When this control strategy is applied, the input conductance g_h for harmonics always remains equal to the input conductance g_1 of the fundamental ($g_h = g_1 = g_e$). Consequently, the input conductance of the harmonics decreases for lower power levels, together with the damping potential of the converter. Moreover, for lower values of the desired input conductance, the influence of the input capacitance of the converter will gain significance (dashed and dash–dotted curves in Fig. 3) and the frequency range for which the resistive behavior is obtained becomes limited to the low-order harmonics [$<$ 300 Hz for $g_e < (1/200\ \Omega)$].

III. Control Strategy for a Programmable Harmonic Resistance

A. General Operation of the Control Strategy

Since the most desirable behavior is achieved with high values of the input conductance (Fig. 3), a converter with a pronounced damping of harmonic resonances should have a high constant harmonic input conductance g_h for the entire power range. Therefore, the output voltage controller should only change the input conductance g_1 of the fundamental to balance the input and output power, and leave the harmonic input conductance g_h unaffected. Such a control strategy is depicted in Fig. 4. The input conductance for harmonics is now an external input g_h and can be programmed to be a constant. In order to change only the input conductance of the fundamental component, the output of the output voltage controller g' is multiplied with the fundamental component of the line voltage. The result is used to adjust the desired value of the input current

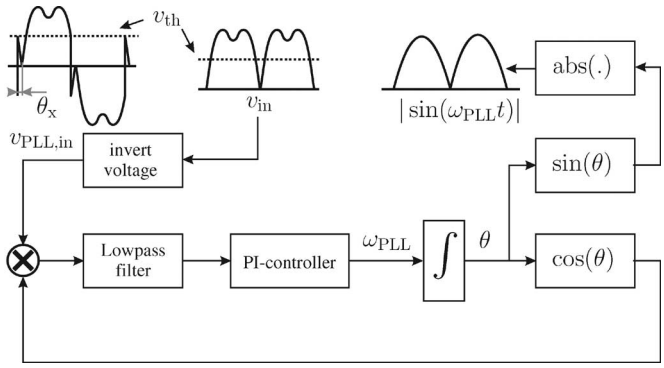

Fig. 5. Block diagram of the PLL.

$i^*_{in,n}$. The input conductance of the fundamental can now be calculated as $g_1 = g_h - g'$. Hence, the input conductance of the fundamental can be changed independently of the input conductance for the harmonics to vary the power level of the converter.

As the boost PFC converter is only capable of transferring energy from the mains to the load, the range of input conductances must be positive. Moreover, when $g_{1,n}$ and $g_{h,n}$, defined as

$$g_{1,n} = g_1 Z^{ref}_{in} \quad g_{h,n} = g_h Z^{ref}_{in} \tag{3}$$

are dimensionless digital quantities, they are restricted to values less than 1. Consequently, the following input conductances g_1 and g_h are limited to

$$0 < g_1 < \frac{1}{Z^{ref}_{in}} \quad 0 < g_h < \frac{1}{Z^{ref}_{in}}. \tag{4}$$

Therefore, the highest harmonic input conductance g_h, which can be achieved and which also corresponds to the best damping of grid resonances, is $(Z^{ref}_{in})^{-1}$. When g_h is set to zero, a sinusoidal input current is obtained, independently of the input power of the converter, which is determined by g_1.

B. Phase-Locked Loop (PLL)

In order to obtain the required fundamental component of the line voltage, a PLL is employed. The block diagram of this loop is displayed in Fig. 5. The method to obtain the fundamental component of the input signal uses very common components such as a low-pass filter and a PI controller. Nevertheless, as input of the PLL, the line voltage is reconstructed by inverting the input voltage (at the dc side of the diode bridge) during half of each line period. This way, an alternating signal is obtained as input of the PLL without the need to measure the line voltage at the ac side of the diode bridge. In the ideal case, the input voltage should be inverted each time the line voltage reaches zero to obtain the line voltage. However, since in real converters the input voltage does not reach zero, the detection of these zeros is very hard to accomplish. Therefore, the waveform is inverted when a predefined threshold voltage v_{th} is crossed. Although this introduces some distortion in the input waveform of the PLL, the sinusoidal waveform obtained at the output of the PLL will be nearly in phase with the

fundamental component of the line voltage. The phase error can be easily calculated for a sinusoidal line voltage $\widehat{v}_{\rm in}\sin(\omega t)$. The input of the PLL $v_{\rm PLL,in}$ can be expressed as

$$\begin{cases} v_{\rm PLL,in} = \widehat{v}_{\rm in}\sin(\omega t), & \omega t \in [0, \pi - \theta_{\rm x}] \cup [\pi, 2\pi - \theta_{\rm x}] \\ v_{\rm PLL,in} = -\widehat{v}_{\rm in}\sin(\omega t), & \omega t \in [\pi - \theta_{\rm x}, \pi] \cup [2\pi - \theta_{\rm x}, 2\pi] \end{cases} \tag{5}$$

where $\theta_{\rm x}$ is the phase shift between the effective switching point and the ideal switching point, which is the zero of the line voltage (Fig. 5). The fundamental component of this waveform can be obtained with a Fourier analysis, yielding the following:

$$\begin{cases} v_{\rm PLL,in,1} = A_1\sin(\omega t) + B_1\cos\omega t \\ A_1 = \widehat{v}_{\rm in}\left\{1 - \frac{2\theta_{\rm x}}{\pi} + \frac{\sin(2\theta_{\rm x})}{\pi}\right\} \\ B_1 = \widehat{v}_{\rm in}\left\{\frac{1}{\pi} - \frac{\cos(2\theta_{\rm x})}{\pi}\right\}. \end{cases} \tag{6}$$

For small values of $\theta_{\rm x}$, where $\sin(2\theta_{\rm x}) \approx 2\theta_{\rm x}$ and $\cos(2\theta_{\rm x}) \approx 1$, the aforementioned equations simplify to $A_1 = \widehat{v}_{\rm in}$ and $B_1 = 0$, so the fundamental component of $v_{\rm PLL,in}$ will be equal to the line voltage $\widehat{v}_{\rm in}\sin(\omega t)$. If the angle $\theta_{\rm x}$ becomes significant, the phase shift ψ between the fundamental component of the line voltage and the output of the PLL becomes visible. It can be estimated with the following:

$$\tan\psi = \frac{B_1}{A_1}. \tag{7}$$

When the amplitude of the fundamental component of the line voltage is, e.g., $\sqrt{2}\cdot 230$ V, the implementation of a threshold voltage of 50 V results in an error $\theta_{\rm x} = 8.8^\circ$ in the detection of the zero of the line voltage. Evaluation of (7) learns that, in this case, the phase shift between the fundamental component of the line voltage and the fundamental component of the input of the PLL is less than 1°. This means that a safe threshold voltage can be chosen which guarantees a low phase shift ψ and ensures good detection of the zero of the line voltage. As a result, if the parameters of the low-pass filter and the PI controller of the PLL are tuned well, the estimated waveform of the PLL will be very close to the fundamental of the line voltage. The presence of significant harmonics on the line voltage may lead to some extra phase shift. Moreover, measures must be taken to prevent multiple inversions of the input voltage, since harmonics can cause multiple crossings of the threshold. A simple solution is to disable the detection as long as the input voltage remains lower than another (higher) threshold. When such measures are taken and no multiple inversions occur, this algorithm is hardly disturbed by harmonics. When the harmonic content of the voltage is low, other PLL strategies are possible, such as the method proposed in [17].

C. Operation in the DCM

The objective of the proposed control strategy is to obtain a resistive behavior of the converter for harmonics, which is independent of the input power of the converter. Nevertheless, when the input power of the converter is decreased, this converter may start to operate in the mixed conduction mode (MCM), which is a combination of DCM near the zero-crossings and CCM in the remainder of the line period, whereas the duty-feedforward algorithm in Section II was only intended for operation in CCM. As a result, the extension of this digital control algorithm for operation in MCM must be used [7]. This extension includes the correction of the input current samples by a factor κ, given by

$$\kappa(t) = \frac{dv_{\rm o}(t)}{v_{\rm o}(t) - v_{\rm in}(t)}. \tag{8}$$

With this extension, the line current distortion can be significantly reduced. Nevertheless, some distortion will exist, due to the changing dynamics of the converter in the DCM.

When the input power of the converter is low, another problem yielding line current distortion may arise. The amplitude of the fundamental component of the reference current is low, whereas the harmonic components (which are independent of the input power) are large, leading to negative values of the input current reference. However, due to the diode bridge at the input of the converter, the inductor current cannot become negative and it will be clamped to zero during the periods where the desired input current is negative. As a result, the input impedance of the converter for harmonics may display some undesirable variations when the input power of the converter is low and the voltage distortion is high.

IV. Experimental Results

A. Test Setup

For the experimental verification of the control algorithm, a 1-kW boost PFC converter is employed. The converter has an input capacitor of 470 nF, an inductor of 1 mH, and an output capacitor of 470 μF. The switches are MOSFET SPP20N60S5 and diode RURP3060. The converter is supplied from a linear amplifier (PAS1000 of Spitzenberger & Spies). Under normal operating conditions, the line voltage is 230 V, 50 Hz, whereas the output voltage is programmed to be 400 V. The reference values of the control variables are

$$\begin{cases} V_{\rm in}^{\rm ref} = 399\ {\rm V}, & V_{\rm o}^{\rm ref} = 452\ {\rm V} \\ I_{\rm in}^{\rm ref} = 10.4\ {\rm A}, & Z_{\rm in}^{\rm ref} = \frac{V_{\rm in}^{\rm ref}}{I_{\rm in}^{\rm ref}} = 38.4\ \Omega. \end{cases} \tag{9}$$

The converter is controlled by the ADMC401 digital signal processor of Analog Devices. The sampling of the input current and input voltage is synchronized with the switching of the converter, at 50 kHz, whereas the sampling of the output voltage is performed at 1 kHz.

B. PLL

The locking of the PLL is shown in Fig. 6. Although the output of the PLL is generated each switching cycle, the calculations required for the locking of the PLL are performed once every 0.2 ms which explains the quantization that can be observed in the lower trace in Fig. 6. The input voltage of the converter (at the dc side of the diode bridge) is displayed in the center trace. For this experiment, a line voltage waveform

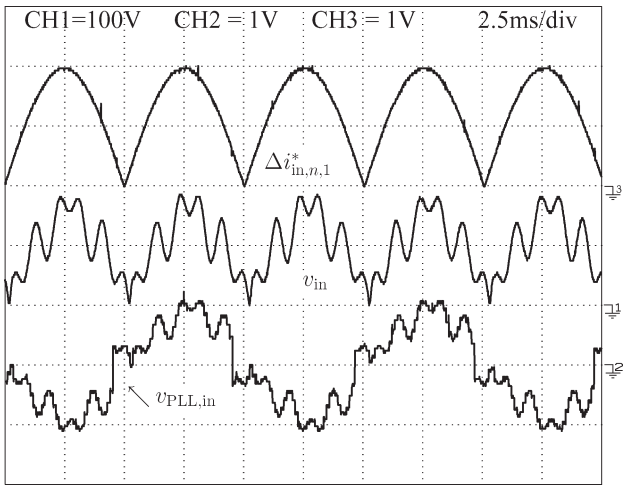

Fig. 6. Upper trace: Output of the PLL. Center trace: Input voltage of the converter. Lower trace: Flipped input voltage used as input for the PLL.

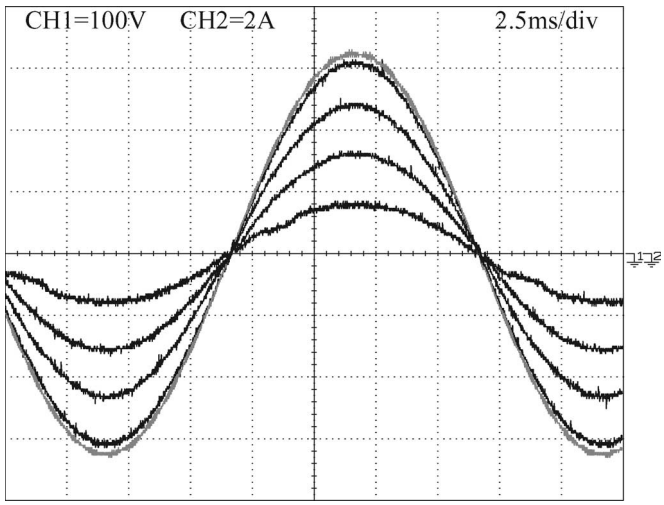

Fig. 7. (Black curves) Line current and (gray curve) line voltage of the boost PFC converter at 980-, 752-, 508-, and 253-W input power, with sinusoidal line voltage.

with huge distortion has been chosen: 10% of fifth and seventh harmonic and 20% of eleventh harmonic, corresponding to a total harmonic distortion (THD) of the line voltage of 24.5%. Although the input voltage is not flipped exactly at the point where the line voltage reaches zero (lower trace in Fig. 6), the PLL is able to follow the line voltage with the correct fundamental frequency and only a very small phase shift between the PLL output (upper trace in Fig. 6) and the input voltage (center trace). For input voltage waveforms with a "normal" distortion, the phase shift is virtually zero.

C. Input Impedance

In the experimental waveforms in Figs. 7 and 8, the harmonic input resistance of the converter is set to its minimum (maximum of g_h), which is equal to $Z_{\mathrm{in}}^{\mathrm{ref}} = 38.4\ \Omega$. In a first experiment, the influence of the new control algorithm on the operation of the converter with sinusoidal line voltage was evaluated. The results are shown in Fig. 7 and Table I. Both the

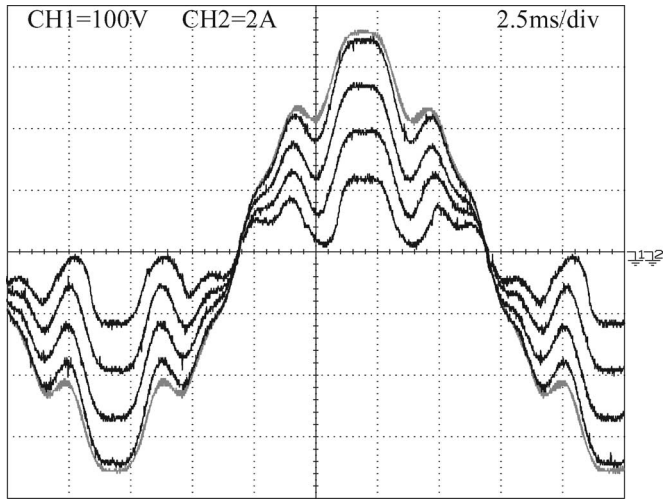

Fig. 8. (Black curves) Line current and (gray curve) line voltage for line voltage with fifth, seventh, and eleventh harmonic distortion, for 980-, 746-, 509-, and 263-W input power.

TABLE I
MEASUREMENTS OF THE THD_I AND THE POWER FACTOR FOR SINUSOIDAL LINE VOLTAGE

P_{in} [W]	THD_I [%]	power factor
980	1.04	1.000
752	0.96	0.999
508	1.10	0.999
253	4.70	0.998

figure and the table confirm that the line current of the converter shows a very low distortion as long as the converter operates in CCM (input power greater than 500 W [7]): the power factor is unity, whereas the THD of the line current is only 1% in a power range between 500 and 1000 W. Since for lower input power the converter starts operating partially in the DCM, the line current shows some distortion. Nevertheless, when sample correction is employed, the THD of the line current is limited to only 4.70% for operation at 253 W.

The new control strategy was also evaluated with a distorted line voltage waveform, supplied by the linear amplifier, and consisted of a fundamental 50-Hz voltage and different low-order harmonics: 10% of fifth harmonic voltage component and 5% of seventh and eleventh harmonic, corresponding with a THD of the line voltage of 12.25%. This voltage waveform is represented by the gray trace in Fig. 8. The input conductance for harmonics is set to its maximum value, corresponding with a theoretical harmonic input impedance of 38.4 Ω. The resulting input current is shown as black traces in Fig. 8 for different power levels (980, 746, 509, and 263 W). The three upper black traces in Fig. 8 show a clearly visible reduction of the fundamental component of the line current, whereas the amplitude of the harmonic components is maintained. The resulting harmonic impedance is shown in Table II, confirming the resistive nature (very low phase angle $\angle Z_{\mathrm{in},h}$) of the input impedance of the converter. Moreover, the magnitude of the harmonic impedance for the fifth, the seventh, and the eleventh

TABLE II
HARMONIC ANALYSIS OF THE WAVEFORMS IN FIG. 8

$P_{\rm in}$	980 W		746 W		509 W		263 W	
h	$\lvert Z_{{\rm in},h}\rvert[\Omega]$	$\angle Z_{{\rm in},h}[^\circ]$	$\lvert Z_{{\rm in},h}\rvert[\Omega]$	$\angle Z_{{\rm in},h}[^\circ]$	$\lvert Z_{{\rm in},h}\rvert[\Omega]$	$\angle Z_{{\rm in},h}[^\circ]$	$\lvert Z_{{\rm in},h}\rvert[\Omega]$	$\angle Z_{{\rm in},h}[^\circ]$
5	40.1	1	40.2	1.1	40.5	1	43.0	8.7
7	40.1	0.7	39.9	0.7	40.1	0.9	45.3	12.3
11	41.6	1	41.5	0.5	41.7	0.4	60.5	20.7

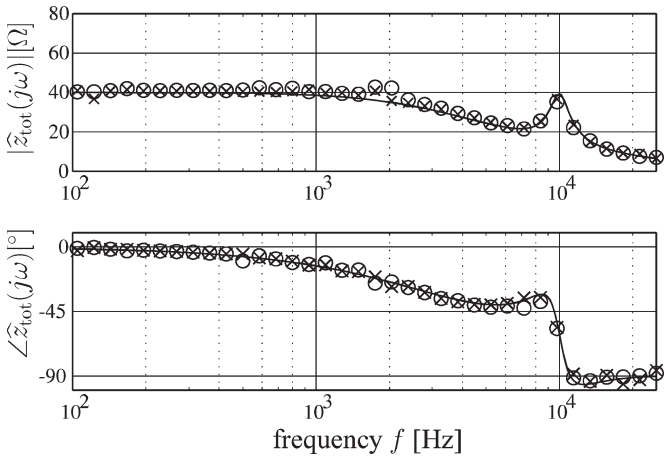

Fig. 9. Measured input impedance of the converter with programmable harmonic impedance set to $Z_{\rm in}^{\rm ref}$ for (crosses) 1-kW and (circles) 500-W input power, compared to the (full line) theory.

harmonic is constant for a wide power range from 500 W to 1 kW and remains very close to the programmed value.

Even when the converter starts operating in the DCM, corresponding to the lowest black trace in Fig. 8, the wave shape is hardly affected, which shows that the magnitude of the impedance remains more or less at its desired value. Nevertheless, Table II demonstrates that the phase angle increases for the harmonics. The reason for this distortion is clearly visible in the lowest black curve in Fig. 8: the combination of the large harmonic components of the inductor current and the low fundamental component leads to a low reference value for this inductor current, yielding operation in DCM. For even lower values of the fundamental component of the input current, the reference value may become negative, which is not achievable, due to the diode bridge at the input of the converter.

The resistive behavior of the input impedance of the converter is also confirmed by the experimental results of a frequency response analyzer, shown in Fig. 9 as circles for 500-W input power and as black crosses for 1 kW. This analyzer was employed to analyze the input current and input voltage of the converter for an input voltage consisting of a 230-V 50-Hz sinusoidal component and a small component (7-V amplitude) with a frequency varying between 100 Hz and 25 kHz. Fig. 9 shows that the converter behaves resistively up to a frequency of 1 kHz. For higher frequencies, the behavior will be a combination of a resistor and a capacitor: the magnitude of the impedance will start to decrease, whereas the phase shift steadily increases toward 90°. The experiments show that with the new control algorithm, the experimental results are still very close to the theoretical analysis performed in [8].

D. Damping Performance

The damping performance of the converter with programmable harmonic impedance is demonstrated on a scale model of a typical distribution feeder, as shown in Fig. 10. The power system is represented by its sinusoidal mains voltage $V_{\rm m}$ and its internal impedance $\omega L_{\rm m}$, which is dominated by the short-circuit impedance of the distribution system. The nonlinear loads are concentrated in the point of common coupling (PCC) and are capacitively smoothed diode bridge rectifiers with an input filter impedance $\omega L_{\rm NL}$. In the practical setup, typical values found in practice are used: $\omega L_{\rm m} = 4.47\%$ and $\omega L_{\rm NL} = 4.0\%$. All values are referred to the total apparent power of the distribution system (in this case, $S_{\rm REF} = 1200$ VA and the reference voltage $V_{\rm REF} = 230$ V). The total nonlinear load level $p_{\rm NL}$ is 15%.

The capacitor $C_{\rm m}$ represents the PFC capacitor banks. In the next experiments, the capacitor $C_{\rm m}$ is tuned to get a resonance at the ninth harmonic, resulting in a severe voltage distortion at the PCC, as shown in Fig. 11. In the same figure, the capacitor current i_C is also shown. The resonance at the ninth harmonic component is clearly visible. In Table III, the harmonic decomposition of the PCC voltage displays a maximum at the ninth harmonic component (5.22%). The resulting THD (THD_V) of the voltage at the PCC is 6.5%.

To mitigate this voltage distortion, the boost PFC converter with the proposed SHI current control loop is connected at the PCC. In Figs. 12–14, the voltage at the PCC $v_{\rm PCC}$ and the input current of the SHI $i_{\rm conv}$ are shown for three different SHI output power levels (253, 510, and 750 W, respectively). The damping performance is clearly shown in Table IV. The voltage THD at the PCC is reduced with about 50% to 3.2% for a resistive impedance value for harmonics $1/g_h$ of 1 p.u. As expected, the resulting THD_V values are almost independent of the output power level of the PFC converter.

Only for low power levels (300 W or lower), there is a small difference between the measured value and the predicted value of the current $i_{\rm conv}$. The reason is that the converter behavior differs from the ideal behavior when the boost PFC converter is operating in DCM for low power levels [8]. However, the damping performance remains virtually unaffected (Fig. 12, Table IV).

The damping performance of the proposed control strategy is compared with the damping performance of the "classical" resistive boost PFC converter. Therefore, the regular current control loop in Fig. 2 is used. In this case, the conductance for the fundamental component equals the conductance for harmonics and is dependent on the desired output power level. In Table V, the damping performance of the boost PFC converter

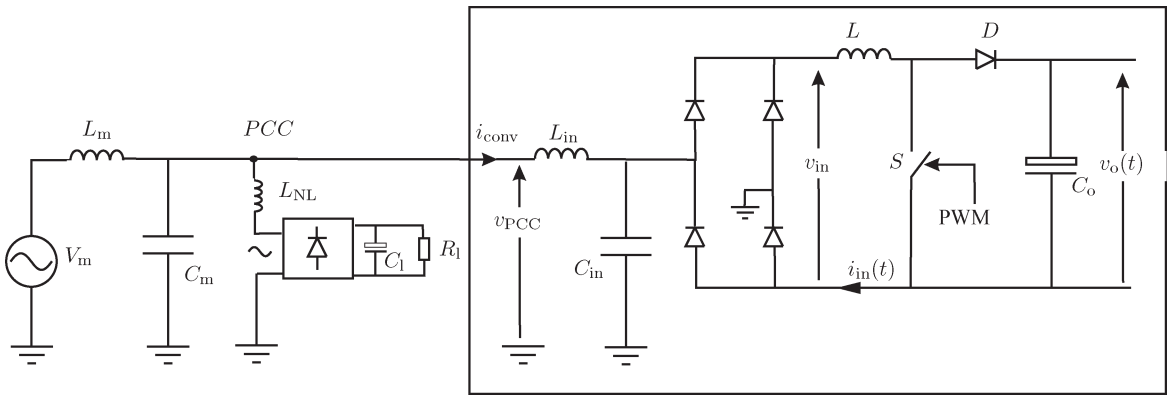

Fig. 10. Distribution system.

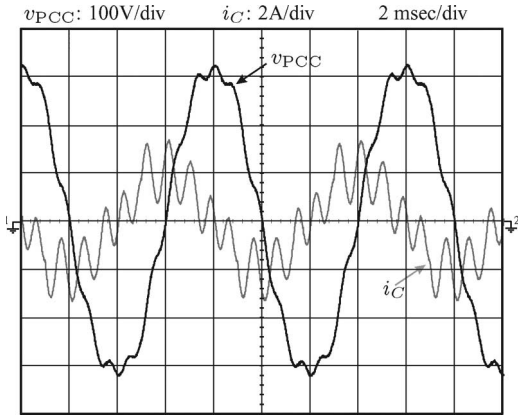

Fig. 11. $v_{\rm PCC}$ and i_C when no SHI is installed.

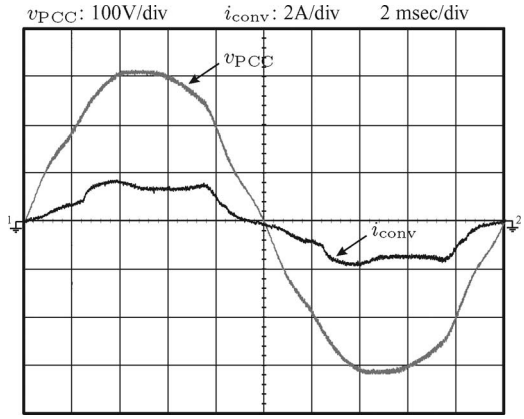

Fig. 12. $v_{\rm PCC}$ and $i_{\rm conv}$ for $P_{\rm o} = 253$ W.

TABLE III
$V_{\rm PCC}(h)$ WITHOUT CONVERTER

h	$V_{\rm PCC}$
1	232.2 V
3	1.68 %
5	2.11 %
7	2.73 %
9	**5.22 %**
11	0.61 %
13	0.57 %
15	0.24 %
17	0.10 %
19	0.10 %
21	0.04 %

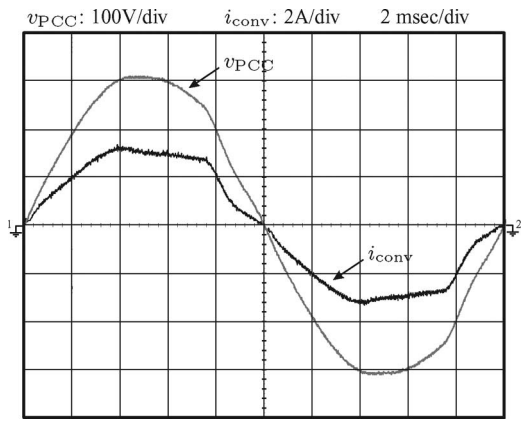

Fig. 13. $v_{\rm PCC}$ and $i_{\rm conv}$ for $P_{\rm o} = 510$ W.

is shown for the same output power levels as in Table IV. Because the damping performance is dependent on the output power level, large THD_V values may occur at light load (e.g., 253 W), due to the slightly damped resonance.

The input current $i_{\rm conv}$ has the same waveform as the input voltage $v_{\rm PCC}$ because of the constant resistive value for all harmonics, including the fundamental. This is shown in Fig. 15 for an output power level of 510 W (compare Fig. 15 with Fig. 13).

V. CONCLUSION

PFC converters with low harmonic input resistance are desirable loads to help reduce the harmonic distortion on the feeding grid. Therefore, a novel control strategy was proposed. Whereas previously proposed controllers tried to obtain a resistive behavior of the converter with a constant input impedance for all frequencies, including the fundamental, the proposed control strategy allows to set a harmonic input resistance independent of the fundamental component of the input current. Consequently, the harmonic input resistance remains low, even when the input power of the converter is decreased. This paper describes the operation of a digitally controlled boost PFC converter with the new control algorithm. Experimental tests on a 1-kW prototype show that a practical realization of the algorithm is possible and that the harmonic input resistance of the converter can be programmed very accurately in a wide

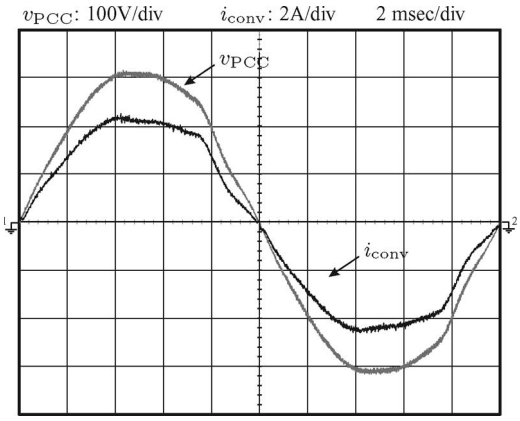

Fig. 14. v_{PCC} and i_{conv} for $P_o = 705$ W.

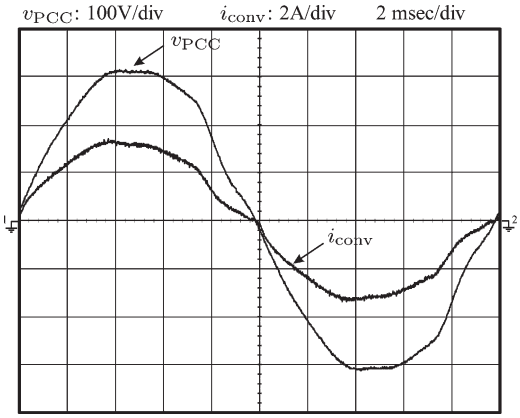

Fig. 15. v_{PCC} and i_{conv}; resistive PFC converter with resistive control strategy $P_o = 510$ W.

TABLE IV
THD$_V$(PCC) VALUES FOR DIFFERENT POWER LEVELS OF THE CONVERTER

	without SHI	253 W	510 W	705 W
$THD_V(PCC)$	6.5 %	3.7 %	3.2 %	3.2 %

TABLE V
THD$_V$(PCC) VALUES FOR A PFC CONVERTER WITH RESISTIVE CONTROL STRATEGY

	without SHI	253 W	510 W	705 W
$THD_V(PCC)$	6.5 %	5.7 %	4.1 %	3.7 %

power range of the converter. Eventually, the damping performance of the converter with the new control strategy has been compared with the usual resistive control strategy, showing a better damping of grid resonances for the new strategy.

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Koen De Gussemé (M'03) was born in Aalst, Belgium, in 1979. He received the M.Sc. degree in electromechanical engineering and the Ph.D. degree from Ghent University, Ghent, Belgium, in 2001 and 2006, respectively.

Since 2001, he has been a Researcher in the Electrical Energy Laboratory, Department of Electrical Energy, Systems and Automation, Faculty of Engineering, Ghent University. His research topics include digital control of switching converters, power factor correction, and grid-connected inverters for distributed generation.

Wouter R. Ryckaert (M'02) was born in Ghent, Belgium, in 1976. He received the M.Eng. degree in electrical engineering from the Katholieke Hogeschool Sint-Lieven, Ghent, in 1998, and the M.Sc. and Ph.D. degrees in electrical and mechanical engineering from Ghent University, Ghent, in 2001 and 2006, respectively.

Currently, he is with the Department of Industrial Sciences, Laboratorium voor Lichttechnologie, Katholieke Hogeschool Sint-Lieven. His research interests include power quality, electric power systems, and grid-connected inverters for distributed generation.

David M. Van de Sype (M'01) was born in Aalst, Belgium, in 1975. He received the M.S. and Ph.D. degrees in electromechanical engineering from Ghent University, Ghent, Belgium, in 1998 and 2004, respectively.

From November 1998 to September 2005, he was with the Electrical Energy Laboratory, Department of Electrical Engineering, Systems and Automation, Ghent University. Since October 2005, he has been with Inverto N.V., Evergem, Belgium, as a Senior Engineer, where he develops power electronic systems. His research interests include power electronics, control of converters, and power factor correction.

Jozef A. Ghijselen (S'89–M'90) received the M.Sc. and Ph.D. degrees from Ghent University, Ghent, Belgium, in 1990 and 2001, respectively.

Between 1990 and 2004, he has been with the Electrical Energy Laboratory, Ghent University. In 2004, he joined Inverto N.V., Evergem, Belgium, as a Senior Project Manager. His research interests include power electronics and power quality.

Jan A. Melkebeek (M'82–SM'84) was born in Ghent, Belgium, on February 20, 1952. He received the Dr. Ing. degree in electrical and mechanical engineering, the Ph.D. degree in applied sciences, and the Dr. Habilitus degree in electrical and electronical power technology from Ghent University, Ghent, in 1975, 1980, and 1986, respectively.

He was a Visiting Professor at the Université Nationale de Rwanda, Butare, Rwanda, Africa, in 1981 and a Visiting Assistant Professor at the University of Wisconsin, Madison, in 1982. Since 1987, he has been a Professor in electrical engineering (electrical machines and power electronics) in the Electrical Energy Laboratory (EELAB), Department of Electrical Energy, Systems and Automation (EESA), Faculty of Engineering, Ghent University. He is the Director of the EELAB (formerly the Laboratory for Electrical Machines and Power Electronics or before the Laboratory for Industrial Electricity). Since 1993, he has been the Department Head of EESA (formerly the Department of Electrical Power Engineering). His teaching activities and research interests include electrical machines, power electronics, variable frequency drives, and control systems theory applied to electrical drives.

Prof. Melkebeek is a member of the Koninklijke Vlaamse Ingenieursvereniging (K.VIV) and the Koninklijke Belgische Vereniging van Elektrotechnici (KBVE-SRBE). He is a Fellow of the Institution of Electrical Engineers. He serves also as a member of the IEEE Industry Applications Society (IEEE-IAS) Electric Machines Committee, the IEEE-IAS Electric Drives Committee, and the IEEE Power Engineering Society Machine Theory Subcommittee.

Lieven Vandevelde (M'05) was born in Eeklo, Belgium, in 1968. He received the M.Sc. degree in electrical and mechanical engineering and the Ph.D. degree from Ghent University, Ghent, Belgium, in 1992 and 1997, respectively.

Since 1992, he has been with the Electrical Energy Laboratory, Department of Electrical Energy, Systems and Automation, Faculty of Engineering, Ghent University. Since 2004, he has been a Professor in electrical power engineering at the same university. His research and teaching activities are in the field of electric power systems, electrical machines, and (computational) electromagnetics.