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Proton- and Neutron-Induced Single-Event Upsets in FPGAs for the PANDA Experiment

Markus Preston, Hans Calén, Tord Johansson, Myroslav Kavatsyuk, Károly Makónyi, Pawel Marciniewski, Peter Schakel, and Per-Erik Tegnér

***Abstract*— Single-event upsets (SEUs) affecting the configuration memory of a 28-nm field-programmable gate array (FPGA) have been studied through experiments and Monte Carlo modeling. This FPGA will be used in the front-end electronics of the electromagnetic calorimeter in PANDA (Antiproton Annihilation at Darmstadt), an upcoming hadron-physics experiment. Results from proton and neutron irradiations of the FPGA are presented and shown to be in agreement with previous experimental results. To estimate the mean time between SEUs during operation of PANDA, a Geant4-based Monte Carlo model of the phenomenon has been used. This model describes the energy deposition by particles in a silicon volume, the subsequent drift and diffusion of charges in the FPGA memory cell, and the eventual collection of charges in the sensitive regions of the cell. The values of the two free parameters of the model, the sensitive volume side $d = 87$ nm and the critical charge $Q_{\text{crit}} = 0.23$ fC, were determined by fitting the model to the experimental data. The results of the model agree well with both the proton and neutron data and are also shown to correctly predict the cross sections for upsets induced by other particles. The model-predicted energy dependence of the cross section for neutron-induced upsets has been used to estimate the rate of SEUs during initial operation of PANDA. At a luminosity of $1 \cdot 10^{31}$ cm^{-2} s^{-1}, the predicted mean time between upsets (MTBU) is between 120 and 170 h per FPGA, depending on the beam momentum.**

***Index Terms*— Field-programmable gate array (FPGA) configuration memory, Monte Carlo simulations, PANDA, single-event upsets (SEUs).**

I. Introduction

THE Facility for Antiproton and Ion Research (FAIR), currently under construction in Darmstadt, Germany, is an accelerator facility focused around four main experimental pillars. One of these is PANDA (Antiproton Annihilation at Darmstadt) [1], in which an antiproton beam with a momentum of between 1.5 and 15 GeV/c will interact in a fixed proton or nuclear target. The aim of the experiment is to investigate hadron-physics phenomena in an energy regime where the theoretical framework of the strong interaction (quantum chromodynamics or QCD) cannot be treated perturbatively.

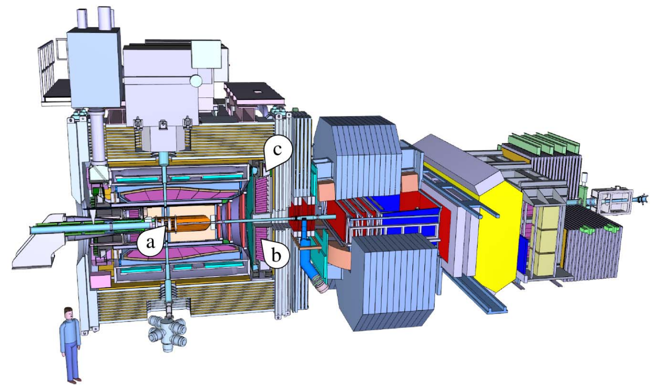

Fig. 1. Overview of the PANDA experiment. (a) Location of the beam target. (b) Location of the EMC forward endcap. (c) Location of the front-end digitizer boards. The length of the full setup is approximately 13 m. Courtesy of the PANDA collaboration.

One of the detector systems in PANDA is the target-spectrometer electromagnetic calorimeter (EMC), shown in Fig. 1, which will be used to detect photons, electrons, and positrons. The signals from the EMC will be read out by a large number of field-programmable gate array (FPGA)-based front-end digitizer boards, placed in close vicinity to the active detector volume. These boards will be exposed to different types of radiation, which can cause data corruption or device failure. One of the main risks anticipated are single-event upsets (SEUs) in the FPGAs, in which radiation interacting in the device can cause changes and malfunction of the FPGA.

The risk of SEUs is a major concern in the design and operation of particle-physics experiments [2], [3]. Today, there is an increased interest in using commercially available static random access memory (SRAM)-based FPGAs in the high-radiation environments present close to the detectors in these experiments [4], and there have been several studies aimed at qualifying these devices for such applications [5]–[7]. The radiation field in a collider experiment is often complex, consisting of various particles having a wide range of energies [8]. Therefore, studying the energy dependence of the SEU cross section for different particles would provide more details needed for quantifying the SEU risk. This is especially true

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for neutrons, which are common in a collider-experiment environment. Recently, the SEU threat posed to microelectronics by thermal and low-energy neutrons has been studied [8]–[10]. Here, we present measurements of the cross sections for SEUs induced by protons and neutrons of different energies in a 28-nm FPGA. The Monte Carlo model described in this article provides a way of determining the SEU energy dependence by fitting the model to measured data. Monte Carlo methods are commonly used to model SEUs in microelectronics [11]–[13], and the two-parameter model presented here was developed to predict the energy dependence of the SEU cross section in an FPGA where the exact material composition of the device is unknown. Through the two free parameters in the model, charge collection via both drift and diffusion is described, giving a more realistic description of the phenomenon than traditional methods. The free parameters of the model are determined from a detailed fit to experimental data, and the model is used together with separate simulations of the neutron fluence spectrum in PANDA to predict the rate of neutron-induced SEUs during operation of the experiment.

The structure of the article is as follows: In Section II, the PANDA EMC and the front-end digitizer are described, and the concept of SEUs in FPGAs is introduced. In Section III, the irradiations of the FPGA and the associated results are presented. In Section IV, the new model of SEUs is described and its results are presented and compared with experimental data. In Section V, the model is used to predict the rate of SEUs in PANDA.

II. EMC

The detectors in PANDA are divided into two subsystems: the target spectrometer (TS) and the forward spectrometer (FS). The TS surrounds the beam–target interaction point, whereas the FS is used to detect the most forward-boosted particles so that almost full solid-angle coverage is achieved. The two subsystems contain multiple types of detectors for tracking, particle identification, and calorimetry. EMCs will be used in both TS and FS, although they will be based on different technologies: the TS EMC [14] consists of approximately 16 000 scintillator crystals of lead tungstate (PWO)[1] and the FS EMC [15] is a shashlyk-type sampling calorimeter consisting of approximately 1500 cells of lead interleaved with plastic scintillators. In this article, the focus will be on the front-end electronics used in the TS EMC.

The TS EMC is subdivided into three parts: a cylindrical barrel and two endcaps. In the barrel and backward endcap parts of the EMC, as well as in the outer region of the forward endcap, large-area avalanche photodiodes will be used to read out the light from the scintillators. In the central region of the forward endcap, vacuum photo tetrodes will be employed as light sensors, due to their higher rate capability and radiation hardness. As the primary antiproton–proton interaction is of the fixed-target type, the highest particle fluences are expected in the most forward direction. This also has consequences for the front-end electronics, which will be placed very close to the EMC volume: as the highest fluences are expected in the forward endcap, the front-end electronics used to read out that part of the EMC will be exposed to the most harsh radiation environment. Fig. 1 shows the PANDA experiment, highlighting the parts relevant for this study.

[1]$PbWO_4$.

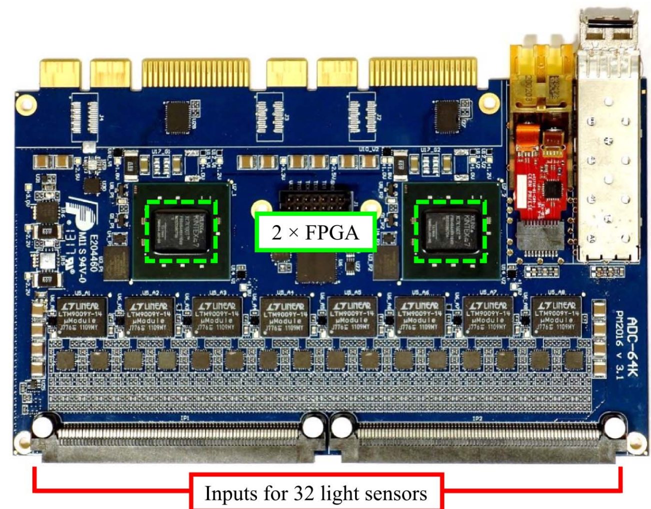

Fig. 2. Digitizer board for the TS EMC forward endcap. Each module has inputs for 32 light sensors, and the digitized signals are processed by two Kintex-7 FPGAs. From [16].

A. Front-End Digitizer

The photodetectors of the TS EMC forward endcap will be read out by 217 front-end digitizer boards, each equipped with two Xilinx Kintex-7 FPGAs. Signals from the detector are digitized by eight eight-channel analog-to-digital converter (ADC) circuits and then processed by two FPGAs. In order to cover the required energy range of the calorimeter, two levels of detector-signal amplification are used simultaneously. As a result, the 64 ADC channels on the board can digitize signals from up to 32 light sensors. As the PANDA experiment will be run without a hardware trigger, the data will be analyzed in real time by the FPGAs, with important signal features (such as pulse amplitude and timing) determined by the FPGAs. The FPGAs provide flexible preprocessing, and the signal features of the interesting events are transmitted via optical links. The layout of the device is shown in Fig. 2.

B. SEUs in FPGAs

Owing to the importance of the FPGAs in the EMC data chain, their reliability in the radiation field present during an experimental run has to be evaluated. Radiation-induced damage to FPGAs can be either cumulative or stochastic [17], [18]. Cumulative effects appear as the device is exposed to a higher and higher accumulated particle fluence, causing continuous degradation in the performance of the device. On the other hand, the topic of this article is SEUs, which is an example of stochastic radiation effects.

An SEU is a state change in microelectronics, induced by ionizing radiation. The resources in an FPGA can be conceptually separated into two layers—the application layer and the configuration layer [19]. The present study focuses

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on the configuration of the FPGA, which stores the functionality of the device in terms of logic resources and routing, as defined by the firmware. Changing the state of a single bit in the configuration memory could potentially change the logic and/or routing between blocks in the FPGA.

The configuration memory of the Kintex-7 FPGA is based on 28-nm SRAM [20], in which the state of a single configuration-memory bit is kept by a cell containing four transistors forming two cross-coupled inverters. The state of the cell can be changed by applying different voltages to the transistor gates—as is done when programming the device. When an ionizing particle passes through the transistor structure of the memory, it ionizes atoms in the device, creating free electron/hole pairs. If this excess charge is collected at the transistors in a sufficiently short time, the resulting current (and subsequent voltage drop) may be sufficient to cause the cell to change its state.

In order to estimate the SEU rate in the digitizer FPGAs, proton and neutron irradiations of the device have been performed. Charged particles may cause ionization through direct and indirect ionization. Direct ionization happens as the charged particle itself ionizes the material in the device. Indirect ionization happens when the incident particle reacts with an atomic nucleus in the device, causing highly ionizing reaction products to travel through the device. Indirect ionization is the main process through which protons cause SEUs, whereas direct ionization from protons does not generally generate enough charge to cause SEUs. Neutrons, being electrically neutral, do not cause ionization by themselves and so the only mechanism of neutron-induced SEUs is indirect ionization.

III. Experiments

One of the standard methods of characterizing the SEU sensitivity of a microelectronics device is through accelerated testing [21]–[24], where the device is irradiated in a high-intensity particle beam. If such measurements are performed with particles of different types and energies, the behavior of the device under realistic operating conditions may be estimated.

To measure the SEU sensitivity of the FPGA under different conditions, the Xilinx soft error mitigation (SEM) core [20] was implemented in the FPGA firmware. The tested FPGA had the part number XC7K160T, the same that is planned to be used in PANDA. In the studied FPGA, the configuration memory is divided into a number of frames, where each frame consists of 101 32-bit words [25]. A frame is the smallest addressable part of the configuration memory, and the SEM core continuously monitors each such frame for SEUs using an error correction code (ECC) scheme. This mechanism allows for the detection of state changes in individual bits and for correction of most of the corresponding SEUs. It is useful to define three particular types of SEUs in this context.

1) Single-bit upset: a single bit was upset by an ionizing particle.
2) Interframe multibit upset: multiple bits, each in a different memory frame, were upset.
3) Intraframe multibit upset: multiple bits within the same memory frame were upset.

During the experiments, the SEM core was able to correct all SEUs except for intraframe multibit upsets. These were reported as uncorrectable, and the device had to be power cycled and reconfigured to restore the upset bits. In addition to the error types above, which were identified using the ECC, the SEM core also reported errors detected with a cyclic redundancy check (CRC) mechanism. These errors were also uncorrectable. For the correctable errors, the locations of the upset bits were reported. For uncorrectable errors, no such information was available and, therefore, the exact number of bits involved in those errors was not known. The structure of the errors not correctable by the ECC has been studied in more detail earlier [5].

The SEU sensitivity of a device is quantified by the SEU cross section σ_{SEU}, which has been determined experimentally by irradiating the device with protons and neutrons of different energies. The SEU cross section per bit is the relation between the number of upset bits N_{SEU}, the particle fluence Φ, and the number of bits in the configuration memory N_0, given by

$$\sigma_{\text{SEU}} = \frac{N_{\text{SEU}}}{\Phi N_0}. \tag{1}$$

During all experiments, a single digitizer board was powered on at its operating voltage and placed such that the particle flux was centered on one of the two FPGAs, striking the front face of that FPGA perpendicularly to the surface of the board. In the proton and high-energy neutron irradiations, the particle beam covered approximately half of the digitizer board and was homogeneous over the surface of the FPGA. The SEM core was monitored continuously via a serial link, with its output timestamped and written to a log file.

A. Proton Irradiation

The device was irradiated with protons of three different energies—80, 100, and 184 MeV—at the Accélérateur Groningen-Orsay (AGOR) Facility for Irradiations of Materials (AGORFIRM) at KVI-CART, Groningen, the Netherlands [26]. During the irradiation, the primary beam had an energy of 190 MeV and was collimated using a 120-mm circular collimator. The beam was broadened using scatter foils to ensure a homogeneous fluence across the irradiated device. Because of this, and because the beam had to travel some distance through air, the maximum beam energy at the location of the device was 184 MeV. The two lower proton energies were obtained using aluminum degraders. The system was calibrated each time the particle energy was changed, so that the fluence could be determined.

B. High-Energy Neutron Irradiation

The device was irradiated with neutrons with a continuous energy spectrum below 180 MeV at the atmospheric-like neutrons from thick target (ANITA) neutron source at TSL, Uppsala, Sweden [27]. A proton cyclotron was used to generate a 180-MeV beam of protons, which was directed into a 2.4-cm-thick tungsten target. As the beam was stopped

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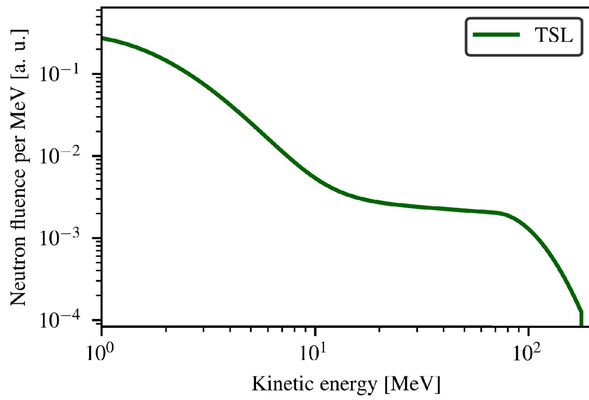

Fig. 3. Neutron energy spectrum at the location of the FPGA during the high-energy neutron irradiation. Data from [27].

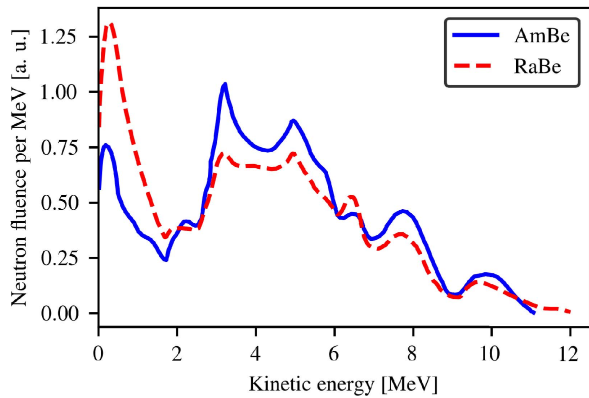

Fig. 4. Neutron energy spectra of the two low-energy neutron sources used during the experiments. Data from [28].

in the target, neutrons were generated in nuclear reactions. The resulting beam was collimated using a 100-mm circular collimator. Due to the spallation process used to generate the beam, the neutrons had a continuous energy distribution from 0 to 180 MeV, as shown in Fig. 3. In accordance with standards for accelerated neutron testing [23], the fluence of neutrons with energies above 10 MeV was determined by measuring the current from the tungsten target.

C. Low-Energy Neutron Irradiation

The device was irradiated with low-energy neutrons at Stockholm University using two different ^{9}Be(α, n) neutron sources: a radium–beryllium (RaBe) source and an americium–beryllium (AmBe) source. Due to differences in the energy distribution of the α particles emitted by radium and americium, the resulting neutron spectra differ slightly as shown in Fig. 4, but the maximum neutron energy is approximately 12 MeV for both sources. The relative neutron intensity for the two sources was measured, through neutron activation of indium, to be $I_{\mathrm{n}}(\mathrm{AmBe})/I_{\mathrm{n}}(\mathrm{RaBe}) = 0.53 \pm 0.02$ (one standard deviation). The absolute neutron intensity from the RaBe source was measured, through neutron activation of antimony, to be $(1.4 \pm 0.3) \times 10^{6}\ \mathrm{s}^{-1}$, giving an absolute neutron intensity from the AmBe source of $(0.7 \pm 0.2) \times 10^{6}\ \mathrm{s}^{-1}$.

TABLE I

NUMBER OF MEASURED CORRECTABLE (N_{C}), UNCORRECTABLE (N_{U}), AND CRC ERRORS (N_{CRC}) ERRORS

Particle	Energy [MeV]	Fluence [cm^{-2}]	N_{c}	N_{u}	N_{CRC}
Proton (KVI-CART)	80	$1.2 \cdot 10^{9}$	312	19	4
Proton (KVI-CART)	100	$1.7 \cdot 10^{9}$	391	18	4
Proton (KVI-CART)	184	$1.4 \cdot 10^{9}$	269	14	2
Neutron (TSL)	< 180	$2.1 \cdot 10^{9}$ [a]	549	22	2
Neutron (RaBe)	< 12	$3.0 \cdot 10^{9}$	91	2	0
Neutron (AmBe)	< 12	$4.3 \cdot 10^{9}$	117	2	0

[a] Fluence of neutrons above 10 MeV.

D. Analysis

As stated above, the exact number of bits involved in each reported error is not known if the error was uncorrectable. To determine the actual number of upset bits, the bit multiplicity M has been defined as the number of bits affected in a particular error. For correctable errors, the multiplicity is $M_{\mathrm{c}} = 1$, whereas for uncorrectable and CRC errors, it is only known that the multiplicities (M_{u} and M_{CRC}, respectively) are larger than 1. The total number of SEUs, $N_{\text{SEU, exp}}$, during an experiment is given by

$$N_{\text{SEU, exp}} = N_{\mathrm{c}} + N_{\mathrm{u}}\langle M_{\mathrm{u}}\rangle + N_{\mathrm{CRC}}\langle M_{\mathrm{CRC}}\rangle \tag{2}$$

where N_{c}, N_{u}, and N_{CRC} are the measured number of correctable, uncorrectable, and CRC errors, respectively. The measured number of errors of each type are presented in Table I. We assume that the probability distribution for M_{u} follows the one presented in [5], where intraframe errors during neutron irradiation of the Kintex-7 FPGA were studied. The mean of this probability distribution is $\langle M_{\mathrm{u}}\rangle = 2.4$. The number of CRC errors is generally small, and as no additional information about the bit multiplicity for these errors was available, it is assumed that the distribution giving M_{CRC} is the same as for M_{u}.

Inserting (2) into (1), the experimental cross section is given by

$$\sigma_{\text{SEU, exp}} = \frac{N_{\text{SEU, exp}}}{\Phi_{\text{exp}} N_0}. \tag{3}$$

The particle fluence Φ_{exp} was determined during each measurement, and the systematic uncertainties in the determined values were estimated to be 10% for the high-energy proton and neutron measurements and 30% for the low-energy neutron measurements. The uncertainties in $N_{\text{SEU, exp}}$ were determined by combining the statistical uncertainties in the number of measured errors with the details of the M_{u} probability distribution. Combining these with the systematic uncertainties in Φ_{exp}, the total uncertainties in the SEU cross sections were determined. The experimental results are presented in Table II. The SEU cross section for the Kintex-7 configuration memory has been studied through proton and neutron irradiations in the past: by reading back the configuration-memory bitstream after irradiation with 180-MeV [5], 105-MeV [7], and 64-MeV protons [29] and TSL neutrons [5], by using the Xilinx SEM core

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TABLE II
EXPERIMENTAL RESULTS

Particle	Energy [MeV]	$N_{\text{SEU, exp}}$	SEU cross section [10^{-15} cm^2 bit^{-1}]
Proton (KVI-CART)	80	367 ± 21 [a]	7.5 ± 0.9
Proton (KVI-CART)	100	444 ± 23	6.4 ± 0.7
Proton (KVI-CART)	184	307 ± 19	5.4 ± 0.6
Neutron (TSL)	< 180	607 ± 27	7.1 ± 0.8
Neutron (RaBe)	< 12	96 ± 10	0.87 ± 0.42
Neutron (AmBe)	< 12	122 ± 11	0.78 ± 0.38

[a] All uncertainties correspond to one standard deviation.

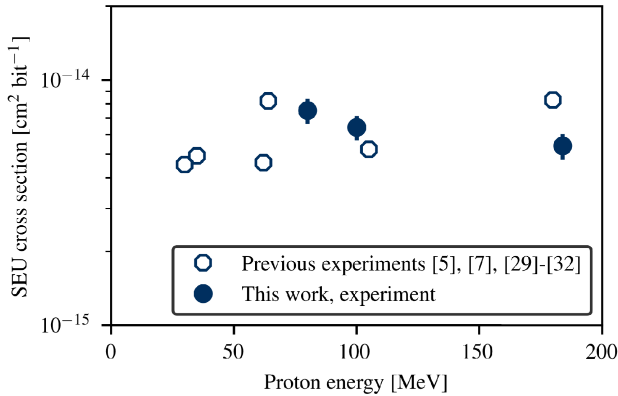

Fig. 5. SEU cross sections for protons as a function of proton energy. Results of the experiments in this article (filled circles) are compared with data from previous experiments (open circles).

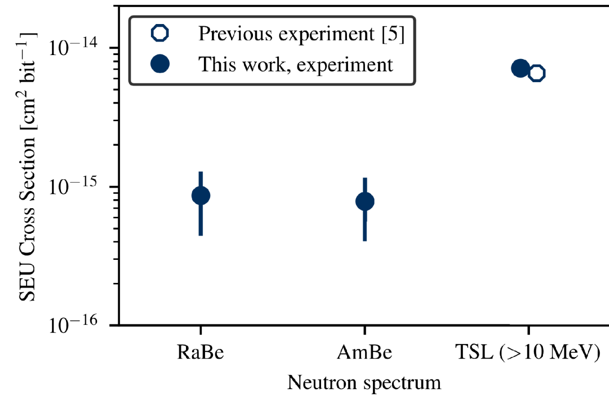

Fig. 6. SEU cross sections for neutron as a function of neutron energy spectrum. Results of the experiments in this article (filled circles) are compared with data from a previous experiment (open circle). Note that the SEU cross section for the TSL spectrum was determined using only neutrons above 10 MeV in the fluence calculation, as described in Section III-B.

during irradiation with 35-MeV protons [30], by using custom error detection and correction firmware during irradiation with 30-MeV protons [31], and by using an external scrubber providing error detection and correction during irradiation with 62-MeV protons [32]. These experiments were performed on different devices than in the present work, using FPGA part numbers XCK70T [30], [32] and XCK325T [5], [7], [29], [31] (compared to XCK160T used in the present work).

The experimental results from our measurements are compared with those from these previous experiments in Figs. 5 and 6.

IV. THEORETICAL MODELING

The experimental results describe the SEU sensitivity of the irradiated FPGA. However, the radiation environment at the locations of the digitizer boards in PANDA will not be the same as during the irradiations—the energy distributions of the incident particles will be different. In order to determine the energy dependence of the SEU cross section, a Monte Carlo model of SEUs has been developed. In this model, the Geant4 toolkit [33]–[35] has been used to simulate proton and neutron interactions in a $100 \times 100 \times 30$ μm^3 silicon volume. As discussed in Section II-B, charge collection by transistors in the FPGA is responsible for SEUs. The model contains two free parameters: the critical charge Q_{crit} and the sensitive volume side d. Q_{crit} is the amount of charge needed to upset the state of a transistor, and d determines the size of the region around the transistor with the most efficient charge collection. Conditional on these two parameters, the energy depositions determined from the simulations yielded predictions for the SEU cross section. The parameters of the model have been fit such that the experimental data were reproduced, after which the model can be used to predict the SEU cross section for any incident proton or neutron energy.

A. Geant4 Setup

The Geant4 toolkit has been used to develop models of radiation effects in microelectronics in the past [11]–[13], [36]–[42]. Depending on the application, the functionality of the toolkit itself can be tuned to give optimal performance and realistic results for the energy range and particle types of interest. In this article, interactions of protons and neutrons have to be described, mainly at energies below 200 MeV. Also, since the SEUs are ultimately caused by ionization close to the CMOS transistors, accurate models for electromagnetic physics are required. This is especially true because of the small dimensions of the CMOS cell.

To include all of the required features in the Geant4 simulation, the QGSP_BIC_HP_electromagnetic option 4 (EMZ) physics list was chosen. It relies on the quark gluon string model for hadronic interactions above 10 GeV and a binary cascade model for interactions of primary protons and neutrons at lower energies. It uses the NeutronHP package, which gives the most accurate description of neutrons below 20 MeV. Finally, the EMZ electromagnetic option includes a combination of the most detailed models for low-energy electromagnetic physics. All simulations were performed with version 10.4 of Geant4.

As stated above, the Geant4 simulation consisted of simulating the energy depositions resulting from proton and neutron interactions in a $100 \times 100 \times 30$ μm^3 silicon volume. As the model was aimed at studying the effects of these energy depositions on a single memory cell, some limitations had to be imposed on the beam size in the simulation. This is because the beam area in combination with the number of

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TABLE III
PARAMETERS OF THE SIMULATIONS

Particle	Energy [MeV]	Number of initial particles	Fluence [cm^{-2}]
Proton	80	$2 \cdot 10^{11}$	$2.2 \cdot 10^{16}$
Proton	100	$2 \cdot 10^{11}$	$2.2 \cdot 10^{16}$
Proton	184	$2 \cdot 10^{11}$	$2.2 \cdot 10^{16}$
Neutron	$<$ 180 (TSL)	$8 \cdot 10^{11}$	$8.9 \cdot 10^{16}$ (all energies) $2.1 \cdot 10^{16}$ ($>$ 10 MeV)
Neutron	$<$ 12 (RaBe)	$8 \cdot 10^{11}$	$8.9 \cdot 10^{16}$
Neutron	$<$ 12 (AmBe)	$8 \cdot 10^{11}$	$8.9 \cdot 10^{16}$

simulated primary particles determines the particle fluence Φ_{sim} incident on the single memory cell. To increase the fluence without increasing the computing time, the beam size could be decreased. However, the size of the beam still had to be considerably larger than the memory-cell area. The reason for this is that there is a possibility that even a particle produced far away from the memory cell can reach the cell and cause sufficient ionization close to the transistors. This effect will be underestimated if the beam area is the same as the cell area. The beam size used in the model was determined by investigating the beam-size dependence of the predicted cross section. The cross section saturates at large beam sizes, where all contributions from ionizing particles generated far from the cell have been taken into account. To include this effect and still allow for reasonable computing time, the beam size was set to 30×30 μm^2.

Six Geant4 runs were performed to compare the model predictions with the experimental data: three with 80-, 100-, and 184-MeV protons, and three with neutrons having continuous energy spectra. The three proton beams were assumed to be fully monoenergetic, whereas the applied neutron energy spectra were taken from measurements and models of the TSL [27] and RaBe/AmBe neutron spectra [28]. Although the full energy spectrum of TSL was included in the model, the corresponding Φ_{sim} was determined for the neutrons above 10 MeV. This was done to allow for comparison with the experiment, where only the fluence above 10 MeV was measured and used to determine the cross section. Nonetheless, neutrons below 10 MeV cause SEUs (as demonstrated through the low-energy neutron irradiations described in Section III) and such events would be included in the model. Table III summarizes the six runs.

The Geant4 geometry itself did not contain anything related to the memory cell or the transistors—these features were included in a later stage of the analysis and are described below. To allow for this analysis, the start and end positions and the energy-deposition information of all particle steps occurring during the Geant4 simulations were stored.

B. Model Geometry

The rectangular parallelepiped (RPP) model has been used to simulate SEUs in microelectronics in the last 40 years [43]–[48] and has previously been used to predict the rate of SEUs in PANDA [49]. In this model, a single memory cell is represented by a parallelepiped. By simulating particles incident on the memory cell, the amount of deposited energy in the RPP may be determined for each event. If the amount of generated charge during an event is larger than a specified critical charge, the event is classified as an SEU. The parameters in such a model are the RPP size and the critical charge. The basic assumption of this model, that the charge-collection mechanism after ionization in the device may be represented by a single volume which has a uniform charge-collection efficiency, is unphysical as has been pointed out by Wrobel *et al.* [50], Warren *et al.* [51], and Sogoyan *et al.* [52]. In reality, the charge-collection efficiency of a transistor is not constant throughout a fixed volume, since multiple processes contribute to the charge-collection mechanism. The two main processes are charge drift and charge diffusion [53]. Drift occurs when an electron or hole is liberated in close proximity of a p-n junction in a transistor. In this region, an electric field is present and the charge is rapidly collected. Diffusion occurs when an electron or hole is liberated further down into the silicon substrate. In this region, there are no strong fields present and the charge has to diffuse to a transistor p-n junction where it is collected efficiently. Different approaches have been taken to address these shortcomings of the RPP model, for example, by modeling the time structure of charge diffusion and collection [54], [55], by modeling the total amount of charge collected through diffusion [50]–[52], or by introducing a nested RPP model that allows for variations in the charge-collection efficiency [51]. More realistic models such as these also allow for charge sharing between adjacent transistors and memory cells, an effect not included in the standard RPP model.

The model presented in this article has been developed to address some of the issues with the RPP model and treats charge diffusion in a way similar to what has been proposed in [50] and [52]. It can be seen as an extension of the traditional RPP model, modeling both charge drift and diffusion. At the same time, it only contains two free parameters and does not assume any detailed knowledge of the physical structure of the device. It relies on five main assumptions with regard to the structure of a single memory cell:

1) The cell is assumed to contain four transistors—two nMOS transistors and two pMOS transistors—that are potentially sensitive to charge collection. These are the transistors holding the state of the cell. At any moment, two of these transistors will be on and two off.
2) Only the drains of the off-transistors are assumed to be sensitive to charge collection, as indicated by a previous work [56].
3) Because of the directions of the electric fields present near the drains, only electrons are assumed to be efficiently collected at the off-nMOS drains, and only holes at the off-pMOS drains.
4) The transistor drains are assumed to be placed 110 nm apart on a row in the memory cell. This distance was chosen as it agrees well with the scaling trends of the memory-cell area with respect to the CMOS feature size [57].
5) The only material included in the model is silicon, as the details of the structures and materials around

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and above the transistors were not known. To imitate the presence of the material above the memory cell, the cell was located 15 μm into the silicon volume. This is half the width of the beam, which as discussed in Section IV-A was chosen such that SEUs caused by secondary particles generated far from the sensitive parts of the cell are also included in the model. This argument can be made also when it comes to the thickness of the material above the cell—the probability that a secondary particle produced very far above the cell causes an SEU is very low.

Each of the four transistor drains is modeled as a cylinder with the base diameter being equal to the height. The size of such a cylinder is therefore fully determined by the cylinder height d. In each cylinder, charge is assumed to be collected with a high, constant efficiency due to the presence of an electric field. This is analogous to the RPP model. Charge collection below the cylindrical volumes, i.e., further down into the CMOS substrate, is possible but with a probability proportional to the solid angle subtended by the cylinder bases. To first order, this describes the probability for diffusion from a point in the CMOS substrate to one of the regions with a high electric field present (the cylinders). A schematic drawing of the memory-cell structure in the model is shown in Fig. 7.

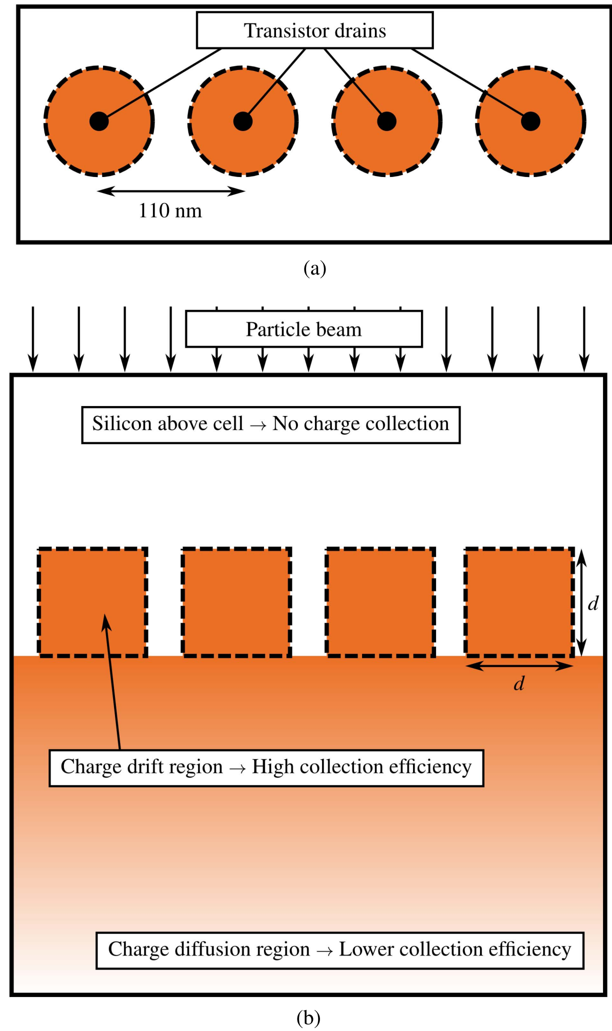

Fig. 7. Geometry of the memory cell in the SEU model. (a) Top view of the cell, indicating the positions of the transistor drains relative to the cell and each other. The dashed circles around the drains show possible sizes of the core cylinder of the sensitive volume. (b) Memory cell from the side, and how the charge-collection efficiency decreases further down into the silicon substrate.

C. Charge-Collection Analysis

As discussed above, each position (x, y, z) in the silicon block has an associated charge-collection efficiency ϵ_{coll}. Inside the cylinders, the charge-collection efficiency assumes a constant value of 100%. Below the cylinders, the probability that a generated charge reaches cylinder i is proportional to the solid angle Ω_i subtended by the base of that cylinder. This can be seen as a first-level approximation based on the random-walk nature of the diffusion process [58]. If a charge reaches the cylinder base, it will be collected with the same efficiency as all charges inside the cylinder. The charge-collection efficiency at all other locations (above and between the cylinders) is zero. The full charge-collection efficiency for a single cylinder i is thus given by

$$\epsilon_{\text{coll},\ i}(x, y, z) = \begin{cases} 1, & \text{inside cylinder } i \\ \Omega_i(x, y, z)/4\pi, & \text{below cylinder } i \\ 0, & \text{otherwise.} \end{cases} \quad (4)$$

As mentioned in Section IV-A, the information of all particle steps in the Geant4 simulations were stored. For each event, with one primary proton or neutron, there is a set of steps, each having a start position $\vec{r}_0$ in the silicon block and an end position $\vec{r}_1$ in the block. In the simulations used in this article, the average step length was approximately 50 nm. Each step had an associated energy deposition E_{dep}, which corresponds to the amount of energy lost via ionization during the step. It is assumed that the number of electron–hole pairs N_{eh} generated along the step is proportional to E_{dep}:

$$N_{\text{eh}} = kE_{\text{dep}} \quad (5)$$

where $k = 1/3.6\ \text{eV}^{-1}$ for silicon [59].

A single step from the Geant4 simulation is a straight line between $\vec{r}_0$ and $\vec{r}_1$. By parameterizing this line, the variable t gives any point $\vec{r}(t)$ along the step

$$\vec{r}(t) = \vec{r}_0 + t(\vec{r}_1 - \vec{r}_0), \ \ 0 \le t \le 1. \quad (6)$$

The total charge q_{coll} collected from a single step by the ith cylinder is determined by integrating the charge-collection efficiency along the whole step, also taking the electron–hole production into account

$$q_{\text{coll, i}} = \int_0^1 dt\ \ N_{\text{eh}} \cdot e \cdot \epsilon_{\text{coll},\ i}(\vec{r}(t)) \quad (7)$$

where e is the elementary charge. As stated above, it is assumed that for each produced electron–hole pair, only the electron or the hole will have the possibility of being collected at a particular drain.

During the analysis, the ROOT toolkit [60] was used. For each simulated event, (7) was solved numerically for all

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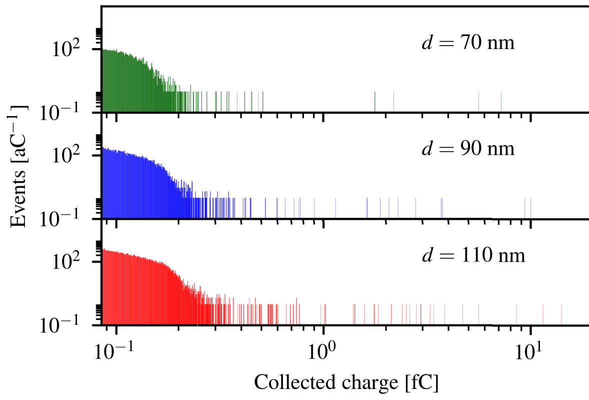

Fig. 8. Distribution of the amount of collected charge Q_{coll} at one of the four transistor drains for three different sensitive volume sides d for $2 \cdot 10^{11}$ primary 80-MeV protons.

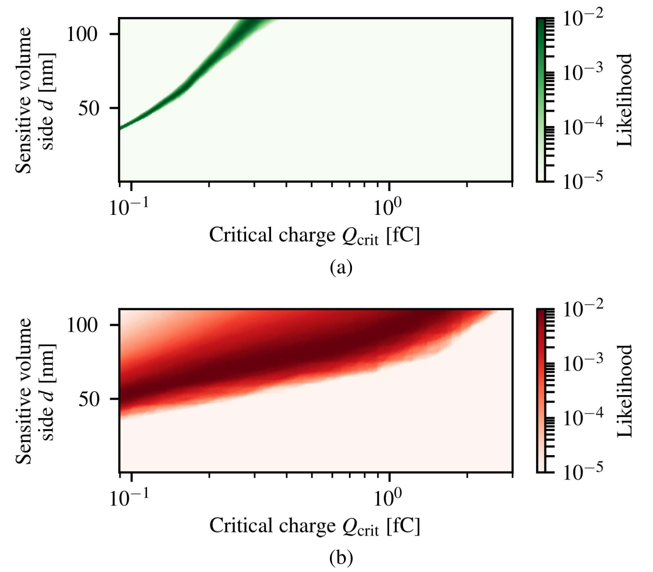

Fig. 9. Likelihood-function values as a function of the critical charge Q_{crit} and the sensitive volume side d for (a) 80-MeV protons and (b) AmBe neutrons.

associated steps and the total collected charge in each cylinder, Q_{coll}, was determined by summing the contributions from all steps. It is clear that Q_{coll} will depend on d, as a larger cylinder collects more charge than a small. This can be seen in Fig. 8, where the distribution of collected charge in one of the four cylinders is shown for three different values of d.

The second free parameter of the model is the so-called critical charge Q_{crit}. In principle, it is the charge that has to be collected at a transistor drain (i.e., in a cylinder in this model) for the cell to change state. However, depending on the actual initial state of the cell (0 or 1), only two of the four cylinders will be sensitive to charge collection. One, therefore, has to consider two independent cases, which are defined as follows:

1) Initial state = 0: cylinder 1 is sensitive to collection of negative charges and cylinder 3 is sensitive to collection of positive charges.
2) Initial state = 1: cylinder 2 is sensitive to collection of positive charges and cylinder 4 is sensitive to collection of negative charges.

These initial conditions were analyzed separately using the same simulation output. For each event, if the amount of collected charge in cylinder 1 or 3 exceeded Q_{crit}, the event was classified as an SEU flipping the cell state from 0 to 1. If the amount of collected charge in cylinder 2 or 4 exceeded Q_{crit}, the event was classified as an SEU flipping the cell state from 1 to 0. The SEU cross section predicted by the model for a certain value of d and Q_{crit} is

$$\sigma_{\text{SEU, model}}(d,\ Q_{\text{crit}}) = \frac{1}{2\Phi_{\text{sim}}}\left(N^{0\to1}_{\text{SEU, model}}(d,\ Q_{\text{crit}}) + N^{1\to0}_{\text{SEU, model}}(d,\ Q_{\text{crit}})\right) \quad (8)$$

where $N^{0\to1}_{\text{SEU, model}}$ and $N^{1\to0}_{\text{SEU, model}}$ are the number of SEUs in each bit-flip case and Φ_{sim} is given by Table III.

D. Fit to Data

Combining (1) and (8), the model-predicted cross section may be used to predict the expected number of experimentally observed SEUs:

$$\left\langle N^{*}_{\text{SEU, exp}}\right\rangle(d,\ Q_{\text{crit}}) = \sigma_{\text{SEU, model}}(d,\ Q_{\text{crit}})\Phi_{\text{exp}}N_0. \quad (9)$$

In order to determine which values of d and Q_{crit} give the best fit to the experimental data, a likelihood fit was performed. The likelihood $L(N_{\text{SEU, exp}}|d,\ Q_{\text{crit}})$ is the probability of experimentally measuring a particular number of SEUs, given certain values of d and Q_{crit}. This probability was determined by first convolving the distributions of $\sigma_{\text{SEU, model}}$ and Φ_{exp} (the former being given by the statistical uncertainty in the model and the latter by the experimental uncertainty in the fluence) to give the distribution of $\langle N^{*}_{\text{SEU, exp}}\rangle$. The resulting distribution was convolved with a Poisson distribution with a mean given by $\langle N^{*}_{\text{SEU, exp}}\rangle$. The assumption that this variable is Poisson distributed is reasonable, as motivated by the fact that the number of uncorrectable errors in the measurements is much smaller than the number of correctable errors, as shown in Table I. By determining the likelihood function in this way, both the experimental and model uncertainties were taken into account. The likelihood function was evaluated for each of the six measurements and is shown in Fig. 9 for two of the measurements.

The probability that a particular pair of d and Q_{crit} values are correct is in Bayesian statistics given by the posterior probability. Assuming a uniform prior probability and that the marginal likelihood is simply a normalization constant, the posterior probability is proportional to the product of the six individual likelihood functions, as shown in the following equation:

$$p\left(d,\ Q_{\text{crit}}|\vec{N}_{\text{SEU, exp}}\right) \propto \prod_{i=1}^{6} L\left(N^{(i)}_{\text{SEU, exp}}|d,\ Q_{\text{crit}}\right). \quad (10)$$

The normalized posterior distribution is shown in Fig. 10. The parameter expected values, standard deviations, and

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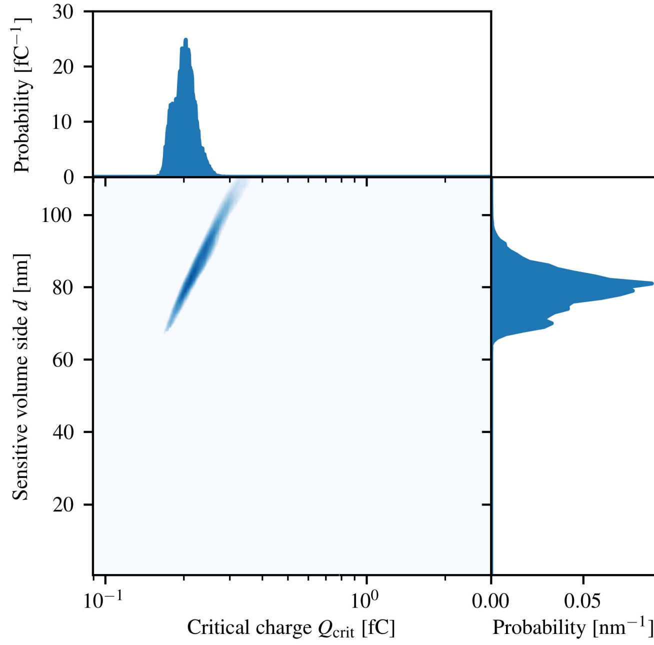

Fig. 10. Posterior distribution of the two parameters in the model, the critical charge Q_{crit} and the sensitive volume side d. The 1-D distributions are the marginal distributions for the parameters.

TABLE IV

PARAMETERS OF THE POSTERIOR DISTRIBUTION. THE PARAMETER UNCERTAINTIES CORRESPOND TO ONE STANDARD DEVIATION OF THE POSTERIOR DISTRIBUTION

Parameter	Value	Unit
d	87 ± 7	nm
Q_{crit}	0.23 ± 0.03	fC
$\text{cov}(d,\ Q_{\text{crit}})$	0.192	nm^2 fC^2

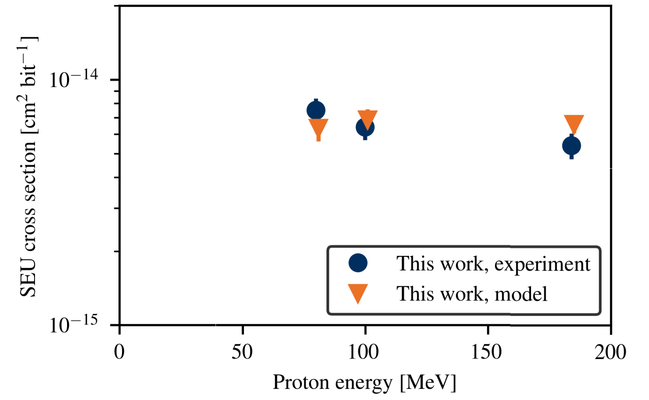

Fig. 11. SEU cross sections for protons as a function of proton energy. Results of the model (triangles) are compared with the experimental data (circles) of this article.

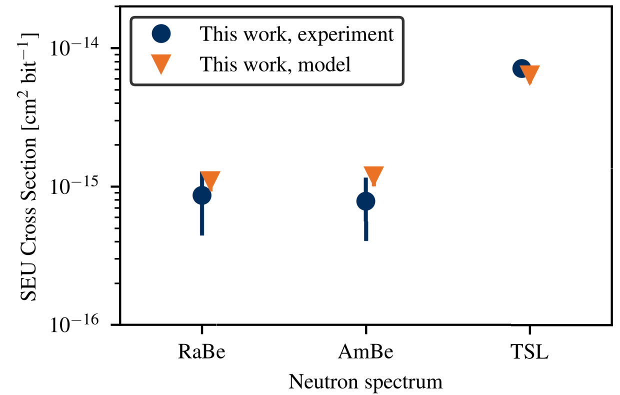

Fig. 12. SEU cross sections for neutrons as a function of neutron energy spectrum. Results of the model (triangles) are compared with the experimental data (circles) of this article. Note that the SEU cross section for the TSL spectrum was determined using only neutrons above 10 MeV in the fluence calculation, to mimic the experimental considerations described in Section III-B.

covariance, as determined from the posterior distribution, are presented in Table IV.

E. Results of Fit

To enable comparison between the model predictions and the experimental data, the cross sections predicted by the model were determined using posterior predictive checking [61] methods. Here, the model-predicted cross sections were determined as functions of Q_{crit} and d and weighted with the posterior distribution to yield the best estimates of the cross sections. The model predictions are compared with the experimental results in Figs. 11 and 12.

The SEU cross sections predicted by the model are in overall agreement with the experimental data, both for proton- and neutron-induced upsets. In order to quantify the goodness of fit, the likelihood ratio [62] may be used:

$$\lambda = \frac{\prod_{i=1}^{6} L\left(N_{\text{SEU, exp}}^{(i)} | \langle d,\ Q_{\text{crit}} \rangle\right)}{L_0} \tag{11}$$

where $L(N_{\text{SEU, exp}} | \langle d,\ Q_{\text{crit}} \rangle)$ is the value of the likelihood function at the expected value of the posterior distribution, as shown in Table IV, and L_0 is the value of the likelihood function in the hypothetical case of the model predictions exactly matching the experimental data. In practice, the quantity $-2\log(\lambda)$, which has the same interpretation as the χ^2 in the case of Gaussian uncertainties, is commonly used and was determined to be $-2\log(\lambda) = 11.3$ with four degrees of freedom.

F. Model Validation

The critical charge predicted by the model, $Q_{\text{crit}} = 0.23 \pm 0.03$ fC, is in good agreement with predictions based on the scaling trends of CMOS devices [63]. In that work, the critical charge at a feature size of 32 nm is predicted to be between 0.13 and 0.44 fC and between 0.088 and 0.36 fC at a feature size of 22 nm. The predicted value of the sensitive volume side, $d = 87 \pm 7$ nm, is reasonable based on the geometry of the modeled memory cell. The distance between the centers of two adjacent cylinders was set to 110 nm based on the CMOS scaling trends, and at the predicted value of d there is no overlap between adjacent cylinders. This corresponds

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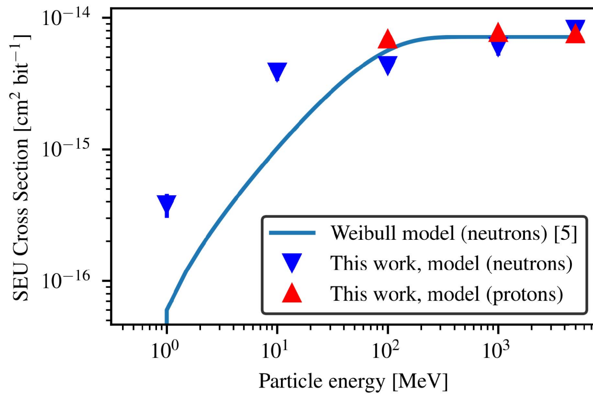

Fig. 13. SEU cross sections for neutrons and protons as a function of energy. Results of the present model (triangles) are compared with a model (full-drawn) for neutrons proposed in [5].

to a realistic situation where there is no sharing of charge between different drains close to the transistors due to the strengths of the electric fields there.

The model can be used to predict $\sigma_{\text{SEU}}(E_{\text{n}})$, the cross section for neutron-induced SEUs as a function of neutron energy. This variable has been studied for the Kintex-7 FPGA in the past [5], where the energy dependence was modeled as a Weibull function saturating at high neutron energies. There, the parameters of this function were determined by combining measurements of the SEU cross section in a high-energy neutron beam with measurements of the interaction cross section of the same beam in a silicon detector. Fig. 13 shows a comparison between the Weibull model and the predictions by the model in this article. Although the two models agree well at high neutron energies, there are some discrepancies at lower energies. This could be partly due to the fact that the Weibull model was fit to high-energy neutron data only.

The model can also be used to predict the cross section $\sigma_{\text{SEU}}(E_{\text{p}})$ for proton-induced SEUs as a function of proton energy, as shown in Fig. 13. Indirect ionization is the primary SEU mechanism for high-energy protons and neutrons, whereas low-energy protons have been shown to cause SEUs through direct ionization [64]–[66]. The good agreement between the neutron and proton cross sections at high energies indicates that the cross sections for the nuclear reactions needed in indirect ionization are similar for neutrons and protons. It is not clear in what way low-energy protons affect the FPGA studied in this article, and therefore, the reliability of the model in that energy regime cannot be confirmed. There are unfortunately no experimental data on low-energy proton irradiations of the Kintex-7 FPGA. Because of this, and because low-energy protons are not a concern during operation of PANDA as described in Section V, the model will not be used for predictions of low-energy proton SEUs.

The model of the memory cell presented here only contains very little material above the memory cell (15 μm of silicon), and no metals which are probably present in the real device. Inclusion of heavier elements in the model would affect the energy loss of incident particles due to both ionization and nuclear reactions. This has been shown to affect the cross section for single-event effects in some devices, for instance, through induced fission in tungsten [67]–[69]. Because of this, the true Q_{crit} value may be different from the one predicted here, especially since the model was fit to data where the primary mechanism of SEUs is indirect ionization. On the other hand, including only silicon greatly simplifies the model as no detailed knowledge of the device is necessary.

TABLE V
PROPERTIES OF THE HEAVY IONS USED TO DETERMINE THE SEU CROSS SECTION DEPENDENCE ON LET

Ion	Beam energy [MeV]	Linear energy transfer at surface [MeV mg^{-1} cm^{-2}]
^{15}N^{+4}	139	1.83
^{20}Ne^{+6}	186	3.63
^{30}Si^{+8}	278	6.42
^{40}Ar^{+12}	372	10.15
^{56}Fe^{+15}	523	18.54
^{82}Kr^{+22}	768	32.10

In order to test the validity of the model in cases where direct ionization is the primary mechanism of SEUs, the model has been used to predict σ_{SEU} as a function of linear energy transfer (LET) by simulating interactions of heavy ions with different LET values in the silicon volume. The properties of the ions were taken from [70] and are presented in Table V. The LET dependence of the SEU cross section for the Kintex-7 configuration memory has been studied through heavy-ion irradiations in the past: by reading back the configuration-memory bitstream after irradiation [71] and by using the Xilinx SEM core during irradiation [30], [72]. In these measurements, the top layers of the evaluated FPGAs (part numbers XC7K70T [30], [72] and XC7K325T [71]) were thinned to allow high-LET heavy ions to reach the sensitive parts of the devices. The model predictions are compared with these data in Fig. 14. The agreement is good at relatively low LET values, whereas the model overestimates the SEU cross section at higher LET values. As the model was fit to measurements with neutrons and high-energy protons, the agreement is surprisingly good for heavy ions, considering the different upset process. Nonetheless, the simplified memory-cell geometry in the model most likely affects highly ionizing particles differently than the materials that even after thinning of the FPGA were present above the memory cells in the experiments [73]. These effects would be more pronounced at high LET values [74], where the largest discrepancy between the model and experiment are also seen in Fig. 14.

V. SEU Rates in PANDA

When used in the PANDA experiment, the digitizers in the forward endcap EMC will be placed in crates around the perimeter of the detector. In order to predict the expected rate of radiation-induced SEUs in the FPGAs under these conditions, the particle fluence as a function of energy is needed. To estimate this, PandaRoot [75], based on the FairRoot [76] Monte Carlo simulation framework,[2] was used.

[2]In this article, FairRoot version 16.06 and PandaRoot version dec17 were used.

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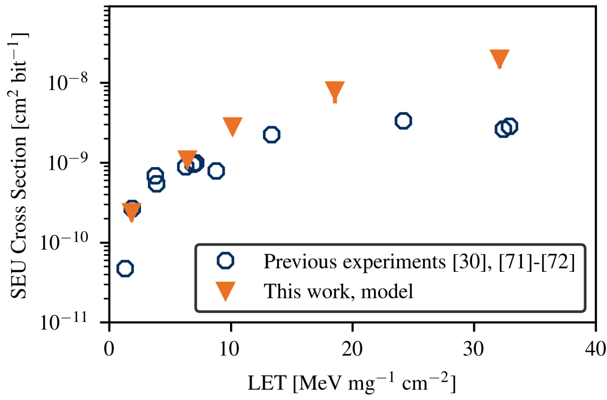

Fig. 14. SEU cross sections for heavy ions as a function of LET. Results of the present model (triangles) are compared with previous experiments (open hexagons).

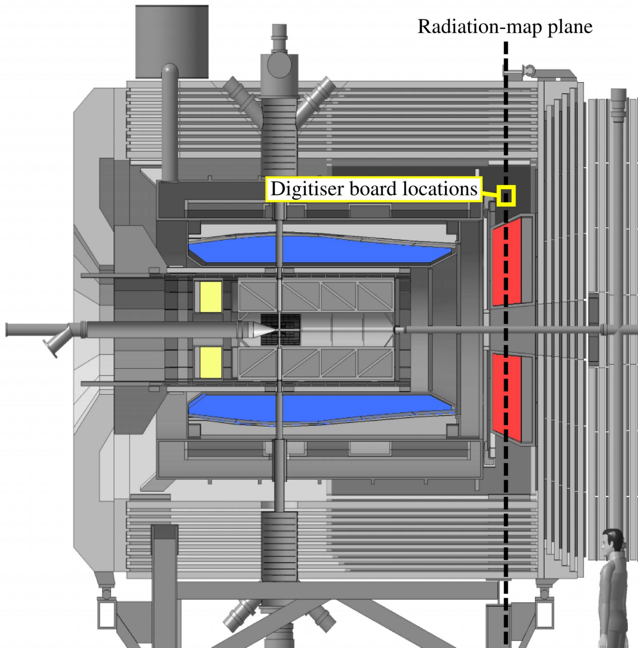

Fig. 15. Cross-sectional view of the PANDA TS. The location of the plane on which the particle fluence was estimated is shown, as is the location of the EMC digitizer boards in this cross-sectional plane. From [14].

In this article, the dual parton model [77] event generator was used to generate proton–antiproton interactions at beam momenta of 1.5 and 15 GeV/c. At each of the two beam momenta, 3×10^6 primary interactions were generated.

PandaRoot relies on Geant4 for tracking all particles resulting from the primary interaction through the PANDA detector geometry. To determine the particle fluence from the PandaRoot simulation, the energy and position information of all trajectories was stored. A plane intersecting the forward endcap vertically, as shown in Fig. 15, was defined. This plane represents the location of the digitizers along the beam axis. All trajectories were checked for intersections with this plane, and the point of intersection on the plane was determined for all intersecting trajectories. Fig. 16 shows the determined fluence rate for neutrons at the plane after evaluating all

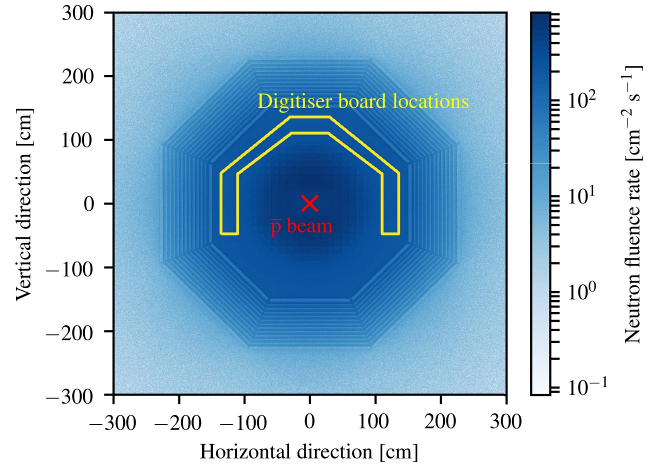

Fig. 16. Map of the neutron fluence rate at a plane through the forward endcap EMC at a beam momentum of 1.5 GeV/c and a luminosity of 1×10^{31} cm^{-2} s^{-1}. The locations of the digitizers are shown by the yellow polygon, and the direction of the antiproton beam shown in the center of the plot.

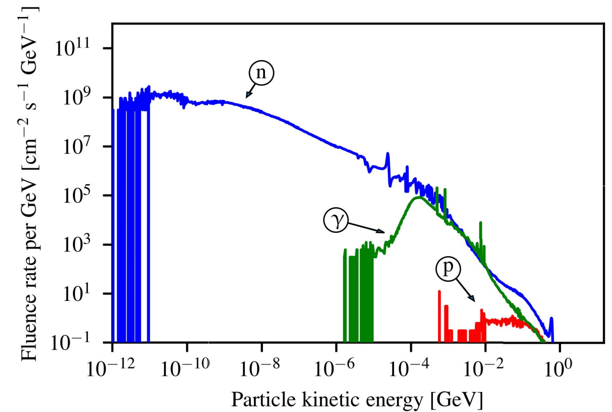

Fig. 17. Energy spectra of neutrons (n), photons (γ), and protons (p) at the digitizer-module locations in PANDA, as obtained from the PandaRoot simulation at an antiproton beam momentum of 1.5 GeV/c at a luminosity of 1×10^{31} cm^{-2} s^{-1}.

trajectories, as well as a polygon defining the locations of the digitizer boards on the plane.

The energy-differential fluence rates of neutrons, protons, and photons striking the digitizers are shown in Fig. 17. As the neutron fluence rate is considerably higher than the proton fluence rate, protons are not expected to be a concern with respect to SEUs. The photon fluence rate is comparable to that of neutrons and could, therefore, pose a risk. For a photon to cause an SEU, however, a photonuclear reaction in the device is required. The cross sections for photonuclear reactions are generally much smaller than those for nuclear reactions caused by protons or neutrons, as the interaction is purely electromagnetic [78]. For this reason, neither photons are expected to be a concern with respect to SEUs in the FPGA, and the expected SEU rate has been determined only for neutron-induced upsets.

The average neutron fluence rate $\langle d\Phi/dt \rangle$ through the digitizer board is given in Table VI, assuming an average luminosity of $\langle \mathcal{L} \rangle = 1 \times 10^{31}$ cm^{-2} s^{-1} and a $p\bar{p}$ total cross section of approximately 100 and 50 mb at 1.5 and 15 GeV/c

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TABLE VI
PREDICTED AVERAGE NEUTRON FLUENCE RATE IN PANDA AT THE LOCATIONS OF THE DIGITIZER BOARDS AT AN AVERAGE LUMINOSITY OF 1×10^{31} cm^{-2} s^{-1}

$\bar{p}$ momentum [GeV/c]	Average neutron fluence rate [cm^{-2} s^{-1}]
1.5	231
15.0	289

TABLE VII
PREDICTED RATE OF NEUTRON-INDUCED SEUS PER FPGA IN THE DIGITIZER BOARDS IN PANDA AT AN AVERAGE BEAM LUMINOSITY OF 1×10^{31} cm^{-2} s^{-1}

$\bar{p}$ momentum [GeV/c]	SEU rate [h^{-1}]	Mean time between upsets [h]
1.5	0.006	165 ± 38 [a]
15.0	0.008	123 ± 30

[a] Uncertainties correspond to one standard deviation.

beam momenta [79], respectively. The assumed luminosity is the average luminosity at the initial phase of operation of the PANDA experiment. It is foreseen that the experiment will eventually be operated at a luminosity ten times higher, which will affect the SEU rate accordingly.

The expected SEU rate R due to neutrons in PANDA was determined using

$$R = N_0 \int \sigma_{\mathrm{SEU}}(E_{\mathrm{n}}) \left\langle \frac{\mathrm{d}^2\Phi}{\mathrm{d}E_{\mathrm{n}}\,\mathrm{d}t} \right\rangle \mathrm{d}E_{\mathrm{n}}, \quad (12)$$

where N_0 is the number of bits in the FPGA configuration memory and $\langle \mathrm{d}\Phi/\mathrm{d}t \rangle$ is the average neutron fluence rate at the digitizers. The mean time between upsets (MTBU) per FPGA is the inverse of the SEU rate R. The predicted SEU rate and MTBU are shown in Table VII.

Fig. 17 shows that a considerable thermal-neutron fluence is expected in PANDA, which in reality may be even higher as some uncertainty in the simulation of thermal neutrons is expected. Thermal neutrons can cause SEUs in CMOS devices [80], mainly through neutron-capture reactions in the device. The probability for such reactions is very much dependent on the material composition of the device, and as the model presented here consists only of silicon, SEUs caused by thermal neutrons may not be properly accounted for. However, the main neutron-capture reaction causing SEUs is expected to be due to ^{10}B present in the device. For the Kintex-7 FPGA, the manufacturer has made modifications to the manufacturing process to reduce the effective thermal-neutron cross section drastically [8], [29].

As the EMC forward endcap will be equipped with 217 digitizer boards, each having two FPGAs, the MTBU for the whole detector may be determined from the values in Table VII. Based on these values, the MTBU for neutron-induced SEUs in the whole forward endcap at the initial luminosity is 23 min at a beam momentum of 1.5 GeV/c and 17 min at a beam momentum of 15 GeV/c. These are the MTBU values for any type of SEUs: correctable and uncorrectable. As the majority of upsets are correctable, it is foreseen that using the SEM core for error monitoring and correcting will be sufficient in combination with power cycling the module when uncorrectable SEUs occur. Although this will introduce dead time in some detector channels, it is negligible compared to the MTBU as a power-cycling operation of the whole digitizer board takes less than 1 s. At higher luminosities, more advanced forms of error mitigation, for example, triple modular redundancy, might be necessary. Also, the SEM core protects only the configuration memory of the FPGA and not, for instance, block memory. As such, additional measures such as triple modular redundancy may be necessary to protect those parts of the firmware design.

VI. CONCLUSION

In this article, a study of SEUs in the configuration memory of a 28-nm FPGA used in the forward endcap of the PANDA EMC has been presented. The cross sections for proton- and neutron-induced SEUs have been measured experimentally and agree with those of previous experiments. In addition, a Monte Carlo model of SEUs has been developed. This model can be seen as an extension to the commonly used RPP model and takes into account charge collection due to both drift and diffusion. The generation of charges close to the memory cell was determined from a Geant4 simulation of energy deposition in a small silicon volume. The two free parameters of the model, the sensitive volume side and the critical charge, were determined by fitting the model to the experimental data. The predicted parameter values are in agreement with values proposed by other authors, and the model-predicted SEU cross sections agree well with experimental data for both protons and neutrons. The model presented here is based on a greatly simplified memory-cell structure, as it, for instance, does not include any material other than silicon. Nonetheless, it presents a more physically correct picture than traditional models of SEUs, taking into account both charge drift and diffusion. In addition to good agreement on proton and neutron data, it is also shown to correctly predict the SEU cross sections for some heavy ions. There are some open questions with regard to low-energy protons, where there is no experimental data to either confirm or reject the model predictions.

This model relies on two free parameters—the critical charge Q_{crit} and the sensitive volume side d—which are directly feature-size-dependent, as well as on the availability of experimental data from irradiations. Therefore, adapting this model to FPGAs of feature sizes different than 28 nm should be possible by fitting to relevant experimental data and verifying the results against separate measurements. For the very latest FPGA devices, which are based on the finFET process technology and have feature sizes below 20 nm, the validity of the model will have to be verified.

Using additional Monte Carlo simulations of the radiation environment at the locations of the digitizer boards in PANDA during initial operation of the experiment, neutrons were found to be the main threat in terms of SEUs. Using the estimated neutron fluence together with the SEU model, the predicted mean time between neutron-induced upsets was found to be 165 ± 38 h per FPGA at a beam momentum of 1.5 GeV/c and 123 ± 30 h per FPGA at a beam momentum of 15 GeV/c.

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At such upset rates, it is estimated that continuously monitoring and correcting SEUs using the same firmware as during the experimental tests will be sufficient. In the event of an uncorrectable error, the digitizer board may be power cycled to correct the upset. This operation is assumed to introduce a negligible dead time in the detectors read out by the affected digitizer board. At higher luminosities, more advanced forms of error mitigation, for example, triple modular redundancy, may be necessary. Even at the initial phase of operation, such measures may be needed to protect other parts of the FPGA not covered by the built-in error monitoring firmware. The memory types not protected by the built-in tool are the block memory, distributed memory, and flip-flops of the FPGA [20]. These effects will have to be studied using a version of the FPGA firmware that includes all the features needed for operation in PANDA. In this process, the SEM core may be used to inject errors into the FPGA configuration [20], making it possible to evaluate the behavior of different parts of the implemented design.

The methods presented here have allowed for the determination of the energy dependence of the cross section for neutron-induced SEUs. As neutron-irradiation facilities typically produce neutrons with a wide energy spectrum, this dependence is not known generally. Once the model in this article has been fit to experimental data, the rate of SEUs in an arbitrary radiation field may be determined. As the model relies on rather simplifying assumptions regarding the memory-cell structure, an interesting field of further research would be to extend the model to even smaller feature sizes as well as to include a more realistic description of the material composition of the device. This could be of use in various applications, as the use of commercial FPGAs in different radiation fields is increasingly common.

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