

HIL Real-Time Simulation of a Digital Fractional Order PI Controller for Time Delay Processes

Cristina I. Muresan, Roxana Both, Eva H. Dulf, Adrian Neaga, Clara Ionescu

Abstract—Fractional order control has been used extensively in the last decade for controlling various types of processes. Several design approaches have been proposed so far, the closed loop performance results obtained being tested using different simulation conditions. The hardware-in-the-loop (HIL) real-time simulation offers a more reliable method for evaluating the closed loop performance of such controllers prior to their actual implementation on the real processes, such HIL simulation being highly suitable especially for complex, hazardous processes in which human and equipment errors should be avoided. The present paper proposes a hardware-in-the-loop real-time simulation setting for a digital fractional order PI controller in a Smith Predictor structure. The designed control strategy and fractional order controller is then tested under nominal and uncertain conditions, considering a time delay process.

I. INTRODUCTION

Fractional order calculus has been used intensively in the control of integer order plants [1-3], being considered to enhance the system control performance [4]. Several approaches regarding the design for fractional order plants have been developed, the great majority being tested through simulation using various case scenarios. In order to further implement such controllers, a more reliable real-time simulation is necessary. The present paper proposes a hardware-in-the-loop (HIL) real-time simulation of a Smith Predictor with a fractional order PI primary controller for a time delay process.

The HIL method chosen for the simulation of the closed loop control differs from pure real-time simulation by the addition of a real component in the loop. With this approach, the accuracy and efficiency of the controller can be tested directly on the real control unit, while the plant is simulated using various simulation environments. Very few HIL real-time simulation of fractional order controllers have been used so far [5]. In this paper, the hardware-in-the-loop setting is done with the process running on a PC, while the Smith Predictor structure and the digital fractional order PI controller is implemented on a National Instruments process computer.

The case study used in this paper is the liquid carbon monoxide level in a cryogenic carbon isotopes separation column. Such plants are very complex units that separate the

two stable carbon isotopes based on the distillation of carbon monoxide at extremely low temperatures ($\approx -194^\circ\text{C}$). A hardware-in-the-loop simulation of the control strategy is therefore highly suitable for such complex processes due to a number of reasons, such as cost reduction, shorter testing times and safety.

The paper is structured as follows. In Section 2, the case study used in this paper is presented. Section 3 offers a description of the HIL implementation of the Smith Predictor with a fractional order PI controller. Section 4 offers some real-time simulation examples, also considering various uncertain situations. The last section of the paper presents the concluding remarks.

II. CRYOGENIC CARBON ISOTOPE DISTILLATION PLANT

The carbon isotope cryogenic distillation unit is built at the National Institute for Research and Development of Isotopic and Molecular Technologies Cluj-Napoca (NIRDIMT-www.itim-cj.ro) [6], having the schematic representation as shown in Figure 1. The main components are: the distillation column (C), the condenser (C1) at the top of the column cooled with liquid nitrogen, the boiler (B) at the bottom of the column, and the vacuum jacket (M) - used for thermal isolation, since the column operates at very low temperatures. Thermal isolation is ensured by vacuum pumps (denoted PVP in Figure 1), while carbon monoxide is fed as a gas through a feeding system, at an intermediary point in the column, kept initially in a special reservoir (R). Manometers (M1, M2, M3) are installed at several points of the distillation column, to measure the pressures [7].

The distillation of carbon monoxide is the process that ensures the overall carbon isotopes separation. At very low temperatures, the carbon monoxide (CO) containing predominant ^{12}C has a different boiling point than the CO containing an increased ratio in the ^{13}C isotope. Thus, the ^{12}CO and ^{13}CO will coexist in the column in an ascending gaseous phase and a descending liquid form. Since the vapor pressure of ^{12}CO is higher than that of ^{13}CO , the ^{12}C isotope accumulates in the gaseous phase, being extracted as waste at the top of the column. The carbon monoxide enriched in ^{13}C accumulates in the liquid phase and is extracted as end-product at the bottom of the column [7]. Since the ratio of the vapor pressure is very close to unity, the separation of the carbon isotopes is very difficult to achieve. The column must operate at some very strict prescribed setpoints and all secondary processes involved must be controlled as well [8].

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Such secondary processes are for example the control of the liquid carbon monoxide level (h_b), the control of the top and bottom pressures, the control of the liquid nitrogen level that cools the gaseous ascending phase.

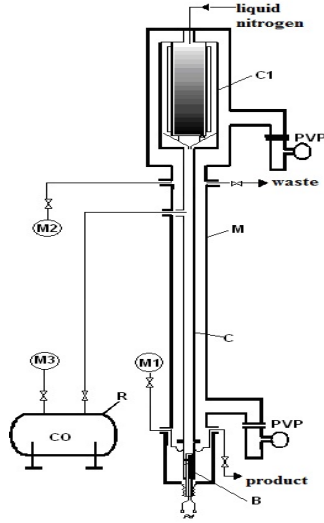


Figure 1. Schematic representation of the carbon isotope separation pilot plant

Maintaining a constant liquid carbon monoxide level (h_b) at the boiler of the column is of utmost importance, since it is based on the boiling of this quantity that the gaseous stream flow is produced. The entire separation process may be compromised if an excessive boiling of the liquid carbon monoxide is performed, generating a gaseous stream flow close or over the value of maximum column capacity. Such phenomenon leads to the column flooding [9], with serious disadvantages regarding the efficiency of the carbon isotope separation process and leading to an end-product of poorer concentration. The liquid carbon monoxide level depends upon the carbon monoxide feed flow into the column, the carbon monoxide waste flow from the column and the electrical power supplied to the boiler. To control the liquid carbon monoxide level the manipulated input is the carbon monoxide feed flow, while the waste flow and the electrical power are maintained constant. Thus the simplified transfer function of the process, identified using experimental data [10], is given as:

$$G(s) = \frac{0.00148}{s^2 + 0.154s + 0.00435} e^{-8s} \quad (1)$$

III. HIL STRUCTURE OF THE SMITH PREDICTOR CONTROL STRATEGY WITH FRACTIONAL ORDER PI CONTROLLER

The closed loop control scheme is given in Figure 2, where $G(s)$ is the rational part of the transfer function in (1), $G_0(s)$ is the nominal model of $G(s)$, τ is the process time delay and τ_0 is the nominal value of the delay and C_{FO-PI} is the fractional order PI controller. The choice of the Smith Predictor is based on its inherent time delay compensation

features, enabling the design of the controller based solely on the time delay free model of the process transfer function.

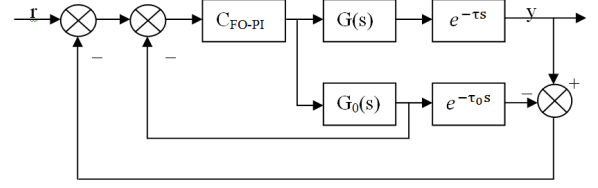


Figure 2. Smith Predictor with fractional order PI controller

The design of the fractional order PI controller is based on two performance specifications: the open loop phase margin (φ_m) and gain crossover frequency (ω_{cg}) [10]:

$$\omega_{cg} = 0.01 \text{ and } \varphi_m = 60^\circ \quad (2)$$

The robustness condition that ensures the performance measures in (2) may be written as:

$$G_0(j\omega_{cg}) e^{-j\omega_{cg}\tau_0} C_{FO-PI}(j\omega_{cg}) = -e^{j\varphi_m} \quad (3)$$

Equation (2) may be rewritten as:

$$G_0(j\omega_{cg}) C_{FO-PI}(j\omega_{cg}) = -e^{j(\varphi_m + \tau_0\omega_{cg})} \quad (4)$$

Using the fractional order PI controller transfer function:

$$C_{FO-PI}(s) = k_p + \frac{k_i}{s^\lambda} \quad (5)$$

the parameters may then be obtained using:

$$k_p + \frac{k_i}{(j\omega_{cg})^\lambda} = -\frac{e^{j(\varphi_m + \tau_0\omega_{cg})}}{G_0(j\omega_{cg})} \quad (6)$$

Solving (6) for k_p and k_i , yields:

$$k_p = -\Re(X_{sp}(j\omega_{cg})) - \cot\left(\frac{\pi}{2}\lambda\right) \Im(X_{sp}(j\omega_{cg})) \quad (7)$$

$$k_i = \frac{\omega_{cg}^\lambda}{\sin\left(\frac{\pi}{2}\lambda\right)} \Im(X_{sp}(j\omega_{cg})) \quad (8)$$

$$\text{where } X_{sp}(j\omega_{cg}) = -\frac{e^{j(\varphi_m + \tau_0\omega_{cg})}}{G_0(j\omega_{cg})}.$$

However, k_p and k_i in (7) and (8), respectively, are given as a function of the fractional order λ . In order to completely define the fractional order PI controller in (5), an adequate value of the fractional order λ must be found. Classical design methods for FO controllers imply the use of optimization techniques, such as Matlab's `fmincon`

function, with significant drawbacks in terms of convergence. Instead, the authors choose an algorithm that automatically selects the fractional order λ which maximizes the open loop gain margin [10]. Figure 3 shows the output of the algorithm, with the open loop gain margin as a function of λ .

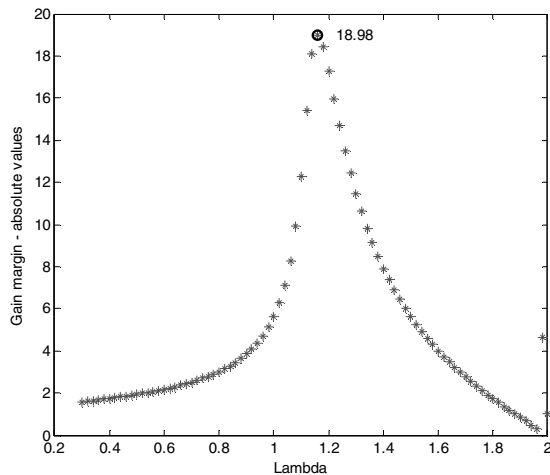


Figure 3. Open loop gain margin as a function of the fractional order λ

The result in Figure 3 shows that the maximum open loop gain margin is achieved with $\lambda=1.16$, thus a controller tuned with such a fractional order would exhibit a higher robustness to gain variations than any other fractional order PI controller. For $\lambda=1.16$, the remaining fractional order PI controller parameters in (7) and (8) [10]:

$$k_p = 0.511 \text{ and } k_i = 0.0155 \quad (9)$$

To simulate the closed loop scheme from Figure 2 in a real time hardware-in-the-loop setting a NI PXI-8183 process computer is used. NI PXI-8183 is one of the National Instruments products by integrating processing and connectivity technologies on the market. Among the integrated technologies are included: analog to digital converter (ADC), digital to analog converter (DAC), counters, etc. The embedded system consists of the following modules: NI PXI-6722, NI PXI-6220, NI PXI-6221. Module NI PXI-6221 was chosen to implement the controller, due to the fact that it has both analog and digital inputs and outputs.

The hardware-in-the-loop configuration of the closed loop scheme with Smith Predictor and fractional order PI controller is given in Figure 4, while the fractional order PI controller implementation scheme using LabVIEW environment is given in Figure 5. In order to obtain the desired HIL structure the controller is implemented and runs on the NI PXI-8183 process computer while the process is implemented and executed on a personal computer. Both implementations are done using the National Instruments LabVIEW environment.

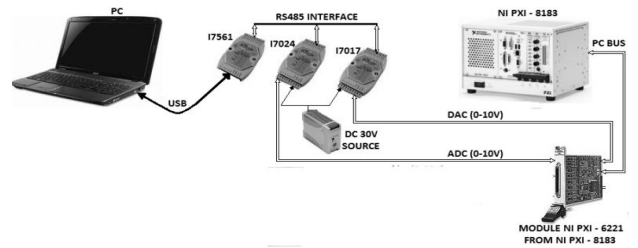


Figure 4. Hardware-in-the-loop closed loop configuration

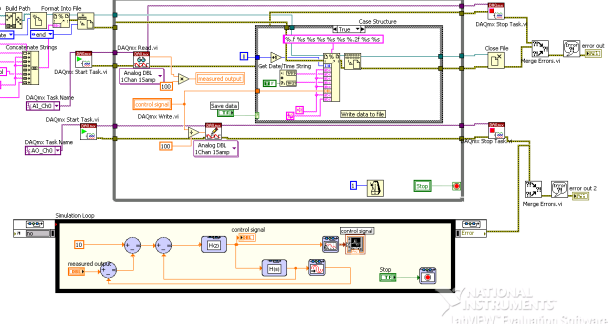


Figure 5. Block Diagram of the controller implementation using LabVIEW

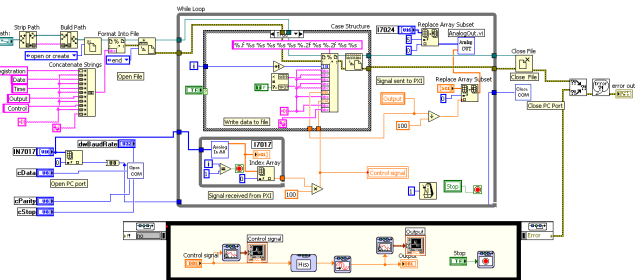


Figure 6. Block Diagram of the process implementation using LabVIEW

The measured output is received using NI PXI-6221 module channel AI_Ch0, defined in Measurement and Automation Explorer (MAX). This component of LabVIEW is used to manage devices and interfaces, virtual channels or tasks. In the upper part of the diagram data save operation is performed. Before the While loop is started in the upper right side a .txt file is opened where the data, representing the control signal, will be saved. The Case structure performs the log and the save functionality. The obtained control signal is sent to the process using NI PXI-6221 module channel AO_Ch0.

Figure 6 presents the block diagram of the LabVIEW process implementation. The control signal is acquired, from the NI PXI-8183 on to the personal computer using the data acquisition modules ICP/CON I-7000. After the control signal is applied to the process, the obtained output signal of the process will be sent to the NI PXI-8183 using the same data acquisition modules. Also, like in the controller block diagram, data save operation is performed which can be observed in the upper part of the diagram. In this case are saved the control signal and the measured output values.

The main reasons for LabVIEW implementation of the

hardware-in-the-loop configuration are: it is a graphic environment for fast implementation of measurement, testing and control applications and it presents several advantages regarding data acquisition, processing when installed on embedded systems like NI PXI-8183 process computer.

IV. REAL-TIME HARDWARE-IN-THE-LOOP SIMULATION RESULTS

The fractional order PI controller in Figure 5 is implemented in its digital form using the recursive Tustin discretization method [11].

Figure 7 shows the closed loop system response to a step change of 10% in the reference signal considering various sampling times for the discretization of the fractional order integrator, using recursive formulas of order 5 and 9, respectively. The simulation was performed using Matlab programming environment, with a step change in the reference signal occurring at 10 minutes simulation time. The simulations show that more accurate results are obtained using a higher order recursive discretization formula and a lower sampling time. For higher sampling times and lower order of discretization, the performance specifications are not met.

The digital fractional order PI controller implemented on the PXI was obtained using a 9th order recursive approximation formula and a sampling time of 0.01 minutes. Figure 8 shows that the closed loop simulation results using the hardware-in-the-loop setting are similar to the results obtained using Matlab. The step change in the reference signal occurs at the beginning of the simulation time.

The robustness of the fractional order PI controller is then tested considering [-50%, +50%] variation of the process time delay. The real-time hardware-in-the-loop simulation results are given in Figure 9, considering a step change in the reference signal at 10 minutes simulation time. The results show that the control strategy ensures a robust performance of the closed loop system, with the settling time and the overshoot maintained below the imposed specifications.

V. CONCLUSIONS

The fractional order controller has been specifically designed to ensure an increased robustness even for significant time delay variations. The simulation results in Matlab show that the closed loop system meets the imposed performance criteria, however prior to the actual implementation of the fractional order PI controller, a more reliable testing is required.

The hardware-in-the-loop real-time simulation offers significant advantages over classical simulation since the

fractional order PI controller and the Smith Predictor structure are implemented on the actual process computer. Using this simulation method, the control strategy is tested directly on the process computer in a more realistic setting.

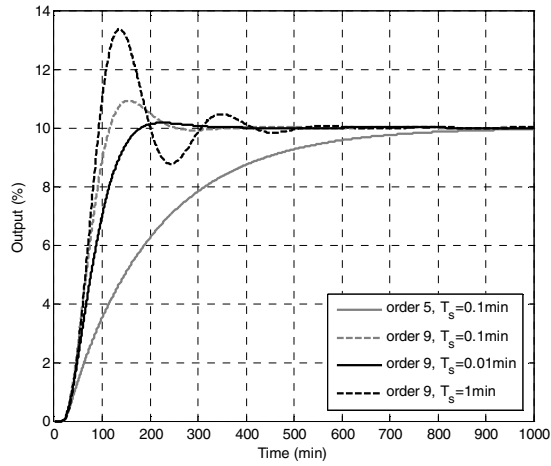
The hardware-in-the-loop real-time simulation results, similar to those obtained using Matlab, show that the designed control strategy can be further used in a real process control loop. The simulation results also prove that the designed controller can meet the imposed performance criteria even for significant time delay variations.

ACKNOWLEDGMENT

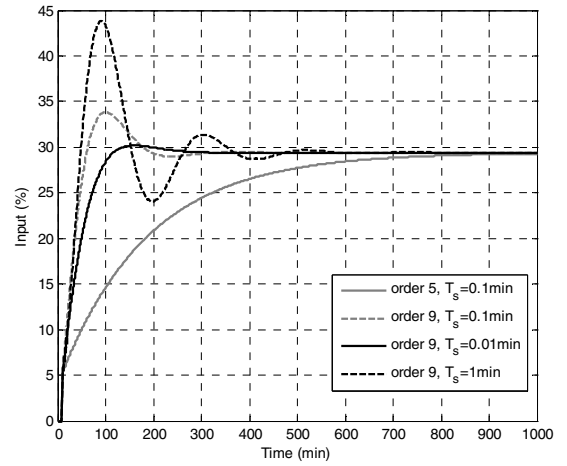
This work was supported by a grant of the Romanian National Authority for Scientific Research, CNCS – UEFISCDI, project number PN-II-RU-TE-2012-3-0307.

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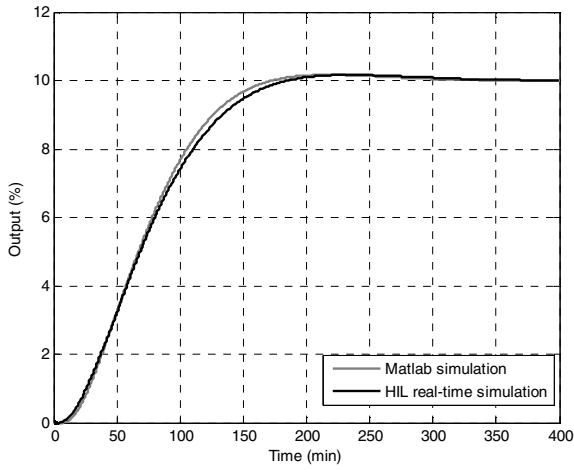


a)

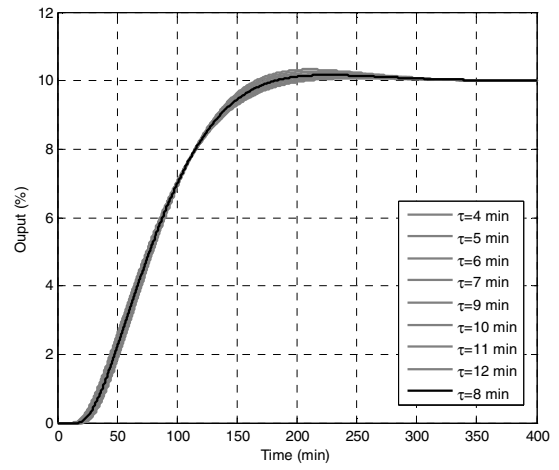


b)

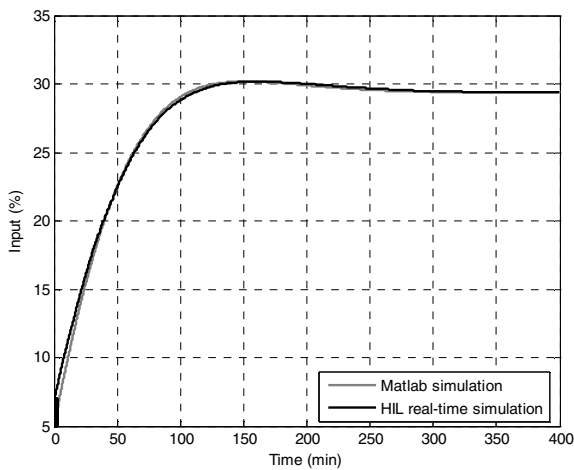
Figure 7. Closed loop simulation results using digital fractional order PI controller a) Output signal b) Input signal



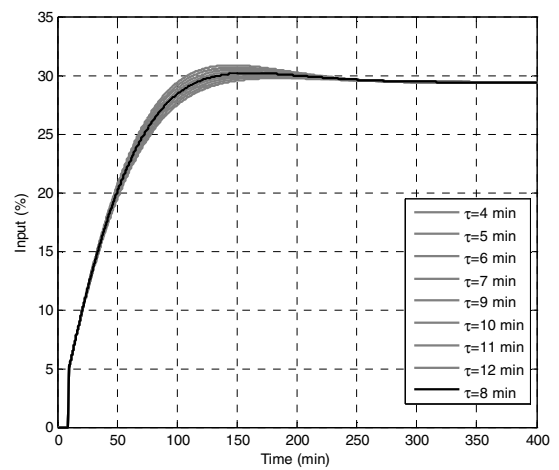
a)



a)



b)



b)

Figure 8. Matlab and HIL real-time simulation results a) output b) input

Figure 9. HIL real-time closed loop simulation results considering $\pm 50\%$ variation of the process time delay a) output b) input