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Electronic-Photonic Integration in the Helios Project

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ABSTRACT

Different ways of integrating of integrating photonics and electronics at the wafer level scale are reviewed: Monolithic, Back-Side, and Front-Side integration. Type and volume applications are selection criteria.

DEMONSTRATOR FOR HELIOS PROJECT

By co-integrating optics and electronics on the same chip, high-functionality, high-performance and highly integrated devices can be fabricated with a well-mastered microelectronics fabrication process. The photonics chips with active devices are connected to electronics drivers or amplifiers and therefore the integration challenge of silicon photonics with microelectronic circuits has been studied for a long time. Different integration schemes have been studied and developed, each with its own merits which are often application specific: Biosensing and high performance computing systems will not necessarily share the same integration schemes as the specifications and the system packaging differ strongly.

If we consider chip-to-chip or die-to-wafer connections, mature technologies such as wire bonding, stud bumping, and flip-chipping are available. The silicon photonics circuit can then be considered as a board where the different subcircuits are attached (laser diodes, drivers, photodetectors, transimpedance amplifiers, etc…). The FP7 HELIOS project focused on the integration at wafer level for either higher performance (reduction of the parasitics) or higher miniaturization. Three main integration avenues have been studied by different partners in the project.

ABOVE IC FABRICATION OF A WDM RECEIVER

The IMEC front side integration scheme is based on 3-D stacking: the photonics die with optical inputs, outputs and an 8/16 channel arrayed Waveguide Grating (AWG) demultiplexer is positioned face-up on an electronics die, and uses through-silicon-vias (TSV) through the thinned photonics substrate for electrically connecting with both dies. Figure 1 shows a schematic cross section of such scheme of integration, and a cross section of the copper-filled TSV. This integration includes postprocessing on the photonic and the CMOS wafer with trans-impedance amplifiers (TIA), which is fabricated by AMS in a .25µm process. The postprocessing goes in parallel, until assembly for integration. In this particular case, an additional III-V integration step for InGaAs photodetectors is performed after the 3D stacking.

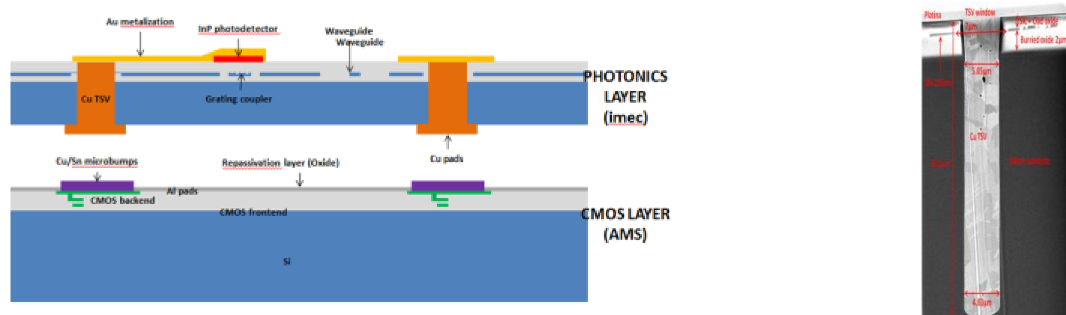

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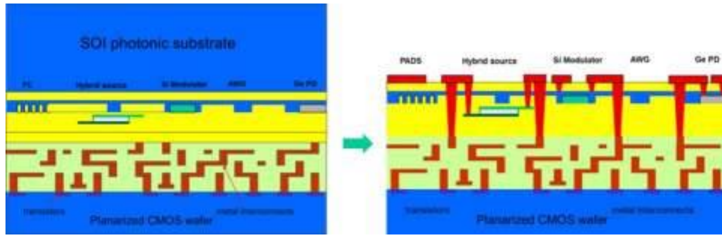
Figure 1: Photonic-electronic integration with TSVs. Left: integration scheme. Right: Cross section of TSV in photonic wafer.

The LETI integration is based on wafer-to-wafer bonding at the last levels of metallization with subsequent processing of the final metallization to connect the photonic devices with the underlying CMOS. The SOI photonic wafer with AWG demultiplexer and Ge-based receivers is processed with a full photonic frontend and backend [1]. In parallel, the AMS-fabricated CMOS is planarized by a deposited oxide coating and chemical mechanical polishing (CMP). Similar oxide cladding and planarization is performed on the photonic wafer, and both wafers are perfectly cleaned for molecular bonding at room temperature (Fig 3).



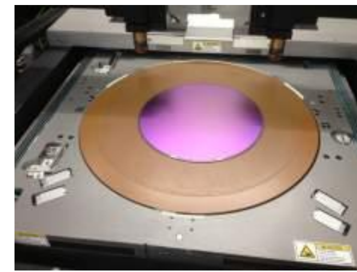


Figure 2: Bonding of the two wafers and connections of TIA to Ge PD

Figure 3: The two wafers after bonding

The substrate of the photonic SOI wafer is then removed by grinding and chemical etching of Si, stopping on the buried oxide (BOX) interface. On this stack the electrical interconnects between the CMOS and the photonic wafer are processed, using silica etching followed by metal deposition and etch (fig 2). The alignment precision between the CMOS and the photonic wafer is of the order of ±2 µm.

FRONTEND INTEGRATION WITH HIGH-PERFORMANCE BICMOS

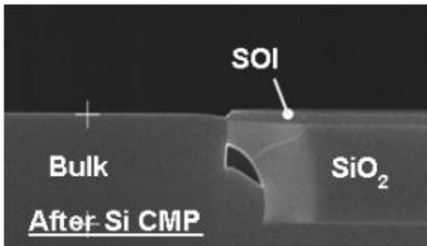


Figure 4: Photonic-Electronic substrate

otonic integration in the frontend of BiCMOS is hampered by strong compatibility of substrate requirements of photonics and of bipolar transistors. P therefore developed the so-called local-SOI approach for a novel photonic CMOS process. The process start with an optical SOI substrate with dimensions r buried oxide and top-Si layer optimized solely for photonic application, without y regard to BiCMOS requirements. Then top-Si layer and buried oxide are moved by a sequence of RIE and wet etch steps from those wafer or chip areas reseen for BiCMOS device fabrication. Etched areas are then re-filled by selective Si epitaxy and planarized by chemical mechanical polishing (CMP) (figure 4). The process sequence for a fully fetched integration of silicon photonic modulators and driver electronics was developed and successful operation of a modulator with BiCMOS drivers was achieved at 10G.

BACKSIDE FABRICATION OF THERMO-OPTIC DRIVEN RING RESONATORS

Instead of having the photonics and electronics on the same side of the wafer, it is also an option to accommodate them at opposite sides. In Fig 5, a schematic cross section is depicted for backside-fabricated photonics. The concept is based on photonic-wafer to CMOS-wafer bonding and TSVs through the CMOS backside. For this, both the photonic and CMOS wafer are planarized up to the top metal. The CMOS wafer is thinned to 250µm and the photonic wafer front side is bonded to the CMOS backside. Then TSVs are processed through deep reactive ion etching, dielectric deposition and patterning, and TSV. Then the CMOS is finished with top metal and passivation. Finally, the handling wafer of the SOI is removed. As test vehicle, we fabricated rings resonators with heaters on the photonic layers and on the CMOS wafer only last level of metallizations and the TSV were performed. Fig. 6 (left) shows TSV with their connections to external pads, and Fig 6 (right) shows a ring resonator with a Ti/TiN heater connected to the TSVs.

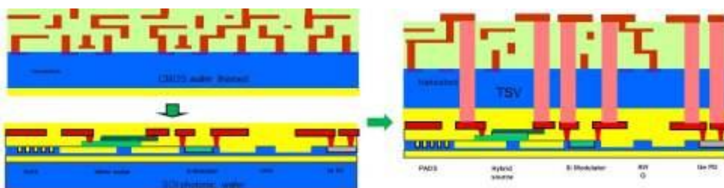


Fig: 5: Back side integration concept

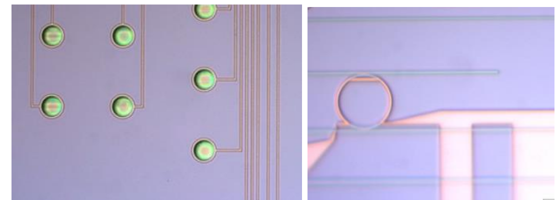


Fig: 6 (left) Front and (right) Back Side of the assembled PEIC wafer

CONCLUSION

This integration work showed to the potentiality of photonic and electronic integration at the wafer scale. Figures of merit are discussed in [2].

AKNOWLEDGMENT

The research leading to these results has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 224312 HELIOS.

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