

# Silicon CMOS Photonics Platform for Enabling High-Speed DQPSK Transceivers

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## ABSTRACT

In this work we review the results obtained under the framework of FP7-HELIOS project for integrated DQPSK transceivers in silicon photonics. A differential DQPSK receiver with balanced zero biased Germanium photodiodes has been demonstrated at 10Gbit/s with an error floor around  $10^{-15}$ . Furthermore, DPSK modulation up to 10Gbit/s with a bit error rate below  $10^{-9}$  is also demonstrated using a silicon push-pull operated dual-drive Mach-Zehnder modulator (MZM) based on carrier depletion. The results indicate the potential of the silicon CMOS photonics platform for boosting next-generation optical networks based on advanced modulation formats.

**Keywords:** photonic integrated circuits, silicon photonics, optical transceivers, modulation, DQPSK.

## 1. INTRODUCTION

An ever growing amount of access network bandwidth is required by end users, and the deployment of passive optical networks, operating up to 10 Gbit/s has already begun to address this demand [1]. Higher bit rates will probably be required in the future, with network operators preferring solutions based on reusing the existing infrastructure and components developed for legacy links. Therefore, advanced modulation formats allowing to scale the bit rate while keeping the use of narrow bandwidth devices are highly desirable. One of the most promising approaches is based on phase-shift keying (PSK) modulation formats, which offer a greater flexibility to achieve higher spectral efficiencies when compared with traditional on-off keying (OOK) modulation. Silicon photonics technology has attracted a great deal of attention during the last years due to its high index contrast and compatibility with complementary metal oxide semiconductor (CMOS) processes thus allowing high density optical circuit layouts and monolithic integration with electronics. Hence, silicon photonics is expected to provide an excellent platform for enabling the low-cost, low-power and highly-scalable photonic integrated circuits (PICs) required for deploying next generation optical transceivers.

In this paper, we review the results obtained under the framework of FP7 HELIOS project for developing 10Gbit/s differential quadrature phase-shift keying (DQPSK) transceivers in silicon photonics for optical access networks [3]. Differential detection could provide significant savings in cost and power consumption compared with coherent detection solutions thus making it more suitable for access networks. Different approaches have been proposed for achieving differential silicon receivers, mainly based on the use of standard Mach-Zehnder delay interferometer (MZDI) [3] or using microring resonators [4]. While the ring resonator approach allows a very compact implementation, optimal performance usually requires a tuning mechanism, increasing the complexity and power consumption of the receiver. On the other hand, DQPSK modulation has also been proposed based on silicon Mach-Zehnder modulators (MZM) and ring-based modulators. In the latter, unique features in terms of small footprint and low drive voltage are achieved but they suffer from a low optical bandwidth making thermal control elements also necessary [5]. Therefore, the MZM approach has been chosen as a more robust solution and with the potential of higher operation speeds. Very recently, 112Gbit/s dual-polarization QPSK modulation based on silicon nested MZM has been demonstrated for optical transport networks [6,7].

## 2. DQPSK RECEIVER

The DQPSK differential receiver is depicted in Fig. 1. The proposed device was fabricated on top of a 200-nm SOI wafer with silicon core thickness of 220 nm and buried oxide of 2  $\mu$ m. The process starts with the deposition of 100 nm High Temperature Oxide (HTO) on top of the silicon layer. To couple light from the input

fiber to the receiver, and in order to minimize the size of the chip, curved gratings were used with a coupling loss of about 6 dB. The gratings and the waveguide arms are first patterned, followed by RIE silica etching with  $C_4F_8$ , which defines a hardmask. The silicon is then partially etched (65 nm) with HBr and controlled by ellipsometry in order to define precisely the grating teeth depth. In the second lithography step, the gratings are protected by the resist and the remaining hardmask serves for the waveguides in a self-alignment process. Then a full silicon etch down to the box completes the waveguide fabrication. We then defined cavities for the selective epitaxial growth of Germanium (Ge). This is achieved by deposition of a silica layer which is etched at the end of waveguides. In order to achieve direct coupling, the silicon part of the cavities is etched down to 50 nm on top of the BOX. Germanium was then selectively grown in the cavities and chemical-mechanical planarization (CMP) used to adjust the thickness around 300nm. The doped regions (N and P) of the lateral Ge photodetector are defined sequentially by ion implantation of Phosphorus and Boron. A 400 nm thick  $SiO_2$  was deposited and a deposition and etching of 100 nm of Ti/TiN defined the heaters. Then after deposition of 500 nm of  $SiO_2$  and two-step openings, the electrodes were defined by Ti/TiN/AlCu metal stack deposition and Cl2 etching.

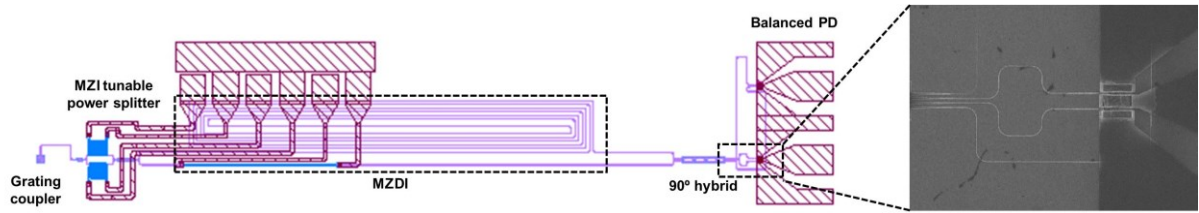


Figure 1. 10 Gbit/s DQPSK differential receiver and SEM image of the Ge-PD.

The different building blocks of the receiver are depicted in Fig. 1(a). A thermo-optically tunable MZI power splitter was first used before the Mach-Zehnder delay interferometer (MZDI). In case of unbalanced behaviour at the output of the MZDI due to excess loss in the delay line, micro-heaters can be used to actively tune the power at the MZDI input, resulting in an increase in the extinction ratio of the MZDI [8], and consequently in the sensitivity of the receiver. At the output of the power splitter, the MZDI was placed. A waveguide length of 18 mm was required for 10 Gbit/s operation. Therefore, compact spirals were used in order to minimize the size of the structure. The propagation losses in the MZDI were about 3dB. The MZDI outputs were coupled to a  $2 \times 4$  Multimode Interference (MMI) acting as  $90^\circ$  hybrid, with an insertion loss of about 6.5 dB [9]. In order to have a 3 dB increase in the sensitivity of the receiver and minimize power consumption, zero bias balanced detection was used based on a Germanium photodetector pair (Ge-PD) in lateral *pinpin* configuration [10]. A scanning electron microscope (SEM) image of the  $10\mu\text{m}$ -length Ge-PD is shown in the right side of Fig. 1. The responsivity was measured to be 1 A/W at 1550 nm using 0 to -2 V bias. The total optical excess loss of the receiver was around 15 dB.

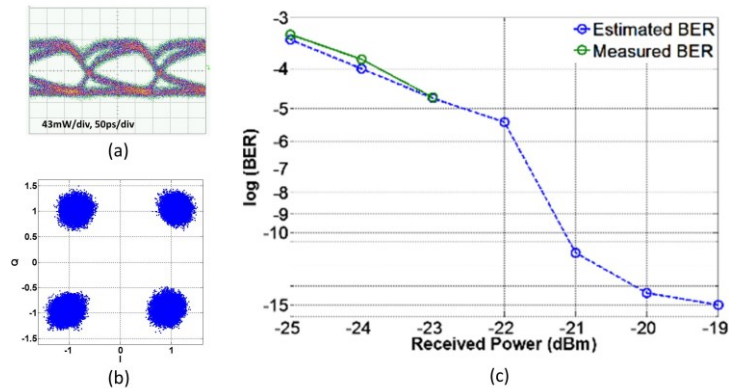


Figure 2: (a) DQPSK eye diagram; and (b) symbol constellation for a received power of -19dBm; (c) Measured and estimated BER versus received power.

For characterizing the receiver, a 10 Gbit/s DQPSK signal was generated using a commercial single-drive Lithium Niobate nested MZ modulator, biased at minimum transmission and driven by the outputs of the pulse pattern generator (PPG), appropriately decorrelated, aligned and amplified at  $2V_\pi$ . The bits were generated from a pseudorandom binary sequence pattern generator (PRBS) with a pattern length of  $2^{13}-1$ . Well opened eye-diagrams and remarkably good constellation diagrams were obtained, as shown in Fig. 2(a)-2(b) for a received power of -19 dBm. The error vector magnitude (EVM) as well as the bit error rate (BER) as a function of the received power was measured. However, as the quality of the received signal was quite good so that no significant amount of errors were recorded in the captured length of the data, which was 100k symbols, the EVM

of the signal was used to estimate the BER for received powers above -23 dBm. Figure 2(c) shows the measured and estimated BER. It should be noticed that for input powers lower than -21 dBm, the erbium doped fiber amplifier (EDFA), used for counteract insertion losses, was no longer able to amplify the signal to a constant output power value of +16 dBm, and lower powers reach the balanced photodiodes. Even so, an error floor value of around  $BER = 10^{-15}$ , which corresponds to a  $EVM = 12.5\%$ , was obtained confirming the excellent performance of the proposal DQPSK receiver for 10Gbit/s operation.

### 3. DPSK TRANSMITTER

The DPSK modulator is depicted in Fig. 3. MMI were used as input/output 3 dB couplers. The silicon waveguide core has also a height of 220 nm, a width of 450 nm, and a slab thickness of 100 nm, as depicted in Fig. 3(c). Optical phase modulation is achieved by depleting the majority carriers from a reverse biased pn junction with doping concentrations of  $1.6 \cdot 10^{17} \text{ cm}^{-3}$  in the p-type region and  $8 \cdot 10^{17} \text{ cm}^{-3}$  in the n-type region. The fabrication process is based on a self-alignment process described in Ref. [11]. The travelling-wave electrodes are formed by depositing a compound AlCu layer on top of highly doped p+ and n+ regions with concentrations of  $1 \cdot 10^{20} \text{ cm}^{-3}$ . A dual-drive electrode configuration was chosen for push-pull operation.

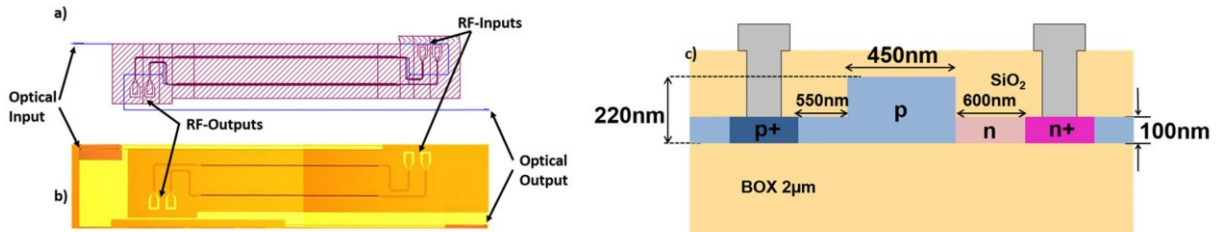


Figure 3. DPSK modulator: (a) GDS design, (b) optical photograph of fabricated device and (c) cross-section of the pn junction.

The DPSK modulator was firstly characterized in DC. Different voltages were applied to the MZM and extinction ratios as high as 30 dB were achieved under these DC conditions. A  $V_{\pi}$  value of 12 V was measured, which for the 3 mm modulation length gives rise to a  $V_{\pi} \cdot L$  product of 3.6 V·cm. The insertion loss, including phase shifter and MMI losses, was about 10 dB. Next, the high speed operation of the modulator was characterized. Digital data signals were generated from a pseudorandom binary sequence pattern generator with a pattern length of  $2^7 - 1$ , delivered by a bit pattern generator (BPG) connected to an external clock. The signals were appropriately decorrelated and aligned before being fed to the electrodes with 8 V peak-to-peak voltage. A double RF signal probe with GSGSG configuration was used to drive the MZM, while another double RF signal probe with 50 ohm terminators was applied at the electrode output (see Figs. 3(a)-3(b)). A reverse DC bias was applied to the phase shifters for operation in carrier depletion.

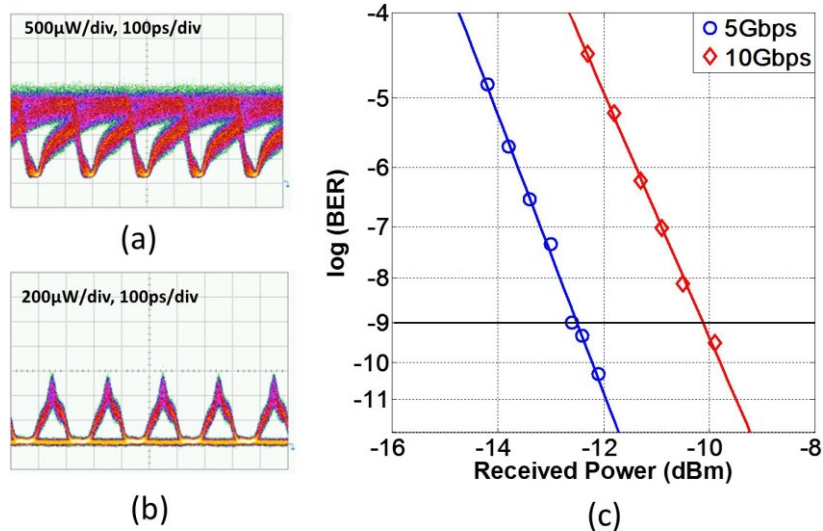


Figure 4. DPSK (a) modulated and (b) AMI demodulated eye diagrams; (c) Measured BER versus received power for 5 Gbit/s and 10 Gbit/s DPSK demodulation.

In order to measure the bit error rate (BER), the optical DPSK modulated signal was passed through an external demodulation circuit based on a polarization delay-interferometer [12]. The measured eye diagram of the modulated DPSK signal at 5 Gbit/s is shown in Fig. 4(a). The noise is mainly due to the limitation in the

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drive voltage which is not high enough to achieve  $V_\pi$  in each phase shifter of the MZM (the driver only offers 66.6% of the required  $V_\pi$ ). However, as digital data information is in the phase of the optical signal, clear eye diagrams were obtained after demodulation, as demonstrated in Fig. 4(b), which shows the alternate-mark inversion (AMI) demodulated eye diagram. The performance of the DPSK modulator was further evaluated by measuring the BER. As shown in Fig. 4(c), error-free (BER <  $10^{-9}$ ) DPSK modulation for 5 Gbit/s is obtained. Furthermore, higher data rates were also tested to characterize the high-speed performance of the modulator. Error-free DPSK modulation was also achieved for 10 Gbit/s with a power penalty of around 2 dB, as shown in Fig. 4(c). DPSK modulation up to 20 Gbit/s was also successfully achieved though it was not possible to measure the BER due to a limitation in the experimental set-up. However, DPSK modulated eye diagrams clearly showed that inter-symbol interference (ISI) did not occur, which confirms the high speed operation of the modulator. Remaining challenges are the reduction of the  $V_\pi$  value as well as insertion losses.

#### 4. CONCLUSIONS

A compact differential DQPSK receiver with zero biased balanced photodetection has been demonstrated at 10 Gbit/s. Furthermore, a dual-drive silicon MZM has also been successfully demonstrated to operate at such data rate. The DQPSK transmitter would be achieved by arranging the MZM in a nested configuration. The results clearly confirm the potential of silicon photonics technology for developing low-power consumption and cost-effective integrated DQPSK transceivers for next-generation optical access networks.

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