Amorphous silicon: For Advanced Photonic Integrated Circuits

Shankar Kumar Selvaraja

Supervisor(s): Dries Van Thourhout, Roel Baets

I. Introduction

Silicon photonics has emerged as one of the matured integrated photonics technology platforms. The ability to scale-down the size of the circuit; thanks to high refractive index and further more using the existing microelectronics fabrication facility for high volume production. In addition, various functionalities, such as, compact wavelength filters, high-speed modulators, hybrid lasers were developed in order to exploit silicon. However, all these developments relied on crystalline silicon. In spite of its superior material quality, crystalline silicon restricts innovation and integration possibilities. In this paper I present an alternative material technology to encounter the limitations of crystalline silicon without much compromise on the advantages of crystalline silicon.

II. Amorphous silicon

Amorphous silicon is one of the material phase (allotropy) of silicon, where the silicon network at disordered unlike crystalline silicon which has ordered Si atom arranged in tetrahedral structure. Initially developed for microelectronics and solar cell applications, distinct electrical and optical properties are now being explored for wider applications, including integrated photonics. In integrated photonics amorphous Si is deposited as thin layer on a substrate at relatively low temperatures (20-400^{o}C). The low temperature depositions is necessary to maintain the amorphous nature of the material unless it will be crystallized forming polycrystalline silicon. Plasma enhanced chemical vapour deposition is a popular microelectronics fabrication process by which amorphous silicon can be deposited. Figure 1 shows the deposition chamber with which amorphous silicon is deposited. The film is deposited by breaking down silicon containing gas(silane-SiH_4) in presence of a dilution gas(Helium). There are various deposition parameters which can be tuned to modify the film properties. Various material properties such as, density, stress, optical absorption, and crystallinity can be tuned. For photonic application low optical absorption is one of the prime requirement to achieve low-loss photonic circuits. Thus, the process parameters were tuned to achieve low-loss amorphous.

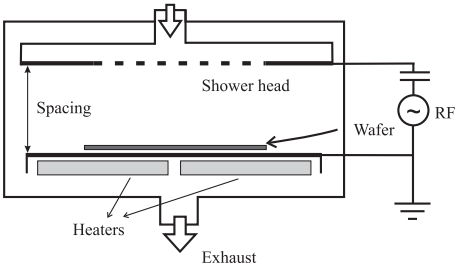

Figure 1. simul.

III. Photonic devices in amorphous silicon

To demonstrate the viability of the deposited amorphous silicon for integrated photonics we have fabricated photonic devices in it. Fig-

S. Selvaraja is with the Information and telecommunication Department, Ghent University (UGent), Gent, Belgium. E-mail: shankar@intec.ugent.be .

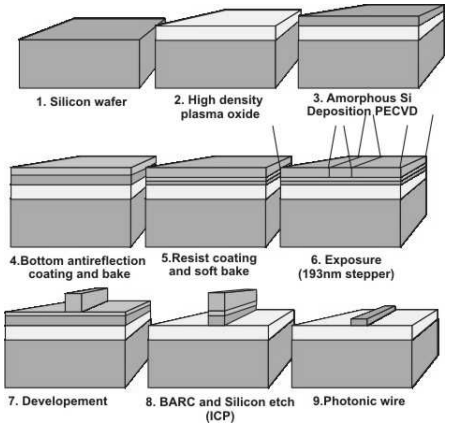

Figure 2. simul.

ure 2 illustrates the process flow for fabricating photonic devices in amorphous silicon. The devices were fabricated using high volume microelectronics fabrication facility at IMEC, Leuven. All the processing were performed on a 200 mm silicon wafer to demonstrate the viability for industrial deployment of this process. To demonstrate the low-loss nature of the deposited material, waveguides were fabricated with varying length to characterize the propagation loss. we demonstrated a propagation loss of 3.45 dB/cm was achieved for high confinement waveguide of 480 nm wide and 220 nm thick [2]. This is lowest propagation loss reported for this dimension.

A. *Single layer circuit: wavelength selective devices*

Apart from waveguides we have also fabricated wavelength selective devices such as, ring resonator filters and mach-zhender interferometers. The devices were fabricated as shown in fig. 2. A broad band light is couple in and out the chip using a grating fiber coupler. The light output is measured using a spectrum analyzer to characterize the spectral response of the devices. Figure 3 shows the spectral response of one of the mach-zhender interferometers.

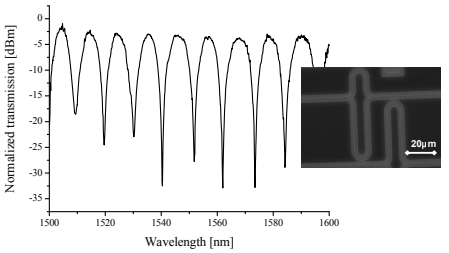

Figure 3. simul.

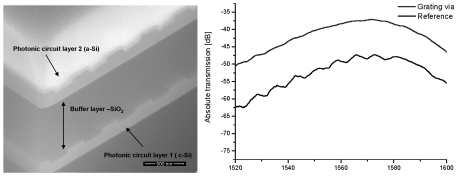

Figure 4. simul.

B. *Multilayer circuit: Optical via's*

To take real advantage of the deposited silicon, double layer photonic circuit was fabricated. In order to coupled both the layers gratings were used to coupled light between the layers. The process flow shown in fig. 2 was used to define the first layer and the next layer is defined by repeating step 2-9. Figure 4 shows the cross section of the fabricated optical via and the transmission spectrum of an optical via. we have measured an efficiency of 11% experimentally, while simulations shows that the efficiency can be increase to 50 %.

IV. Conclusions

Acknowledgments

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References

[1] S. K. Selvaraja, et al., "Low-loss amorphous silicon-on-insulator technology for photonic integrated circuitry," Optics Communications, vol. 282, pp. 1767-1770, 2009.