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Hands-On Tutorial

Coarse-Grained Reconfigurable Architectures - Compilation and Exploration

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ABSTRACT

CGRAs consist of an array of a large number of functional units (FUs) interconnected by a mesh style network. Register files are distributed throughout the CGRAs to hold temporary values and are accessible only by a subset of FUs. The FUs can execute common word-level operations, including addition, subtraction, and multiplication. CGRA processors accelerate inner loops of applications by exploiting instruction level parallelism (ILP) and in some cases also data-level and task-level parallelism (DLP & TLP).

The aim of this tutorial is to give insight in CGRA architectures, their compilation techniques, and to experience first hand how to do source code mapping on a CGRA. Therefore the tutorial consists of presentations as well as a hands-on session.

Categories and Subject Descriptors

C.1.4 **[Computer Systems Organization]**: Processor Architectures – parallel architectures.

General Terms: Performance, Design.

Keywords: CGRA, reconfigurable architecture, compiler, source code mapping.

1. SPEAKERS' BIOGRAPHY

Tom Vander Aa is a senior researcher in the Wireless Communication group of IMEC working on low energy high performance architectures and compilation techniques. Since 2005 he has been working on the ADRES coarse-grain array processor. In 2005, Tom Vander Aa obtained a PhD in electrical engineering from KULeuven, Leuven, Belgium on energy optimization for instruction memory of embedded processors. He has a master in computer science degree, also from KULeuven and is a member of the IEEE.

Panagiotis Theocharis is a doctoral researcher in the Computer Systems Lab of Ghent University working on split compilation for accelerator-based multicores. He holds a diploma in electrical and computer engineering from the National Technical University of Athens and is a member of the ACM and the IEEE.

2. TOPICS

Below is a list of topics covered during the tutorial:

- **Presentation**: Introduction to CGRAs and their compilation techniques, taking the ADRES CGRA as an example (45')
- **Presentation + demo**: Introduction to the DRESC tool chain (15')
- **Guided hands-on**: The audience can have a first try of compilation and simulation. (30')
- **Presentation**: How to optimize your source code for CGRAs (30')
- **Hands-on**: The audience will try to optimize a prepared example for the CGRA. (30')
- **Presentation**: Current research in CGRA compilation: building optimizing compilers using machine learning. (30')

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