

Photonics and Electronics Integration in the HELIOS project

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ABSTRACT

The objective of the European project HELIOS is to combine a photonic layer with a CMOS circuit by different innovative means, using microelectronics processes. Bonding of AWG + Ge Photodiodes on CMOS wafer is achieved.

HELIOS PROJECT DESCRIPTION

The HELIOS project (pHotonics ELeCtronics functional Integration on CMOS) was launched in May 2008 under the 7th Framework Programme (FP7) of the European commission. It gathers 19 European partners and aims at combining a photonic layer with a CMOS circuit by different innovative means. This 4-year project is coordinated by CEA-LETI and has been awarded a 8.5 Million Euros grant (<http://www.helios-project.eu>). By co-integrating optics and electronics on the same chip, high-functionality, high-performance and highly integrated devices can be fabricated using a well-mastered microelectronics fabrication process. HELIOS will thus allow to combine a photonic layer with a Complementary Metal Oxide Semiconductor (CMOS) circuit. The objectives of the project are manifold with the aim of demonstrating the power of this CMOS photonics production chain through several complex photonic IC's that address different industrial needs. These include a 40Gb/s modulator, a 16x10 Gb/s transceiver, a Photonic QAM-10Gb/s wireless transmission system and a mixed analog and digital transceiver module for multifunction antennas. One of the main challenging tasks of HELIOS is to analyze and compare the figures of merits of different full integration options [1] as sketched in Figure 1.

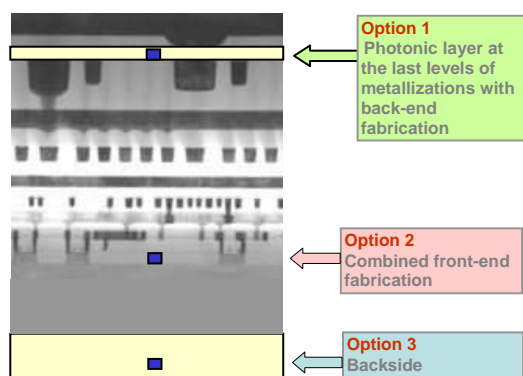


Figure 1: Integration options

Option 1: The photonic layer is build on top of the EIC at the last levels of metallization. Option 1A consists in building the photonic layers with only low temperature processes <400°C. Option 1B consists in fabricating the photonic functions on a separate wafer, then bond it on the electronic wafer. Option 2: A specific front-end technology which combines the processing steps of electronic and photonic devices is developed with a specific design library. Option 3: The use of the rear side of the Electronic Integrated wafer leads to high integration density as for option 1.

The combined fabrication corresponding to option 2 has already been successfully demonstrated by Luxtera using a modified 130nm SOI technology process from Freescale. However III-V components can only be integrated with Flip-Chip technology. Since the beginning of this century, LETI and other project partners developed building blocks for Option 1. The technologies developed are either pure SiGe or heterogeneous through InP die bonding. Recently within the Wadimos project [2] LETI has demonstrated the lasing of InP rings coupled to a SOI waveguide which was fully fabricated in a microelectronics environment. Option 3 uses the same building blocks as option 1. However, Through Silicon Vias (TSV) have to be available in order to connect the photonics active building blocks to the electronic parts. Austriamicrosystems has optimized within the frame of the HELIOS project the TSV technology (Figure 2). Integration of photonic layers at the backside of CMOS wafers is as follows. First of all the CMOS wafer is processed up to the last metal layer. Then the wafer is thinned and the back side of the CMOS wafer is fine polished to prime wafer surface quality (micro roughness <0.5nm) and the completed photonic wafer (already cladded with SiO₂ and planarized by CMP) is bonded at low temperature on this back side. Then, a deep silicon etching is performed down to the metal layer of the photonic wafer. Subsequent TSV isolation and TSV

metallization are deposited. Finally, the top metal, which connects the TSV with the IC, and the passivation is deposited and structured.

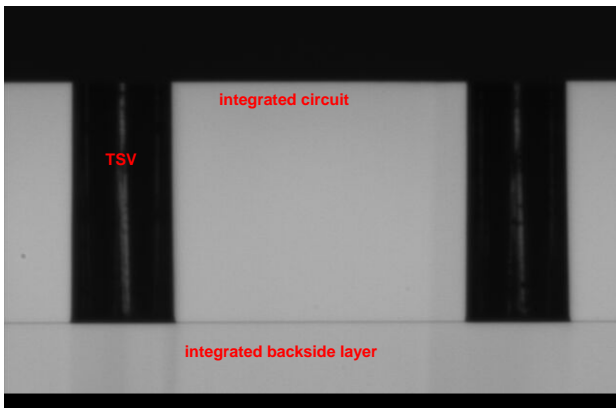


Figure 2: TSV for backside integration

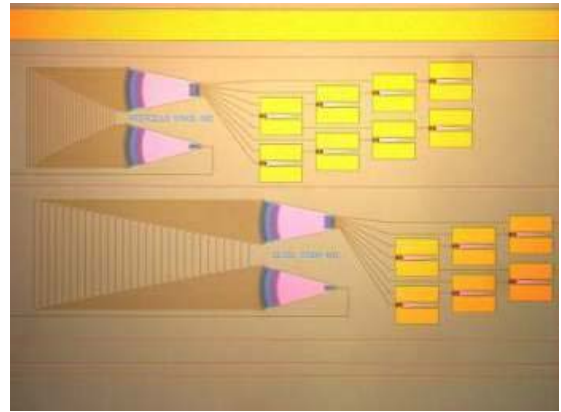


Figure 3: Photonic wafer with AWG and Ge photodiodes

RECEIVER WITH GE PHOTODIODES ON CMOS WAFER

Using the wafer bonding technique, one can introduce a photonic layer at some level in the processing steps of CMOS. Since the first metal layers are too densely packed and thin, introduction at the upper metal layers must be considered. The technique is to use wafer bonding of a processed CMOS wafer and a photonic wafer. After the fabrication of metal 4 in the Austriamicrosystems CMOS process, the planarized surface has been coated with a deposited oxide. The planarity and the micro-roughness have to match the specifications for bonding.

In parallel, on SOITEC optical SOI 220nm on 2 μ m BOX, we have processed a photonic wafer with surface grating couplers, AWG, and Germanium photodetectors. The regular standard technology of epIXfab [<http://www.epixfab.eu/>] was used to define (i) the arrays of 1D gratings couplers with 70nm partial silicon etch and (ii) waveguides with a full etch down to the BOX. Two different 8 channels AWG designed by IMEC were selected with 200GHz or 400GHz spacing. Lithography was performed with a 193nm Deep Ultra Violet stepper and the silicon waveguides were defined using a silica hard mask with HBr etching. We then defined cavities for the selective epitaxial growth of Germanium. This is achieved by deposition of a silica layer which is etched at the end of waveguides. In order to achieve direct coupling, the silicon part of the cavities is etched down to 50nm on top of the BOX. Germanium was then selectively grown in the cavities and CMP used to adjust the thickness. Ion implantation of Phosphorus and Boron was then used to define the N and P parts of the lateral PIN Ge photodiode. Electrodes were finally fabricated using silica deposition and Ti/TiN/AlCu deposition with 248nm DUV lithography and Reactive Ion Etching.

Wafer optical test was performed on the AWG and arrays of photodetectors. The signal of the 8 photodiodes connected to the 400GHz AWG is shown in Figure 4. The light is totally absorbed in a 5 μ m long photodiode. Capacitance is in the 10 fF range and dark current of the order of 80nA (-0.5V). With the design used, the bandwidth was measured at 20GHz (Figure 5), which should be enough for the 10Gbit/s operation required for the demonstrator.

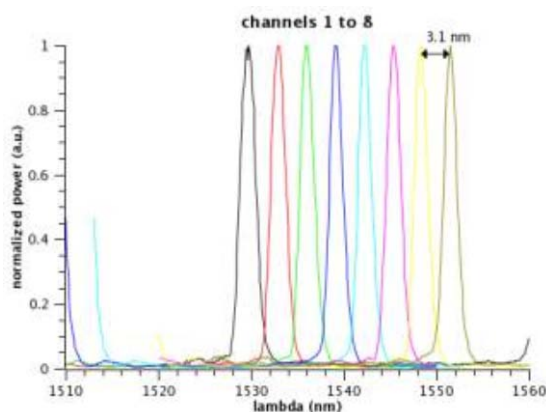


Figure 4: Output of the Ge photodiodes

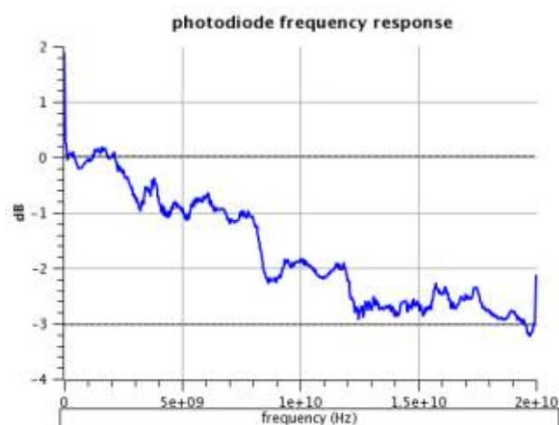


Figure 5: Bandwidth of the Ge photodiodes

Cladding with oxide and planarization of the optical wafer with CMP was then performed in order to prepare the wafers for bonding. Perfect cleaning of both wafers facilitated their direct bonding at room temperature. With EVG equipment and alignment patterns, the alignment accuracy between the electrical and the photonic parts is in the micrometer range. Therefore, the design rules for the subsequent metal layers have to take this alignment margin into account. After bonding, grinding and chemical etching of the backside of the Si optical wafer, a flat surface of thermal oxide remains on the top of this PEIC circuit. Some subsequent process steps are needed to electrically connect the electrical and photonic parts which involve etching through the top layer to contact the electrical circuit below. This technique is often called 3D heterogeneous integration because the CMOS part is separated from the photonic part without any silicon surface waste at the transistor level. With this approach, any microelectronics technology can be used for the electrical parts and III-V components can be embedded in the photonic layer. Figure 6 shows the PEIC composed of the photonic layer (AWG and Ge photodiodes) bonded on a trial CMOS wafer from Austriamicrosystems.

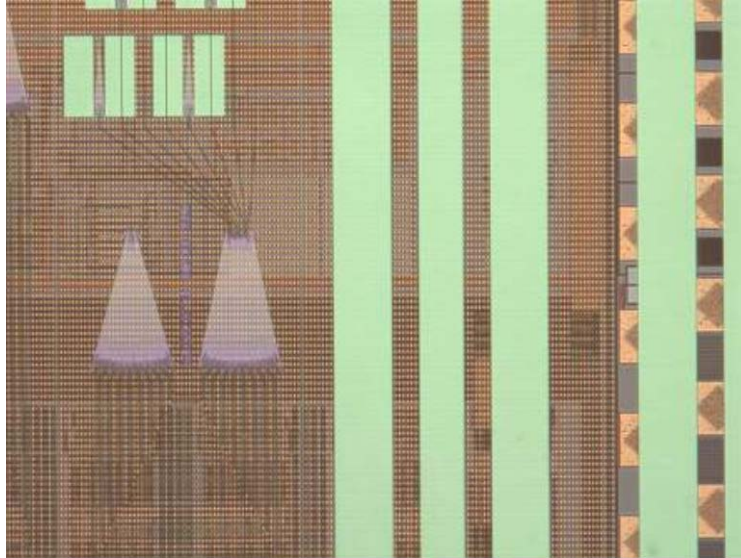


Figure 6: Photonic Electronic wafer with AWG and photodiodes

CONCLUSION

Different approaches for photonics - electronics integration are studied in the HELIOS project. We highlighted the Front Side and Back Side wafer bonding strategies [5]. With a Front Side approach, we demonstrated the operation of an AWG connected to an array of high speed Ge photodetectors. The building blocks developed in the HELIOS project will be assembled in order to achieve the different foreseen demonstrators (high speed modulator, WDM transceiver, QAM system). Already 15GHz modulators [5] and 40GHz Ge photodetectors [6] have already been achieved. Less than 2dB loss couplers have been demonstrated with either 1D surface grating or inverted taper couplers. Moreover InP on Si lasers fabrication with 200mm processing in a microelectronics clean room have been achieved for applications requiring embedded lasers. [3,4]

ACKNOWLEDGMENT

The research leading to these results has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement n° 224312 HELIOS.

REFERENCES

- [1] J. M. Fedeli, L. Di Cioccio, D. Marris-Morini, et al., "Development of Silicon Photonics Devices Using Microelectronic Tools for the Integration on Top of a CMOS Wafer," *Advances in Optical Technologies*, vol. 2008, Article ID 412518, 15 pages, 2008. doi:10.1155/2008/412518 (2008)
- [2] L.Liu & al, GFP2010.
- [3] M.Lamponi &al, GFP2010.
- [4] B.Ben Bakir & al, GFP2010.
- [5] D. Marris-Morini &al, "Low loss and high speed silicon optical modulator based on a lateral carrier depletion structure", *Optics Express* 16 (1), 334-339 (2008).
- [6] L.Vivien & al, "42 GHz p.i.n Germanium photodetector integrated in a silicon-on-insulator waveguide" *Optics Express* 17 (8), 6252-6257 (2009)
- [7] *Silicon photonics II* edited by D. Lockwood and L. Pavesi (Springer Verlag 2010)