200mm Wafer Scale III-V/SOI Technology for All-Optical Network-on-Chip and Signal Processing

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Abstract—**Integrated components, including microdisk lasers, photodetectors, and wavelength selective circuits, for optical network-on-chip and all-optical signal processing are presented using a complementary metal-oxide-semiconductor compatible III-V/silicon-on-insulator integration technology at 200mm wafer scale.**

Keywords—silicon-on-insulator; heterogeneous integration; microdisk laser; network-on-chip; flip-flop

I. INTRODUCTION

It has been envisioned that optical interconnect and more complex optical network-on-chip (ONoC) will replace the current electrical wires for transporting information between processor cores [1]. Silicon-on-insulator (SOI) photonic structure has been considered as a promising platform for such complex networks due to the compact devices and the compatible fabrication processes with complementary metal-oxide-semiconductor (CMOS) technology [2]. With the integration of other functioning materials, e.g., III-Vs, various components, including waveguides, filters, modulators, lasers, detectors, etc, have been demonstrated based on SOI [3]. In this paper, we will introduce our recent development of compact photonic devices for on-chip optical interconnect and high-speed optical signal processing, as well as the integration of them with a CMOS compatible III-V/SOI technology at 200mm wafer scale.

II. INTEGRATION TECHNOLOGY

A. III-V-on-SOI Bonding Technology

To achieve the heterogeneous integration of III-V material and SOI, we adopt the die-to-wafer bonding technology, where unpatterned III-V dice are integrated on top of a processed SOI wafer. Two bonding approaches were mainly investigated. The first is the silicon oxide direct bonding [4]. The patterned SOI wafer is first planarized by deposition of SiO$_2$ and chemical-mechanical polishing (CMP). A thin layer of SiO$_2$ is also deposited on the III-V dice. After chemical activation steps, the two surfaces are brought in contact. Covalent bonding can then be formed through a low temperature annealing at 300°C. This process under development allowed us to achieve a bonding
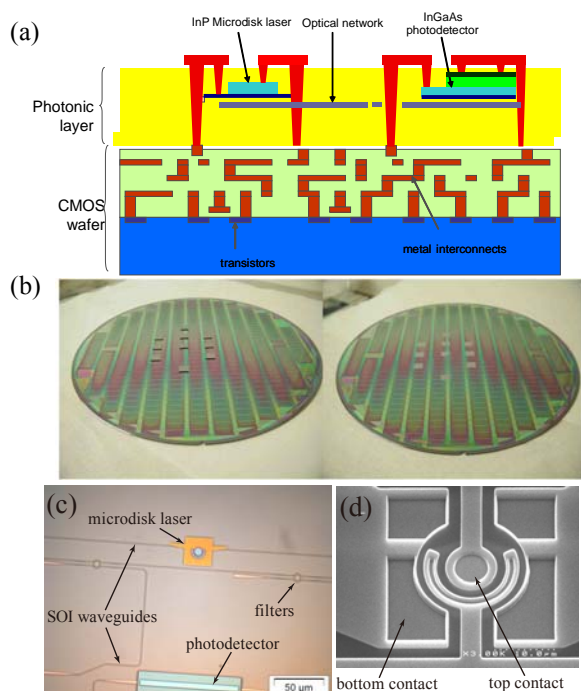

Figure 1. (a) Above-IC silicon photonics and III-V integration scheme. (b) InP die-to-wafer SiO$_2$ direct bonding on 200mm passive optical circuits, after bonding (left), and after complete substrate removal (right). (c) Integration of III-V active devices on top of SOI passive circuits (top view). (d) SEM image of a fully processed microdisk laser.

yield in the order of 80% after complete InP substrate removal. Another approach, the adhesive bonding, uses divinylsiloxane-benzocyclobutene (DVS-BCB) polymer as a bonding agent [5]. A thin DVS-BCB layer is first spin-coated on the SOI wafer, which will planarize the topology of the SOI structure. After attaching the III-V dice, the whole stake is hard cured in order to completely polymerize the DVS-BCB material. In both approaches, after the bonding process the carrier InP substrate is then removed with the combination of chemical grinding and wet etching, leaving only the functioning III-V epi layers. Since it is doubtful whether DVS-BCB is a CMOS compatible material, the direct bonding is adopted for device fabrication in a CMOS pilot line.
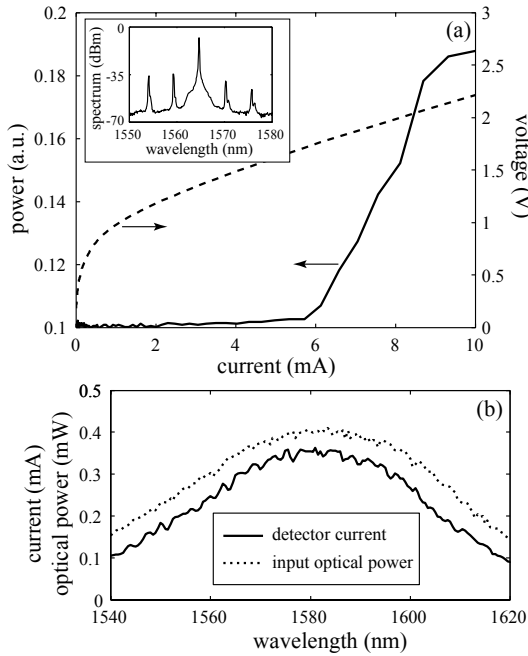
Figure 2. (a) LIV curve of a 40μm diameter microdisk laser. Inset shows the laser spectrum at 23.4mA bias. (b) Wavelength response of an evanescently coupled waveguide detector with an 80μm long absorption section.

B. III-V Epi Layer Design and CMOS Compatible Process at 200mm Wafer Scale

A specific process adapting and modifying the standard III-V materials process steps to comply with a CMOS environment is presented, using the so-called above-IC approach schematically represented in Fig. 1(a). Here the devices are fabricated at the back-end of line (BEOL) levels keeping a temperature budget limited to 350°C – 400°C. An original III-V epi layer design which contains both the laser and the photodetector heterostructures in the same epitaxy was implemented to fabricate the photonic chips (cf., Fig. 1(a)). Compared to already demonstrated point-to-point links where some dice are dedicated to laser structures and some others to photodetectors structures [6], this allows for a much simpler integration scheme as well as much lower footprints optical links. This epitaxy layer was bonded on top of the SOI wafer as shown in Fig. 1(b). The total epitaxy thickness is only 1μm which enables the use of 248nm deep ultraviolet (DUV) lithography without focalization issues. The subsequently III-V processing, including wet and dry etching, oxide isolation layer deposition, metallization, etc, are optimized at 200mm wafer scale. Figure 1(c) shows an optical microscope image of both III-V microdisk and photodetector on top of waveguides (SiO₂ bonding layer thickness: 130nm) after the III-V etching. Regarding the CMOS compatible contacts, the standard gold-based metallization and the usual lift-off technique to define the contact area were discarded. Instead, a Ti/TiN/AlCu metal stack is full-sheet deposited. After a lithography step, the metal stack is dry-etched with a chlorine-based chemistry down to the oxide isolation layer which also acts as an etching stop layer. No annealing is performed on the wafers. This metallization scheme allows obtaining ohmic contacts on both n-InP and p-InGaAs, with a specific contact resistance of
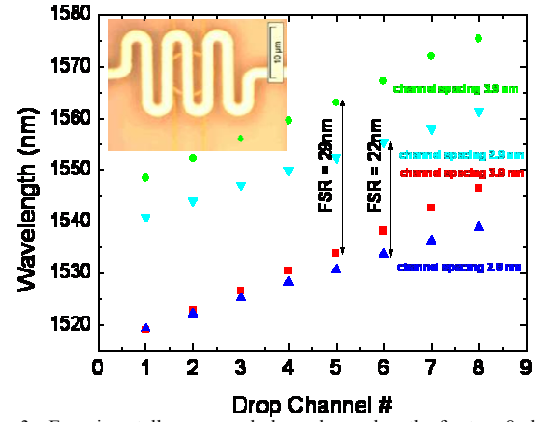

Figure 3. Experimentally measured channel wavelengths for two 8-channel demultiplexers with 29nm and 22nm FSR, respectively. The inset shows a microscope image of the fabricated heater with underlying ring resonator.

$1\times10^{-4}\Omega\cdot cm^2$ for $5\times10^{18}cm^{-3}$ n-InP and $6\times10^{-5}\Omega\cdot cm^2$ for $3\times10^{19}cm^{-3}$ p-InGaAs [7]. Figure 1(d) shows a scan electron microscope (SEM) image of a fully processed microdisk laser.

III. OPTICAL NETWORK-ON-CHIP

Microdisk lasers with diameters of 20μm and 40μm were fabricated and characterized. The output power was collected at one end of the SOI waveguide by using a fiber grating coupler. Continuous-wave lasing at room temperature was observed. The light-current-voltage (LIV) curve of a 40μm diameter microdisk laser is shown in Fig. 2(a). The VI curve is similar to devices fabricated earlier where gold contacts were used [3]. It can be seen that these devices have a threshold current of 6mA, corresponding to a threshold current density of 0.48kA/cm². A maximum output power of 150μW in the SOI waveguide was measured. The optical spectrum of such a microdisk laser at 23.4mA bias is displayed in the inset of Fig. 2(a). The free spectral range (FSR) of the azimuthal fundamental modes is ~5.7nm and the side mode suppression ratio is higher than 27dB at this current. We found that the 20μm diameter disks have threshold currents of ~3mA and output powers up to 68μW.

Evanescently coupled waveguide detectors with various lengths were fabricated, and the SOI waveguides under the detectors were tapered to different widths to examine the coupling efficiency. Responsivity varies from 0.7A/W for detectors with 20μm long absorption sections to 0.9A/W for 100μm long absorption sections on top of 500nm wide waveguides. The wavelength response is shown in Fig. 2(b) for a detector with an 80μm long absorption section. The Gaussian shaped spectrum is caused by the fiber grating couplers. Series resistances between 500 and 1000 Ω were measured. The capacitance is calculated to be in the order of 20 to 180 fF. Therefore, we expect a 3dB bandwidth up to 14GHz.

Wavelength division multiplexing is necessary for improving the capacity of one connection. In ONoCs wavelengths can also be used as a routing mechanism between difference processor cores. Ring based (de)multiplexer is an ideal structure in this case concerning the footprint. Figure 3 shows the measured channel wavelengths from two such
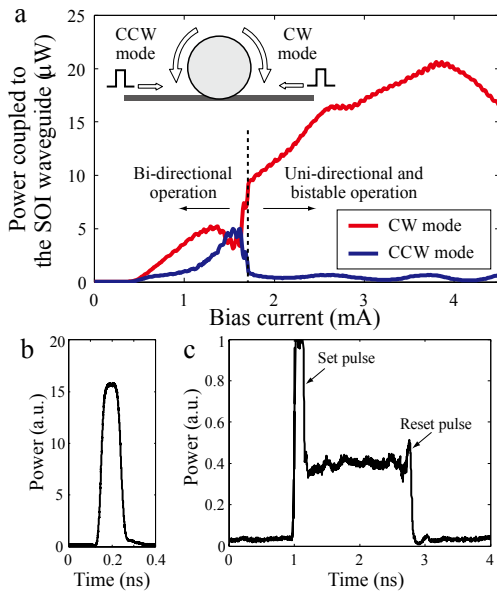
Figure 4. (a) LI curves for CW and CCW mode, inset shows a sketch of the bistable microdisk laser with the triggering pulses. (b) Time trace of the triggering pulses. (c) Time trace of the CCW mode under flip-flop operation.

demultiplexers. Each of them was built by cascading 8 SOI ring filters with slightly different diameters on one bus SOI waveguide. Uniform distribution of the channel wavelengths between one FSR is presented. Further fine-tuning of the wavelength positions can be realized through an integrated Ti/TiN heater on top of each ring as shown in the inset of Fig. 3. A tuning rate of 0.3nm/mW was obtained experimentally.

IV. ALL OPTICAL FLIP-FLOP

It is known that two counter-propagation modes, namely clockwise (CW) mode and counter-clockwise (CCW) mode, can exist in a disk cavity laser [8]. These two modes will compete for the material gain, and in such a disk cavity the cross gain suppression coefficient is twice as large as the self gain suppression coefficient [8]. This leads to a bi-stable uni-directional operation of the laser, where one mode will dominate and the other is suppressed, as show in the inset of Fig 4(a) [9]. Since this phenomenon is based on gain suppression, a high photon density inside the cavity is needed. In the present microdisk laser, this is ensured by using an ultra-small disk structure made possible through a deeply etched sidewall. In addition, a special heat sink was prepared, which improves the thermal behavior of the microdisk laser especially at a high bias current [9]. The coupling between the CW and CCW modes, resulted from the sidewall roughness of the cavity and the back reflection of the output grating coupler, hinders a stable unidirectional operation. This coupling is kept low through optimizing the III-V etching process and decreasing the coupling strength between the cavity and the SOI waveguide using a relatively thick bonding layer. Figure 4(a) shows the LI curve of a designed microdisk laser of 7.5μm diameter under continuous-wave operation. Threshold current is as low as 0.33mA. Bi-stable, uni-directional operation starts at 1.7mA.

An all-optical flip-flop (AOFF) memory can be built from this bistable microdisk laser employing the property that the dominant mode can be switched between CW and CCW by sending optical pulses from the SOI waveguide as shown in the inset of Fig. 4(a). The flip-flop operation is demonstrated in Fig. 4(b & c) using triggering pulses of 100ps duration and 18pJ energy at a continuous bias of 3.5mA. Switching of the lasing direction was achieved within 60ps. The extinction ratio is about 11dB. The total power consumption and the device size of the AOFF are the smallest reported so far at telecom wavelengths. This is also the only electrically-pumped AOFF built on silicon.

V. CONCLUSION

We have demonstrated a CMOS compatible III-V/SOI technology at 200mm wafer scale. Compact devices, including microdisk lasers, photodetectors, ring filters, and flip-flop memory cells were demonstrated with promising performances and a potential for ONoCs and all-optical signal processing.

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