

## Multiple Chip Integration for Flat Flexible Electronics

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### Abstract

These days, there is a lot of interest for making electronic devices lighter and compacter, as the electronics market is rapidly expanding with all sorts of portable devices for home and everyday use. Here, a technology for embedding single thin chips in flexible substrates is further investigated so that several chips might be integrated within the same substrate.

This technology offers the possibility of reducing weight, while at the same time enhancing the mechanical flexibility of the electronic circuitry. Such an integration is particularly interesting in the area of flexible displays, where the flexibility of the display is too often hampered by the rigidity of its driving electronics.

### Introduction

Flexible substrates are often an interesting alternative for rigid PCBs because they are light and conformable. This is especially an advantage when integrating electronic devices for wearable applications. A light and flexible substrate by itself however does not guarantee a light and flexible end result. The flexibility is often drastically reduced when rigid components are assembled onto the substrate.

Considering the current trend of increasing component density, which is of course welcomed for wearable devices, the benefit of the flexibility of the substrate is more and more overshadowed by the rigidity of the components. An obvious way of tackling this issue is to use smaller and thinner -and consequently also lighter components.

However, when chips are thinned down to approximately 20  $\mu\text{m}$ , they are too fragile to be assembled onto a substrate with standard die assembly techniques (at present). The UTCP (Ultra Thin Chip Packaging) technology, copes with this by actually embedding the ultra thin chips inside the substrate [1]. The existing UTCP technology is given in a short overview, discussing the benefits of the flat UTCP variant used here, then the design is briefly discussed, after which the fabrication and the resulting substrates are somewhat more characterized. A conclusion with a future outlook is finally presented, with a particular focus on the area of flexible displays, where flatness of the substrate is crucial for further processing of display backplanes.

### Technology Flow

The technology used here is an enhanced version of IMEC's first UTCP (Ultra Thin-Chip Packaging) technology with an updated process flow to realize a more symmetrical package. The used process flow is depicted in Figure 1.

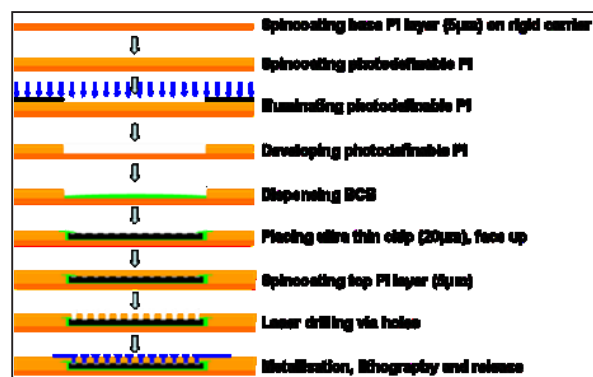


Figure 1

The base PI layer is spincoated onto a rigid (glass) carrier substrate and cured. Then the photodefinable PI is spincoated, illuminated through a mask and developed to define the chip cavity. After curing, the chip is placed face up, using BCB in the cavity as adhesive. The BCB is cured, and the top layer of PI is spincoated and cured in the same way as the base PI layer (thus creating a symmetrical substrate sandwich). The via holes to the chip contacts are laser drilled and after the metal pattern is realized on top, the substrate can be released from its carrier.

### Test Design

The chips used for the embedding trials are thinned-down test chips available at IMEC. They are specified as PTCK chips, which stands for "Packaging Test Chip version K", and measure 5 mm by 5 mm. There are four different versions of PTCKs, but all have the same peripheral bond pad layout, which is all that will be used in the tests described in this paper. This bond pad layout, and how they are connected, is shown in Figure 2. The bond pads at the periphery come in 3 pitches, 100, 60 and 40  $\mu\text{m}$ , and a more zoomed view on the right shows the different interconnection schemes on the chip.

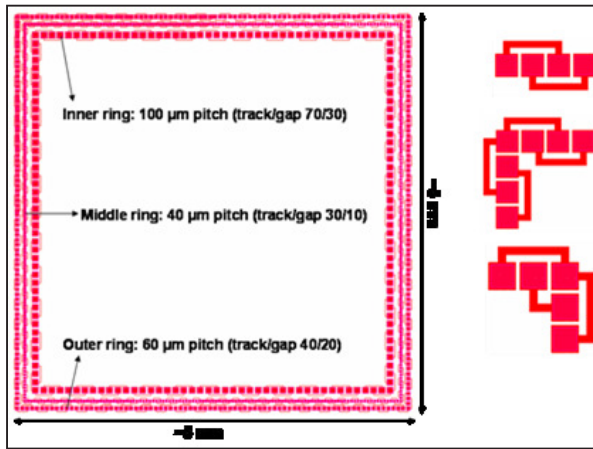


Figure 2

As there are different pitches of output pads available, contact measurements can be done from 100 and 60, down to 40  $\mu\text{m}$  pitch patterns. The metal pattern on the chip allows for daisy chain testing as well as 4-point-measurements for contact resistance.

These chips have been thinned down at IMEC from about 500  $\mu\text{m}$  to approximately 20  $\mu\text{m}$  and are at that point so thin that they become somewhat transparent, sufficiently so that the metal patterns on the front can be easily identified with illumination only from the backside. This is illustrated in Figure 3. The bond pads of the test chips have been bumped with NiAu, approximately 5  $\mu\text{m}$ , which acts as a buffer layer for the laser drilling, to protect the Al contacts.

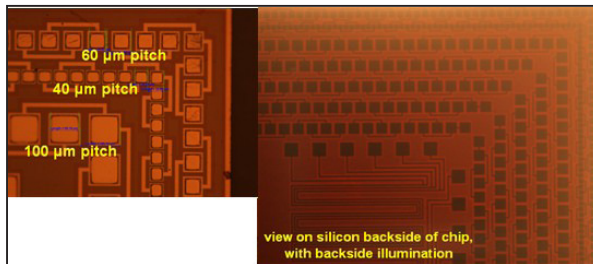


Figure 3

The idea here is to embed several chips in the same PI substrate sandwich. With the feasibility of the technology proven to work at chip bump pitches down to 40  $\mu\text{m}$  [2], the alignment possibilities when placing chips needs to be investigated. In this view, the flat UTCP technology is interesting in such a way that it offers the possibility of photolithographically defining all the cavities, wherein the chips are to be placed, at the same time in one masked illumination step. If the chip then adequately matches the dimensions of the cavity, the placement error should be small enough to ensure good alignment between the (in the cavity) placed chips, and the chips can be interconnected by the routing layer on top.

The test has been set up with four chips to be embedded and interconnected in the same substrate. The four chips are placed in the corners and the layout is designed to form two daisy chains on each separate chip, and a daisy chain running between each two neighbouring chips. The mask designs are shown in Figure 4. The trials have been designed for the (coarsest) chip pitches of 100  $\mu\text{m}$ . Mask layouts are shown for the cavities (upper left), metallization layer (upper right) and soldermask (below left), and additionally the design of the upper left corner is shown more in detail (below right).

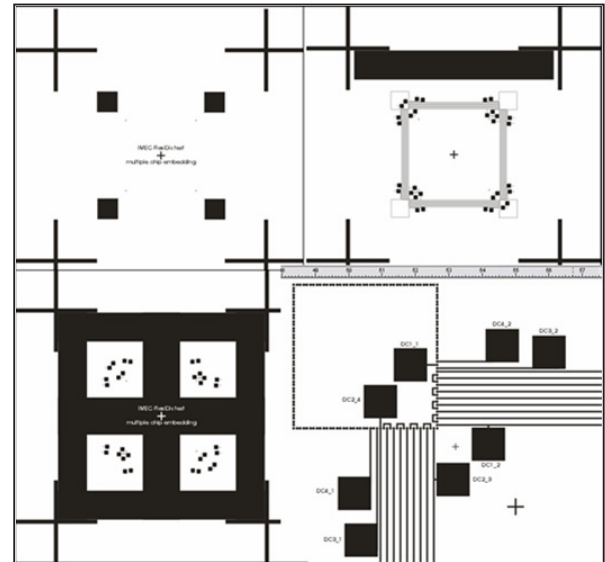


Figure 4

### Fabrication Process

Processing of the device is carried out on a glass substrate, 5 cm by 5 cm. Three layers of spin-on PI, all supplied by HD Microsystems, are involved: the base PI layer, the inner (photodefinable) PI layer and the top PI layer. This layer buildup is symmetrical, with both base and top layer being PI2611 and the inner layer being HD7012, to avoid problems with CTE (Coefficient of Thermal Expansion) mismatch (usually resulting in curling of the substrate when the release is carried out).

The base PI layer is spun at 3000 rpm for 45 seconds to get a 5  $\mu\text{m}$  thick layer (this will be the thickness after curing) and cured a vacuum oven (with 5 sccm nitrogen flow), with a final cure temperature of 350°C. The next layer consists of photodefinable PI, wherein the cavities for the chips are to be made. This layer is applied in a similar way, on top of the base PI layer, but the base layer is plasma-etched (through reactive ion etching, RIE) beforehand to improve adhesion. Spinning at 3000 rpm for 45 seconds now results in a thickness after curing of approximately 36  $\mu\text{m}$ , due to the HD7012's higher viscosity.

As this is the photodefinable layer, first a soft-bake is introduced to the PI after which illumination through the cavity mask is needed for 28 seconds. At this point it is crucial that the substrate is illuminated on a black background: since the substrate is transparent, the UV-light should be absorbed to avoid random scattering when it is reflected on a white background (resulting in poorly defined edges). Development is then achieved by placing the substrate in PA400D for 90 seconds with UltraSonic Agitation (USA) and then rinsing in PA400R for 15 seconds. Both chemicals PA400D and PA400R were again obtained from HD Microsystems. After this the cavities in the PI can easily be identified, and curing, again up to 350°C solidifies the photodefinable layer.

The cavities in the photodefinable layer are then dotted with BCB that will act as adhesive, and the chips aligned and placed inside the cavities manually. Any excess BCB that has spread out on the active side of a chip should be cleaned carefully, as it has proven to be difficult to laser drill the vias to the contacts (at a later stage) through any cured BCB. For curing the BCB, heating up to 250°C is sufficient from the BCB's point-of-view, but since the next cure step will again go up to 350°C (curing of the top PI layer), it is preferable to also use the same final curing temperature here as for the PI layers.

Now that the chips are safely inserted, the top layer can be applied to cover it all up. Again the substrates are plasma-etched to improve adhesion, and as PI2611 is not self-priming, in contrast to HD7012, also adhesion promotor has to be spun onto the plasma-etched active surface. This is done for 30 seconds at 3000 rpm, and is followed by a 1-minute softbake at 120°C. The top layer is spun and cured in the same way as the base layer, to have the same layer thickness and a symmetrical package (in cross-section).

With the chips embedded and covered up by the top PI layer, holes have to be drilled through 5 µm top PI layer so that the chips' bumps (5 µm thick electroless NiAu, as mentioned earlier) can be contacted. The drilling is done with a 355-nm-YAG-laser (laser via drilling), using an attenuation of 300 mW (for a 25 µm spot size), a circular mask of 200 µm diameter and a Gaussian beam, with 100 pulses at 10000 Hz. The resulting vias have a diameter of on average 12 µm. This combination of attenuation and via size corresponds to a power setting of approximately 69 mW. As the chips' contacts measure 70 µm by 70 µm (for the 100 µm pitched design), a matrix of 3 by 3 vias can be realised.

The next layer that needs to be put in place is the metallization layer, that has to route the chips' contacts across the PI substrate. To achieve this, pattern plating is the preferred option, as bare chips typically have fine features, in this case 70 µm. First, the surface with the top PI layer is prepared by plasma-etching to enhance adhesion in the same way as described above. Then a metallization seed layer, consisting of TiW (for adhesion)

and Cu, is deposited by sputtering, the (inverted) pattern is aligned and defined in a photoresist layer by standard lithography. For the plating area of approximately 1 cm<sup>2</sup>, 10 minutes at 100 mA gave satisfying results: approximately 6 µm over the surface area available for plating.

At this point, the whole surface is evidently still shorted by the remaining seed layer, so the seed layer remains to be etched, after stripping the photoresist pattern. The Cu seed layer can be etched with a standard micro-etch solution, while the TiW layer is removed in warm (52°C) H<sub>2</sub>O<sub>2</sub>.

As is common in PCB and flex technologies, soldermask is then applied to cover up everything but the contact areas, so as to protect the Cu tracks against oxidation and corrosion, and the contacts can then be plated up electrolessly with Ni to the desired thickness, typically a few µm. A Au finish is finally applied on the Ni surface of the contacts to improve (i.e. lower) the contact resistance of the contacts.

Now the finished substrate can be cut out and released from the glass carrier.

This whole fabrication process is elaborated and illustrated more and better in [2], but is given here in a brief overview as the article is still being reviewed for publication.

## Results

The first results for embedding multiple chips are promising. A number of problems did arise during processing, such as a substrate table lagging behind during laser drilling, a cavity design not matching the metallization design mask and chip breakage during placement, but all these could be overcome. To give an idea of the result, some pictures of the fabrication can be found in Figure 5. Several pictures are shown: a placed chip (top left), 4 embedded chips interconnected by the Cu metallization layer (top right), a zoomed view (bottom left) and the end result, with soldermask and NiAu finish (bottom right).

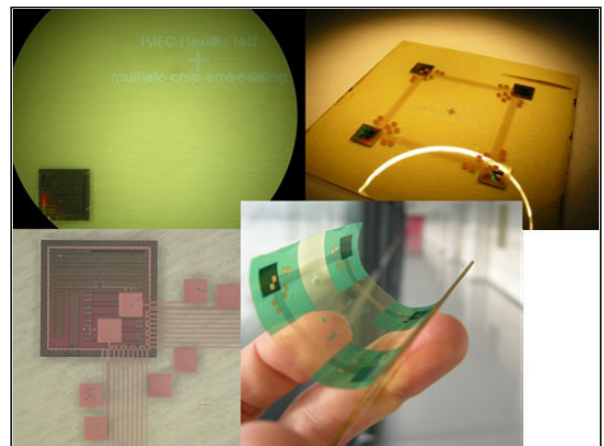


Figure 5

The result, as clarified in the Figure 6, shows that the alignment accuracy of the process is sufficient to interconnect the 100  $\mu\text{m}$ -pitched contacts of the four thin chips embedded in the cavities of the PI substrate.

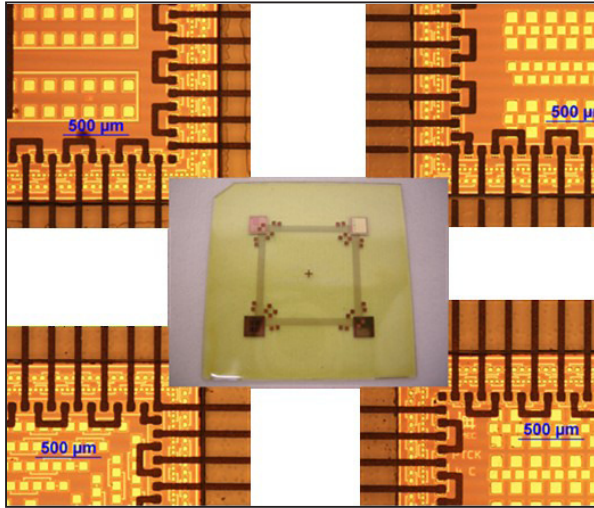


Figure 6

Electrical measurements also confirm the feasibility of this technology, although so far only one substrate has been completed and measured. The measurements are given in Table I.

	Measurement [ $\Omega$ ]	# connections	#□ on UTCP	#□ on chip	Verification [ $\Omega$ ]
DC1_1-2	19.1	18	3498	216	17.874
DC1_2-3	X	2	804	48	4.048
DC1_3-4	X	18	3498	216	17.874
DC2_1-2	16.8	18	3498	216	17.874
DC2_2-3	4.2	2	804	48	4.048
DC2_3-4	17	18	3498	216	17.874
DC3_1-2	8.5	18	175	240	8.721
DC4_1-2	53.4	129	95	1632	56.031
DC5_1-2	9	18	175	240	8.721
DC6_1-2	53.9	129	95	1632	56.031
DC7_1-2	8.6	18	175	240	8.721
DC8_1-2	54.3	129	95	1632	56.031
DC9_1-2	8.4	18	175	240	8.721

Table I

Two daisy chain structures, namely DC1\_2-3 and DC1\_3-4 could not be fully measured due to the fact that a few interconnection tracks were interrupted at the chip cavity interface. This is a known, and sometimes problematic phenomenon, also described in [2], that can be attributed to a combination of insufficient illumination/development of the photoresist pattern for pattern plating, and ill-matching chips and cavities.

The verification column in the table shows what the expected value is for the resistance, based on earlier

results from the UTCP measurements with 100  $\mu\text{m}$ -pitch contacted thin chips [2]. These values are 2  $\text{m}\Omega$  for the contact resistance, 3  $\text{m}\Omega/\square$  for the resistance of the UTCP's Cu metallization, and 34  $\text{m}\Omega/\square$  for the resistance of the Al metallization on the chip.

### Conclusion and Outlook

Here in this paper is presented the research that has been carried out to embed multiple ultra-thin chips in a flexible PI substrate. It has been proven feasible to successfully interconnect several test chips with contacts at a pitch of 100  $\mu\text{m}$ , using UTCP technology that is currently still in the development stage at IMEC.

As for the future, several directions are interesting for this kind of technology. One of the original purposes that it was developed for, encompasses the integration of driver chips into flexible displays, either as separate flexible packages, or directly integrated into (one of) the display substrates. First trials with functional driver chips are being processed to investigate the feasibility of this, as illustrated in Figure 7.

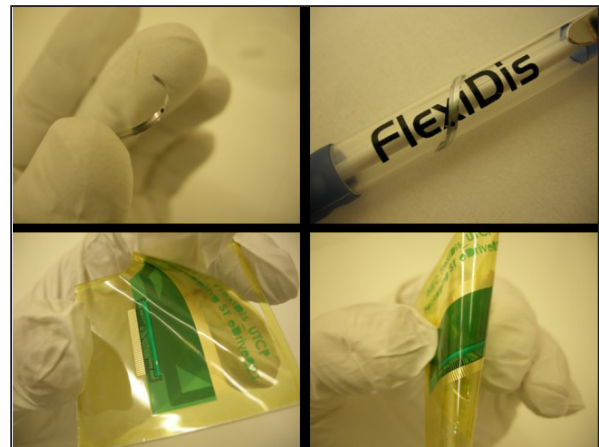
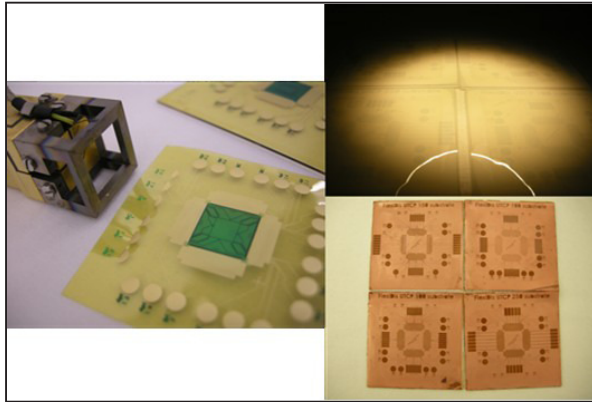


Figure 7

Furthermore, tests are also being carried out to assemble such kinds of UTCPs onto patterned flexible substrates. Example material is shown in the figure below, and will be presented shortly at the 2<sup>nd</sup> Electronics System-Integration Technology Conference in London (ESTC 2008, September 1<sup>st</sup>-4<sup>th</sup>).



*Figure 8*

Finally, embedding of multiple chips could be an important enabler for industrial mass-production of UTCs, where several ultra-thin chips could be embedded using large carrier-substrates. Then further processing is done simultaneously on all embedded devices at once, and finally, the substrate can be separated. This is a technique commonly used, e.g. in flat panel display fabrication.

#### **Acknowledgments**

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#### **References**

1. W. Christiaens, B. Vandeveldel, E. Bosman and J. Vanfleteren, "UTC: 60  $\mu$ m thick bendable chip package", Proceedings of IWLPS (San Jose), November 2006.
2. J. Govaerts, W. Christiaens, E. Bosman and J. Vanfleteren, "Fabrication Processes for Embedding Thin Chips in Flat Flexible Substrates", IEEE Transactions on Advanced Packaging, under review (proposed January 2008).