Analysis and Design of a High Power, High Gain SiGe BiCMOS Output Stage for Use in a Millimeter-Wave Power Amplifier

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***Abstract*—In this paper a high gain, high power output stage designed in a 250nm SiGe BiCMOS technology is presented. The used topology together with a discussion on the stability of the output stage is explained in detail. In order to increase the gain of the output stage and thus increases the attainable power added efficiency (PAE), positive feedback is used. Furthermore a formula predicting the input impedance of a common base transistor at high frequencies is deducted which explains and predicts the magnitude of the feedback mechanism. The output stage achieves a peak gain of 14.4dB at 31GHz with a maximum output power of 22dBm.**

I. Introduction

The continuous increase in cutoff frequencies (f_T, f_{max}) of SiGe BiCMOS technologies makes the latter a sensible option for the realization of millimeter-wave applications. However, with the increase of speed of these technologies the avalanche breakdown voltages (BV_{CEO} and BV_{CBO}) are reduced to values which make it hard to create a millimeter-wave power amplifier (PA) with high output power. The relative small output power of a single PA cell, in comparison to GaAs/GaN/InP PAs, can be countered by power combining several smaller cells both on-chip as off-chip.

Next to creating a high output power, it is also required to have a high PAE since this will lead to lower DC power consumption and thus lower chip temperature. Since the input power of an amplifier is factored into the PAE, this can only be achieved by having a high gain output stage. Moreover, higher gain also allows to go to a more efficient amplifier class like Class-B. This type of amplifier requires an increase in drive level of 6dB in comparison to a Class-A, which is only acceptable with a sufficiently high gain. Yielding the main reason why millimeter-wave power amplifiers are typically biased in Class-AB [1], [2].

The topology of the presented output stage is discussed in Section II of this paper together with how the BV_{CEO}-limit can be overcome. Section III, in turn, explains how the gain of the output stage is increased by applying positive feedback and also provides a formule which can give an estimate of the magnitude of the feedback response and the frequencies at which it occurs. When going to higher gain, special care has to be taken to assure stability. This is discussed in Section IV. The performance of the output stage is summarized in Section V together with a conclusion.

II. Cascode topology and transistor limitations

The output stage topology, chosen in this work, is a differential cascode topology as shown in Fig.1. Although this type of topology needs more headroom, and thus larger DC voltage, than a simple common emitter stage, it can achieve a higher output power and higher PAE. The reason for this is the biasing of the common base cascode transistor which is biased with a more or less constant emitter current. In [3] and [4] it was shown that a common base output transistor can safely be biased at a collector emitter voltage which is significantly higher than BV_{CEO}. Also, since the base of the cascode transistor has a low impedance to ground, the peak value of the time-varying collector emitter voltage can approach the avalanche breakdown limit. The reason for this is that the holes flowing back to the base created by impact-ionization are shunted to ground. As a result the maximum usable peak collector voltage approaches BV_{CBO} [1].

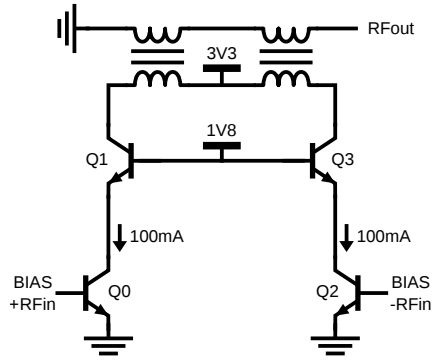

Fig. 1. Differential cascode topology with output balun used as output stage.

The 250nm SiGe BiCMOS technology used in the design of this output stage has a minimum BV_{CEO} of 2.1V and the minimum BV_{CBO} amounts to 6V. The common base output transistor is biased at a collector emitter voltage (V_{CE}) of 2.4V which is above the minimum BV_{CEO} but still safe due to the constant emitter current. Using a V_{CE} of 2.4V leads to a linear voltage swing of $3.8V_{pp}$ (with a saturation voltage of 0.5V and V_{BE} = 0.9V), while using a common emitter stage biased at a V_{CE} of 2V (considering a margin of 0.1V to be safely below BV_{CEO}) would lead to a linear swing of $3V_{pp}$. In other words, the use of a cascode topology leads to

a 2.05dB increase in linear output power while the DC power consumption goes up with a factor of 1.57 (1.96dB).
Although the efficiency η (P_{out}/P_{DC}) of a cascode is only marginally larger than the efficiency of a common emitter stage, the PAE ((P_{out} - P_{in})/P_{DC}) is significantly better due to the larger gain of a cascode and thus smaller required input power. This higher gain stems from the suppression of the miller capacitance at the input due to the cascode [5], however, in Section III it will be shown that this isn't entirely true.
In conclusion, using a cascode helps to overcome the BV_{CEO} limitation and thus achieve a higher output power. Additionally it leads to a higher gain and PAE than a simple common emitter stage.

III. Gain improvement using positive feedback

A. Cascode and Miller capacitance

The reason why a cascode is used is the suppression of the Miller capacitance at the input of the output stage and the resulting higher gain. This suppression is caused by the unity voltage gain of the common emitter transistors in a cascode configuration which leads to a zero AC voltage between the collector and base of transistors Q0 and Q2 in Fig.1 which removes feedback over the base collector capacitance and hence kills the Miller effect. Important to note here is that the unity voltage gain comes from the input impedance of a common base transistor which is approximately $1/g_m$, multiplied with the transconductance g_m of the common emitter transistor. However, it is well known that at high frequencies the input impedance of a common base transistor becomes inductive and thus will lead to a larger than one voltage gain and a return of the Miller capacitance. Hereafter it will be shown that the input impedance not only becomes inductive but also increases with the voltage gain of the common base transistors.

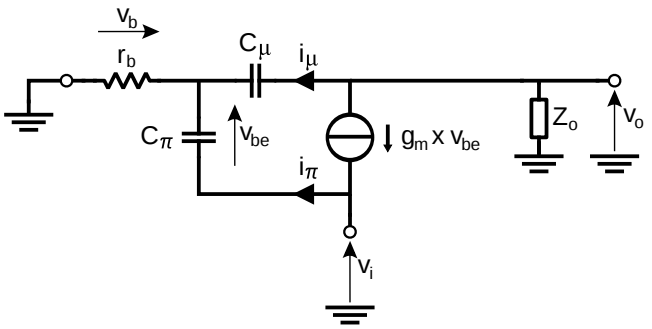

Fig. 2. Small signal representation of the common base transistor in a cascode configuration with v_i the input voltage, v_o the output voltage and Z_o the load impedance of the cascode.

In order to calculate the input impedance of common base transistors Q1 and Q3 in Fig.1, the small signal model shown in Fig.2 is used. This is a simplified version of the complete bipolar small signal equivalent circuit [6]. The impedance Z_o is the resonant load impedance of the cascode output stage with the collector to substrate capacitance C_{CS} included. The parasitic resistances r_μ and r_o can be neglected at high frequencies in comparison to C_μ and Z_o. Resistances r_{pi}, r_{ex} and r_c are left out for initial analysis but are reconsidered in the final formula describing the input impedance. The input impedance of the small signal equivalent of Fig.2 equals:

$$Z_{in} = \frac{v_i}{-g_m \cdot v_{be} + i_\pi}$$

With $v_{be} = -i_\pi / sC_\pi$ this leads to:

$$Z_{in} = \frac{v_i}{\frac{g_m \cdot i_\pi}{sC_\pi} + i_\pi} = \frac{v_i}{i_\pi \cdot \left(1 + \frac{g_m}{sC_\pi}\right)} \tag{1}$$

All that is left to do, is to solve i_π in function of v_i:

$$i_\pi = (v_i - v_b) \cdot sC_\pi \tag{2}$$

The term v_b in equation (2) can be written as:

$$\begin{aligned} v_b &= r_b \cdot (i_\pi + i_\mu) \\ &= r_b \cdot \left(i_\pi + \frac{v_o - v_b}{1/sC_\mu}\right) \\ &\dots \\ v_b &= \frac{v_o \cdot sC_\mu \cdot r_b + i_\pi \cdot r_b}{1 + sC_\mu \cdot r_b} \end{aligned} \tag{3}$$

When equation (2) and (3) are combined the following expression is found for i_π:

$$\begin{aligned} i_\pi &= \left(v_i - \frac{v_o \cdot sC_\mu \cdot r_b}{1 + sC_\mu \cdot r_b} - \frac{i_\pi \cdot r_b}{1 + sC_\mu \cdot r_b}\right) \cdot sC_\pi \\ &\dots \\ i_\pi &= \frac{v_i \cdot sC_\pi \cdot \left(1 - \frac{v_o}{v_i} \cdot \frac{sC_\mu \cdot r_b}{1 + sC_\mu \cdot r_b}\right)}{\left(1 + \frac{sC_\pi \cdot r_b}{1 + sC_\mu \cdot r_b}\right)} \\ i_\pi &= \frac{v_i \cdot sC_\pi \cdot \left(1 - A_V \cdot \frac{sC_\mu \cdot r_b}{1 + sC_\mu \cdot r_b}\right)}{\left(1 + \frac{sC_\pi \cdot r_b}{1 + sC_\mu \cdot r_b}\right)} \end{aligned} \tag{4}$$

In equation (4) the factor A_V is the voltage gain of the common base transistor. To attain a formula for the input impedance of the common base transistor equation (4) is put into equation (1) leading to the following result:

$$Z_{in} = \frac{1 + s \cdot (C_\pi + C_\mu) \cdot r_b}{(g_m + sC_\pi) \cdot [1 + sC_\mu \cdot r_b \cdot (1 - A_V)]} \tag{5}$$

The formula for the input impedance shown in equation (5) is quite remarkable since it shows that the input impedance depends on the voltage gain A_V of the common base transistor and thus also on the impedance Z_o at the output of the cascode. Since this output impedance is a resonant load made up out of the balun inductance and the C_{CS} capacitance of the common base transistors, the input impedance of the common base will increase at exactly the frequency of interest for the output stage. This means that the Miller effect, and subsequentially the Miller capacitance, will be largest at the wanted frequency thus dampening the gain. Furthermore equation (5) shows that any parasitic resistance or inductance in series with r_b will result in a large increase in input impedance and Miller capacitance.
To get a more accurate description of the input impedance the resistances r_{ex} and r_c need to be included. With some lengthy

calculus it can then be shown that the input impedance is given by:

$$Z_{in} = \frac{1 + s\left(C_\pi + C_\mu\right) \cdot r_b + sC_\mu \cdot r_c \left[1 + r_b \cdot \left(g_m + sC_\pi\right)\right]}{\left(g_m + sC_\pi\right) \cdot \left[1 + sC_\mu \cdot r_c + sC_\mu \cdot r_b \cdot \left(1 - A_V\right)\right]} + r_{ex} \cdot \left[1 + sC_\mu \cdot \left(r_b + r_c\right)\right] \quad (6)$$

In DC, equation (6) results in the familiar result $Z_{in,DC} = 1/g_m + r_{ex}$. To prove that the previous analysis is accurate, the input impedance calculated by means of formula (6) is compared to the simulated input impedance of a common base in Fig.3 and Fig.4 showing respectively the real and imaginary part of the input impedance.

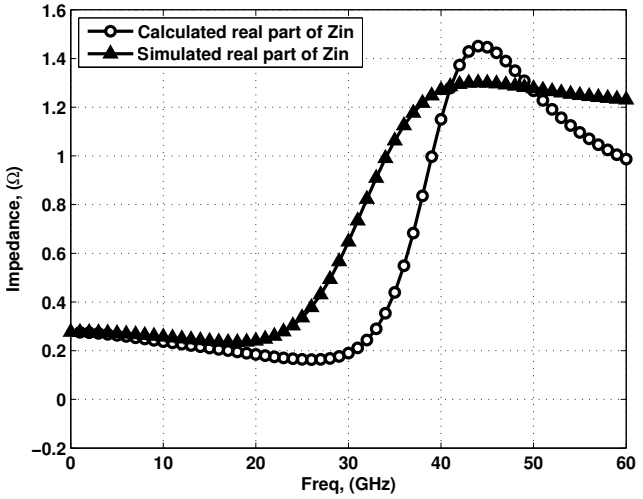

Fig. 3. Calculated real part of the input impedance of a common base transistor versus the simulated values. The resonant frequency of Z_o is 31GHz in simulation.

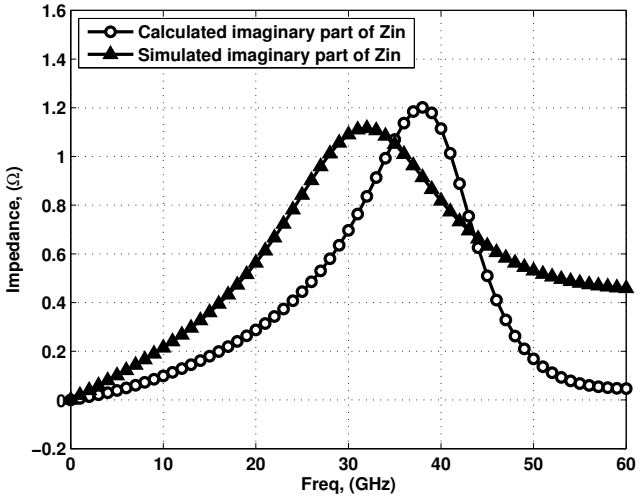

Fig. 4. Calculated imaginary part of the input impedance of a common base transistor versus the simulated values. The resonant frequency of Z_o is 31GHz in simulation.

Figures 3 and 4 show that formula (6) is able to predict the behavior of the input impedance of a common base transistor at high frequencies. It also shows that the input impedance of a common base transistor increases at the resonant frequency of the output load and thus will have a larger input capacitance for the cascode at resonance due to the Miller effect. To counter the resulting drop in gain at resonance, positive feedback can be used as will be shown hereafter.

B. Feedback mechanism and gain improvement

The output stage described in this paper uses cross-coupled feedback capacitors C_F across the collector base junction of the common emitter transistors as shown in Fig.5.

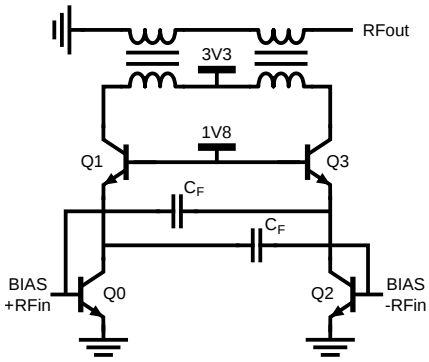

Fig. 5. Differential cascode topology with cross-coupled feedback capacitors across the common emitter transistors.

The feedback in Fig.5 works by compensating the input capacitance of the cascode with the negative capacitance provided by the cross-coupled capacitors which exploit the Miller effect. The total capacitance at the input $C_{in,tot}$ is then given by the following formula [5]:

$$C_{in,tot} = C_{in} + \left(1 - |A_{V,CE}|\right) \cdot C_F \quad (7)$$

With C_{in} the input capacitance without feedback and $A_{V,CE}$ the voltage gain of the common emitter transistors. Equation (7) shows that the total input capacitance of the cascode can be decreased by adding the cross-coupled feedback capacitors.

By adding positive feedback an increase of 2dB in gain can be noticed in Fig.6. By choosing a larger feedback capacitor an even bigger increase in gain can be achieved, however care has to be taken not to cause instability (negative $C_{in,tot}$ in equation (7)). Although an increase with a mere 2dB might not seem much, it quickly becomes significant when the output stage is biased more towards Class-B operation and the gain starts to drop. Also to reduce the linearity and gain demands of a driving stage, a difference of 2dB certainly is noteworthy.

IV. Stability considerations

An obvious source of instability comes from the cross-coupled feedback capacitors which should be limited in size to ensure stability. A much less evident source of instability stems from the parasitic capacitor between the collector and emitter of transistors Q1 and Q3 in Fig.5. This capacitor isn't present in the transistor itself but comes from layout capacitance between the collector and emitter interconnects. Especially when multiple transistors are combined in parallel for high power with small spacing to ensure bias and thermal

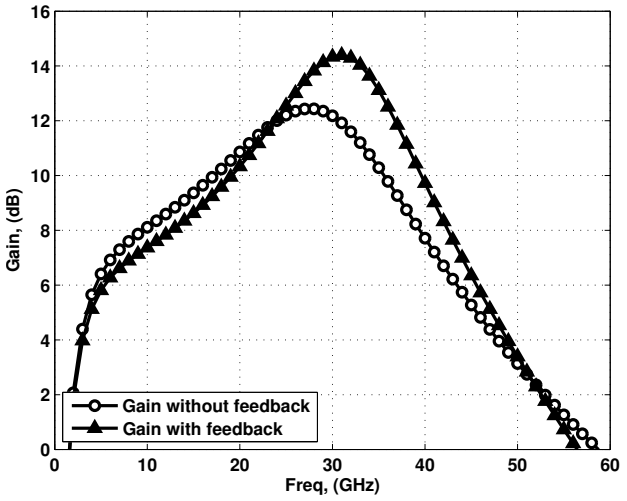

Fig. 6. Gain of the differential cascode configuration with and without the cross-coupled feedback capacitors.

stability, this capacitor becomes large and can cause instability. The basic mechanism behind this instability is the positive feedback between collector and emitter due to this capacitor as discussed in detail in [7].

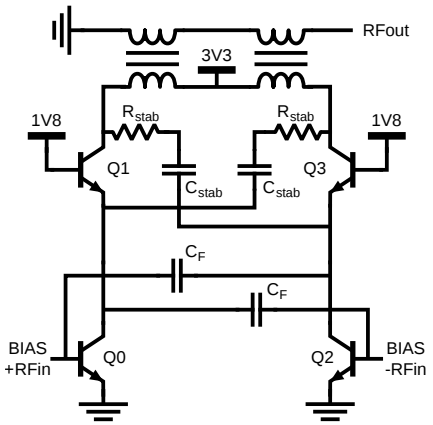

Fig. 7. Differential cascode topology with cross-coupled series resistor R_{stab} and capacitor C_{stab} across the common base transistors.

This is solved by placing a cross-coupled capacitor between the collector and emitter of the common base transistors [7]. However, this leads to a large shift in resonant frequency of the output impedance Z_o. By using a series combination of a resistor R_{stab} and capacitor C_{stab}, as shown in Fig.7, stable operation is obtained with a smaller shift in resonant frequency.

V. Conclusion and Further Work

In this paper, an analysis of an output stage design for a millimeter-wave power amplifier has been provided, highlighting the use of a cascode to achieve high gain and high output power. Furthermore a formula is derived for the input impedance of a common base stage at high frequencies which explains the drop in gain at the resonant frequency of the output load. It is also shown that this effect can be countered by applying positive feedback around the common emitter transistors by means of cross-coupled capacitors. The resulting gain for the output stage is more than 14dB at 31GHz in simulation with a maximum output power of 22dBm

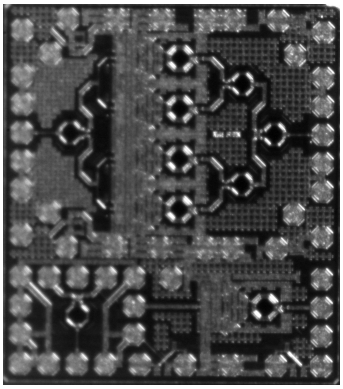

Fig. 8. Die photomicrograph of the complete amplifier together with teststructures (lower part of the die). The complete die measures 1490μm by 1670μm.

The output stage has been designed in a 250nm SiGe BiCMOS technology and is used in a four-way power combining power amplifier at a frequency of about 30GHz which has been taped-out and produced. This amplifier will be mounted directly onto a heat sink and will be probed to verify the performance.

Acknowledgments

The authors would like to thank Jeroen Missine and Bjorn Vandecasteele, both at the Centre for Microsystems Technology (TFCG Microsystems Lab), for their useful advice and help with the current and future assembly of the chips.

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