Flipchip bonding of thin Si dies onto PET foils: possibilities and applications

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Abstract

Low cost large area flexible electronic products are expected to be used in a wide range of applications and in large quantities in our society. Examples of this include sensor packages added to food or conformal intelligent patches that monitor a patient's well-being. Because of their large area, the preferred substrate material for these applications will be low cost materials like polyesters (PEN/PET). Intelligence or communicative capabilities are preferably added to these devices by integrating the chips directly on the low cost foil itself. To maintain the flexibility of the package and not to add too much to the thickness, the Si chip needs to be integrated into the product as a bare, thinned die. Flip chip bonding is currently the most mature, widely available technology to integrate these thin chips. The low temperature stability of the PET foils however puts serious constraints on the materials and the process. The current paper specifically addresses the challenges associated with this. Initial results from a finite element model will be discussed. The model is being developed to understand the influence of the bonding process and material parameters on the final stresses and warpage of the chip. Additionally, lifetime and flexural test results will be discussed of ultrathin chips bonded on Cu and Ag-based screen printed circuitry. Finally, some applications of the technology will be shown: a microcontroller integrated on a Cu-PET foil and a supply chain monitoring tag.

Key words: thin chip, flip chip, PET, large area electronics

Introduction

A new class of low cost, large area electronics is starting to emerge. Examples include cheap sensor packages attached to food packaging to measure the ripeness of food, smart patches that monitor the patient well-being and smart active or passive RFID tags.

The substrate material will not be polyimide as commonly used in flexible electronics. By using polyesters like PEN (polyethylene naphtalate) or PET (polyethylene teraphtalate), the substrate costs can be reduced by a factor of 5-10 [1]. A disadvantage of polyesters is however that they are considerably less thermally stable. PEN has a glass transition temperature (T_g) of ~130 ^oC and PET of ~85 ^oC while poly(imide) has a Tg of ~350 ^oC) [1]. This limitation in thermal stability excludes many well established processes for making electronic products and/or renders the use of existing processes much more challenging.

Printing technologies will play a key and pivotal role in manufacturing of these large area low cost electronics devices. Despite the fact that also quite advanced functionality can be made with printing, it will still for some time be needed to integrate the intelligence and communication capabilities of the device as a Si-based chip. To keep the flexibility of the device and not to add too much to its thickness, this chip will need to be integrated as a bare, thinned Si chip. Because of the low temperature stability of polyesters it is necessary to interconnect the chip using an adhesive.

A wide variety of different types of conductive circuitry types are being considered, developed and evaluated for these devices [2-8]. The circuitry can be printed using technologies like screen printing or inkjet printing by using (mostly Ag-based) conductive inks. Of these technologies, screen printing is likely the most mature. The technology is however limited in resolution to a pitch of around 150 µm. The circuitry can also be made using more traditional technologies like etching or plating of Cu through photolithographic processing. This has the advantage over printing that much finer line widths and spacings are possible and additionally that a huge installed base of equipment is already available.

The current paper specifically addresses the interconnection of ultrathin Si chips on both screen printed and etched Cu circuitry on PET foils using anisotropic conductive adhesives. Flip chip technology is chosen as the bonding method because it is existing (for example used in passive RFID tags) and has a large installed base of manufacturing equipment.

A finite element model has been developed which allows studying the influence of the various bonding parameters and material properties on the

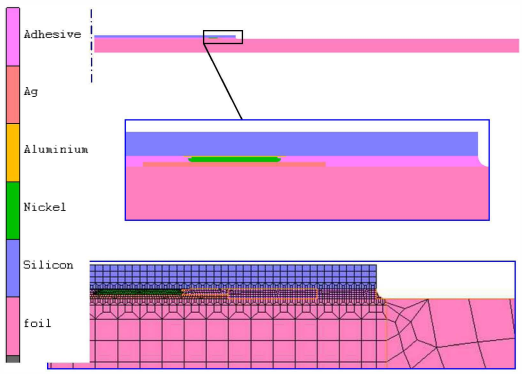

Figure 1. Cross section of modeled geometry.

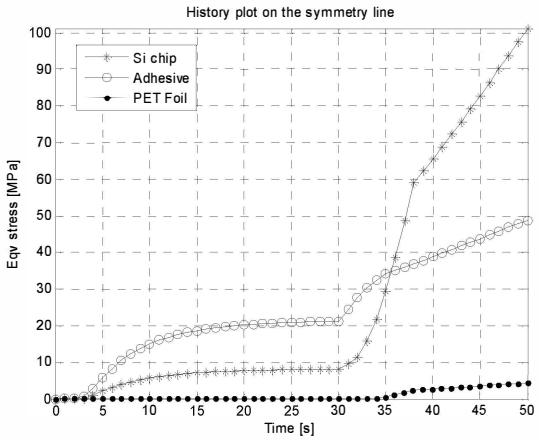

Figure 2. Stress evaluation during bonding. Stresses given as equivalent von Mises stresses. At t=0s, a temperature of 120 C is applied to cure the adhesive. At t=30s, the heating is switched off and the system is cooled down to room temperature until t=50s.

stresses in the system and the warpage (i.e. out-of-plane bending) of the ultrathin chip due to the bonding process. First results of this model will be discussed. Furthermore, it will be shown that flip chip bonding of ultrathin chips on low cost PET foils can be done reliably: a good lifetime and flexural stability has been achieved. Finally, it will be shown that the technology is ready to be used for actual applications in the field of large area low cost flexible electronics. Two examples will be shown of actual applications of the technology. The first example is a fine pitch bare chip Texas Instruments MSP430 microcontroller integrated onto a Cu-PET foil. The second example is a smart RFID food monitor tag which is being developed in the framework of the Catrene project Pasteur [9]: a sensor chip and an RFID chip on a PET foil with screen printed circuitry and battery.

Experimental

The PET foil that was used for the screen printed circuitry was a 120 µm thick thermally stabilized foil from Agfa. The conductive structures were printed using Dupont 5025 Ag-filled screen printing paste on a DEK Horizon 03i screen printer. Curing of the paste was performed in a conventional oven by heating the substrates for a period of 20 minutes at 120 ^{o}C.

The PET-Cu foils that were used for the fine pitch circuitry were obtained from Hanita Coatings. They consist of a 12 µm thick Cu layer on a 50 µm thick thermally stabilized PET foil. Etching of the Cu was performed using traditional photolithographic processing. First a mild acid cleaning and micro etching was performed. Then, a dry film resist was laminated, the substrates were exposed (7s at 10 mW/cm2), developed and spray etched in $CuCl_2$. Finally, stripping using NaOH was performed and anti-tarnish was applied.

Bonding on the screen printed circuitry PET foils was investigated using a 2 x 2 mm IZM28 daisy chain test chip having 20 IO's, a pitch of 300 µm and a thickness of 20 µm. Bonding on the Cu circuitry PET foils was investigated using a 5 x 5 mm IZM42 daisy chain test chip having 168 IO's, a pitch of 50 µm and a thickness of 20 µm.

For both circuitry types, a dedicated fan-out circuitry was made which allowed accurate 4 point (4p) measurements to be performed so as to obtain only information on the bump-circuitry contact resistance.

The flip chip bonding was performed using a Dr. Tresky T3200 semi-automatic bonder. First, the anisotropic conductive (Delo AC163) adhesive was dispensed on the foil at the bonding position of the chip. Then, the preheated teflon-coated bonding tool with the attached chip was aligned and pressed down with the appropriate force onto the foil. Bonding of the daisy chain test chips was performed at a bonding temperature of 120 ^{o}C (as measured in the adhesive) and a bonding time of 30 seconds. For the bonding on the screen printed circuitry a bonding force of 1 N was used. Bonding of the larger daisy chain test chip on the Cu-PET foil was done at a slightly higher bonding force of 2 N.

Results and discussion

Finite element modeling of bonding process

Bonding of the chip is done at an elevated temperature and under pressure. As a result of the bonding process, stresses will be introduced into the system. Si chips having a thickness below 25 µm are flexible. As a result, these stresses can cause warpage (i.e. out of plane bending) of the thin chip. A too high warpage should be prevented as it can lead to damage of the internal structures in the chip.

A generic finite element model has been developed which can simulate the full chip bonding process so as to better understand the influence of the various bonding parameters and material properties on the internal stresses and the warpage of the chip.

The geometry, boundary conditions and material parameters of bonding the IZM28 test chip on a PET

foil with screen printed circuitry have been implemented into the model, see the Experimental section. Figure 1 shows a cross section of the model.

Curing of the adhesive was modeled using the cure kinetics model from Kamal and Sourour [10] where the different parameters have been fitted on experimental data obtained from the adhesive.

Figure 2 shows the stresses in the system (shown as equivalent von Mises stresses) in each layer (silicon chip, adhesive layer and the foil) as a function of time, starting from the moment the temperature is applied during chip bonding (t=0). Nodes have been selected for each layer from the middle of the cross section.

Initially, the system is assumed to be in a stress-free state. When the temperature is applied at t=0, the adhesive is in a liquid state. As a result, the foil and the chip can expand freely with respect to each other due to heating. They will do so differently: the Si chip has a low CTE of 3 ppm/^{o}C while the PET foil has a much higher CTE (CTE < T_g: 25 ppm/^{o}C, CTE > Tg: 60 ppm/^{o}C, Tg=85 ^{o}C).

During curing, the adhesive will transform from a liquid to a solid state, thereby fixing the chip and the foil to each other. Figure 2 shows that the stress levels in the chip and adhesive rise due to the cure shrinkage. The foil will absorb the stresses by deformation due to its lowered modulus at elevated temperature.

At t=30 seconds, the heating is stopped and the system is cooled down to room temperature until t=50 seconds. As a result of the cooling, the Si chip, the adhesive and the foil will shrink. The foil and the chip can however no longer do so freely with respect to each other as they are fixed through the cured adhesive. The stresses rapidly increase, see Figure 2. This causes out-of-plane bending of both the foil and the chip. For the considered bonding conditions, the predicted chip warpage was around 10 µm (measured as the vertical upward movement of the chip center with respect to the edge of the chip). This value is acceptable [11, 12] and corresponds well with measurement values obtained earlier for this chip on this foil type [13].

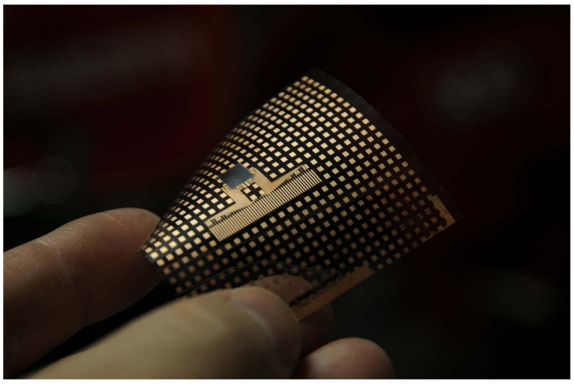

Figure 3. Photograph of 20 µm thick, 50 µm pitch daisy chain test chip bonded on Cu-PET foil

Further investigations have been performed to study how the different material and bonding parameters have an influence on the stresses in the system and warpage of the chip. This will be discussed in detail in a future paper. The results indicate that the used bonding *temperature* is the main factor that determines the stresses in the system and thus also the final chip warpage. Based on this, it can be concluded that for these low cost foils the bonding temperature should be kept as low as possible.

Initial bonding test results

Flip chip bonding experiments of the 20 µm thick daisy chain test chips were performed on both the Ag-based screen printed and on the Cu circuitry PET foils, see the Experimental section. A bonding temperature of 120 ^{o}C was used, which is the lowest possible temperature for this adhesive. For both types of circuitry a good and reproducible low contact resistance could be achieved. For the screen printed circuitry, an average bump-circuitry resistance of 63.5 ± 2.9 mOhm was obtained while for the Cu circuitry a comparable contact resistance of 64.0 ± 3.7 mOhm was obtained. Each value is the average of 8 bonded chips, having 8 measurable 4p contacts per chip. As an illustration, Figure 3 shows a photograph of the 20 µm thick, 50 µm pitch daisy chain test chip, bonded on a PET-Cu foil.

Lifetime testing

Accelerated Humidity Testing (AHT, 60 ^{o}C/90% RH) and temperature shock testing (-40 ^{o}C to +120 ^{o}C, 30 minutes cycle time) were performed to evaluate the lifetime stability of the bonds.

A total of 8 chips, each having 8 measurable contacts were prepared for each circuitry type and for each test. A protective cover layer or coating was not applied onto the chips, thus mimicking a worst case scenario for the humidity testing. The obtained humidity test results are shown in Figure 4 for the screen printed circuitry. Very similar results were obtained for the Cu-based circuitry. These results are therefore not shown.

Plotted are both the average circuitry-bump resistance (4p, Ohm) with the corresponding standard deviation (left axis) and the number of open contacts (right axis).

The accelerated humidity test results (Figure 4 top) show stable resistances up until around 100 hours of exposure. After this, the average resistance and the spread can be seen to increase. This increase is caused by a limited number of the contacts. At 500 hours of exposure, specifically these contacts showed failure. A microscope investigation showed evidence of corrosion of the bonding pads at the failed contacts.

The other contacts showed a stable resistance and a low spread for the remainder of the exposure period.

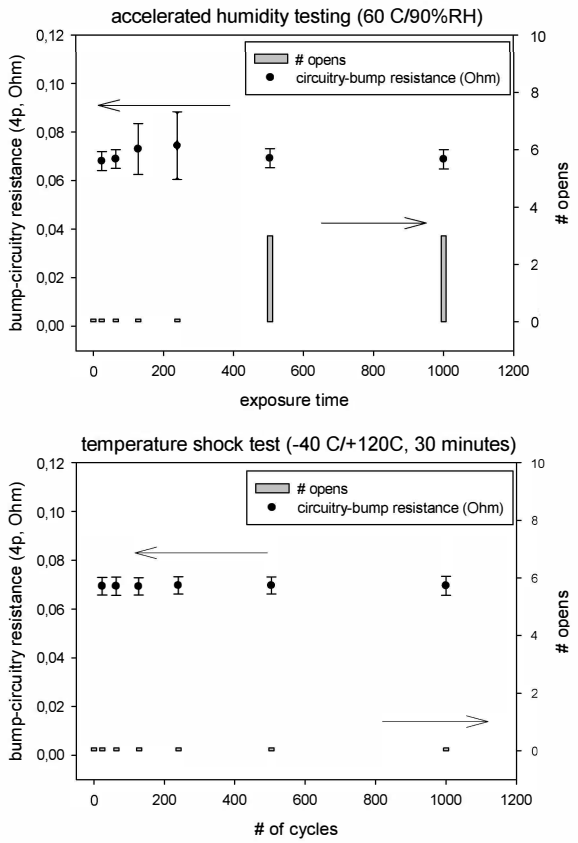

Figure 4. Top: accelerated humidity test results (AHT), Bottom: temperature shock test results (TST)

Overall, it can be concluded that the AHT are reasonably good. Further improvement of the results can be achieved by covering the chip by a protective coating or layer so as to protect it from moist. This is current being evaluated.

The temperature shock tests (-40 ^{o}C to 120 ^{o}C, 30 minutes cycle time), see Figure 4 bottom, were performed to evaluate thermal stability. The obtained results are very good: up to 1000 cycles no significant increase in resistance is observed and none of the contacts failed. This despite the fact that the T_g of the PET is traversed in each cycle.

Flexural testing

When a thin layer system is bended, it will experience tension (elongation) at its outer surface and compression (shortening) at its inner surface. Along the cross section, the strain gradually changes from compression to elongation. For pure bending, there is a position where the system neither experiences tension nor elongation. This position is denoted the 'neutral line' or 'neutral plane'. The exact position along the cross section strongly depends on the moduli and thicknesses of the different layers in the system. Because thin chips are brittle, they are preferably placed at this neutral line.

A surface mounted thin chip, like considered in the current work, will not be located at the neutral line of the system. For maximum flexibility of the system, it will therefore be preferred to cover the chip with an additional layer so as to move the neutral line to the position of the chip.

Finite element modeling and analytical calculations were performed to study the stresses that occur upon bending. The modeled system consisted of a base foil of a given thickness with an ultrathin Si chip mounted on top using a thin layer of adhesive. This system was virtually bended to a given radius by applying three point bending conditions. The same system but with a laminated top foil, having the same thickness as the base foil, was additionally modeled. The chip is then placed in the center of the laminate and should thus experience less strain, thereby improving the flexural reliability.

The results of the calculations are shown in Figure 5. Plotted is the maximum equivalent von Mises stress in the chip as a function of the reciprocal of the bending radius. Results are shown for both a 50 and a 120 µm thick base PET foil with and without a laminated cover PET foil of the same thickness.

The results show that for the 120 µm thick base foil, the stresses are roughly decreased by a factor of 2 as a result of covering it with an additional layer. For the 50 µm thick base foil, the differences are considerable less: a roughly 20% decrease in stress is observed as a result of laminating a cover foil. This difference can be explained by the fact that the thinner the base foil and the cover foil, the larger the contribution of the chip thickness to the total stack will be. In any case, the calculations clearly show that it is advisable to apply a covering layer on a surface mounted chip as it gives a significant decrease in the maximum stresses that the chip will experience.

Experiments were performed to also practically study the influence of the cover layer. Samples were prepared where 8 ultrathin chips were mounted on a 120 µm thick PET foil. Mounting was performed with the grinding and polishing lines on the chip both parallel and anti-parallel to the planned bending

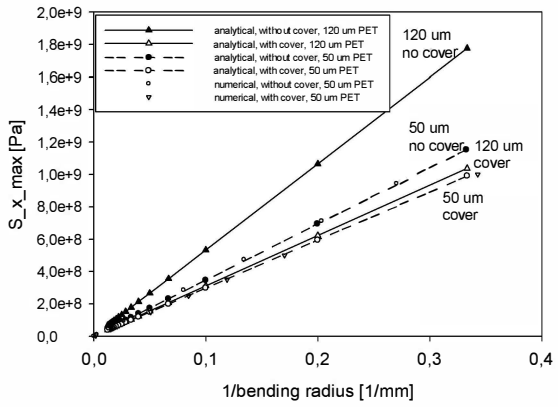

Figure 5. Analytical and numerical results of 3 point bending of an ultrathin chip bonded onto different PET foils, with and without a cover foil.

direction. Also another set of the same samples was prepared where a 120 µm cover foil was laminated. Subsequently, the samples were bended down to a diameter of 25 and 10 mm by using a custom-built flex tester.

Both types (with and without cover layer) could survive bending over a diameter of 25 mm. Also continued bending for up to 500 cycles resulted in no broken chips. The 10 mm bending diameter was more critical. The sample without a cover layer did not survive this diameter: 100% of the chips were broken already after the first cycle. The sample with a cover layer could survive this bending diameter with no broken chips for a limited number of cycles. Continued exposure up to 500 cycles however also here resulted in some broken chips where especially those mounted with the polishing marks perpendicular to the bending direction showed failure. This indicates that fatigue plays a role with the polishing marks acting as stress initiators.

Application of the technology

It has been shown above that bonding of ultrathin Si chips on low cost PET foils is feasible and results in a good lifetime and flexural reliability. Currently, the process is being applied in several applications that are under development at Holst Centre. As an illustration, two of these applications will be discussed.

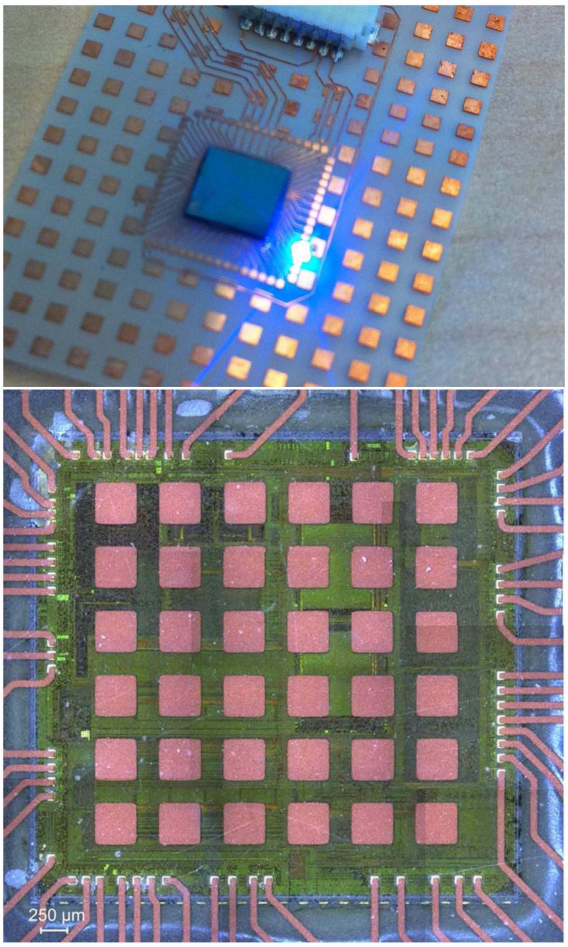

Figure 6. Top: MSP430F1611 bare die microcontroller bonded on Cu-PET foil. Bottom: bottom view microscope photograph of chip bonded to foil (looking through foil)

MSP430 microcontroller integrated onto a PET foil

Many applications require a microcontroller to be integrated to allow data processing / analysis or driving of the system. A commonly used, general purpose, low power and low cost microcontroller is the Texas Instruments MSP430. The subtype MSP430F1611 was selected for integration on a PET foil. This 16 bits microcontroller runs at 8 MHz and has for example on-board memory, clock and AD convertors. The size of the chip is 5 x 5 mm, it has 64 IO's, a pad size of 75 µm and a minimum pitch of 100 µm. Thinning and electroless Ni-Au bumping of the chips was performed in-house.

Integration of the microcontroller on a PET-Cu foil was performed successfully using the adhesive and settings discussed above. The microcontroller showed full functionality, also for a prolonged period. As an illustration, Figure 6, top side shows a photograph of the microcontroller driving a bare die 50 µm thick LED, which was mounted onto one of the IO's of the chip using an isotropic conductive adhesive. Figure 6, bottom shows a bottom view microscope photograph, looking through the foil onto the internal circuitry of the microcontroller. The microscope photograph shows a good alignment of the chip with respect to the circuitry on the foil. Currently work is being performed to also integrate a radio chip onto a PET foil.

Food monitoring tag

A good application example of a future low cost smart RFID tag is being developed in the Catrene project Pasteur which is led by NXP [9]. In this project, a wireless sensor platform is being developed to monitor the environmental conditions of perishable goods in the supply chain between producer and consumer.

The platform is based on a CMOS-based sensor chip which can measure different gases (O_2, CO_2, ethylene) but also temperature and humidity. By adding an active tag (e.g. including a battery) with this sensor chip to packaging solutions (crates, containers, boxes etc.) the quality of the product can be guaranteed more effectively throughout the supply chain.

The active RFID tag in its current form is shown in Figure 7. It consists of a PET foil with screen printed circuitry, antenna and battery (left side, not present in photograph).

Two Si chips need to be mounted on the PET foil: an RFID chip and the sensor chip. Again, flip chip attachment was used for both chips. For the RFID chip, the exact process, adhesive and conditions as discussed above have been used. The

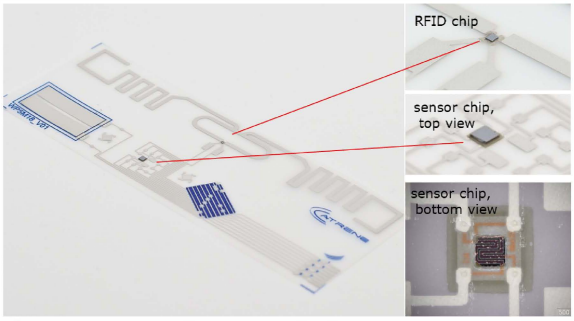

Figure 7. Photograph of smart RFID tag being developed in Catrene project Pasteur [9]

sensor chip has its functionality on the bottom side. Thus, when mounted face down, a cavity needs to be present in the foil to allow passage of gases. The assembly procedure that was used is as follows. First, a cavity was laser-machined in the foil using a 355 nm Nd:YAG laser source. Then, the anisotropic conductive adhesive was carefully dispensed around the perimeter of the cavity. Finally, the chip was flip chip mounted. The sensor chip attached to the PET foil is shown in Figure 6, bottom right hand side. Both chips were mounted successfully and showed appropriate functionality.

Conclusion

Flip chip bonding of ultrathin Si chips on low cost PET foils has been investigated on two different types of low cost electronic circuitries. Based on the experimental results it can be concluded that for both types of circuitries, a reproducible, low contact resistance and a good lifetime can be achieved. Flexural test experiments and mechanical calculations show that for small bending radii it is preferred to cover the chip with an additional layer as this can lead to significant decrease of the stress level upon bending. A finite element model has been developed to understand how the different material properties and bonding parameters influence the stresses in the system and the warpage of the ultrathin chip. First results indicate that the main stresses in the system are introduced upon cooling down of the system. Additionally, mainly the used curing temperature determines the stresses in the system and thus warpage of the chip. Finally, two examples have been shown where the developed technology has been used successfully: a bare die microcontroller and a food monitoring tag.

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