24.4 A 10Gb/s Burst-Mode TIA with On-Chip Reset/Lock CM Signaling Detection and Limiting Amplifier with a 75ns Settling Time

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Emerging symmetric 10Gb/s passive optical network (PON) systems aim at high network transmission efficiency by reducing the RX settling time that is needed for RX amplitude recovery in burst-mode (BM). A conventional AC-coupled BM-RX has an inherent tradeoff between short settling time and decision threshold droop, which makes an RX settling time shorter than 400ns hard to achieve [1]. Some techniques have been developed to overcome this limitation [1-2], demonstrating a settling time of 150 to 200ns. Our previous work [3] uses feed-forward automatic offset compensation (AOC) to achieve a response time as short as 25.6ns. However, a feed-forward scheme using peak detectors is intrinsically less accurate and results in relatively high power consumption. In this paper, we present a DC-coupled 10Gb/s BM-TIA and burst-mode limiting amplifier (BM-LA) chipset that uses a feedback type AOC circuit with switchable loop BW. This new technique is capable of removing input DC offset in less than 75ns, and offers continuous decision threshold tracking during payload, to cope with the maximum length of CID. The differential TIA output port senses a CM reset signal provided by the succeeding BM-LA, and activates an on-chip reset and lock function. This BM-LA also integrates auto reset/activity generation circuits providing the AOC BW switching signal, so that this time-critical signal is not required from the PON system.

The chipset's top-level architecture is shown in Fig. 24.4.1. When a burst arrives, BM-TIA performs a fast three-step gain switch (GS) while the activity detection circuit in BM-LA detects the start of the incoming burst. During the preamble, the offset integrator increases the AOC loop BW to achieve fast settling. The AOC BW is then switched to a smaller value, for continuous decision threshold tracking during the payload. At the end-of-burst, the BM-LA resets itself to its initial state preparing for the next burst to come. The BM-LA also sends the reset/activity signal back to the preceding BM-TIA IC by driving the input common-mode voltage V_{CM}. The BM-TIA extracts reset and gain lock signals from V_{CM} without any performance penalty.

As shown in Fig. 24.4.2, the BM-TIA reset/lock CM detection circuit contains CM extraction, a differentiator, two comparators and a RS latch with a delayed output. The differentiator is a passive HPF circuit converting the square wave V_{CM} into high frequency spikes V_{DF}. A reset pulse is generated via comparison to V_{REF2} at the V_{CM} falling edge. At the V_{CM} rising edge, when the positive spike V_{DF} crosses the threshold voltage V_{TH1}, the RS latch sets the lock after an additional delay T_{GS} for gain switch settling. The $R_{DF}C_{DF}$ time constant is made short compared to the burst guard time but large enough to generate the reset pulse robustly over PVT corners. Because of simultaneous DM and CM signaling at the 10Gb/s BM-TIA output, mode conversions between DM and CM must be taken into account as the conversion ratio can be significant in the GHz frequency range. Since V_{CM} only switches during the guard time and the preamble period, CM-to-DM conversion is no problem when the data payload is received. However, DM-to-CM conversion, partly due to mismatches in PCB conductor lengths and loading conditions, generates CM noise that might cause false gain reset/lock signaling. Therefore an LPF capacitor, C, is inserted in the CM extraction circuit, and the comparators are implemented as two-stage amplifiers with an output LPF (formed by R_2 and C_2) to remove high-frequency CM ripple.

In BM-LA, instead of using a *RC* low-pass filter in the AOC [4], the offset is cancelled by means of an offset integrator (Fig. 24.4.3) loop with adjustable loop BW. For small signals, the AOC loop BW is proportional to the unity-gain frequency of the integrator ~ gm/C_L. As the transconductance of the input differential pairs (Q_1-Q_2 for $V_{1+/-}$ and Q_3-Q_4 for $V_{2+/-}$) scales with the emitter current, the loop BW can be adapted by changing the tail currents I_{ss1} and I_{ss2}. In BM operation, the control logic clears the charge accumulated in the integrator with a PMOS switch M_5 during the guard time between bursts. It also generates a switching signal to control the AOC loop BW. When *BW_Switch* is high, the offset integrator has a large AOC loop BW due to a large tail current. When *BW_Switch* is low, the tail current is reduced and so the small loop BW minimizes the data-dependent jitter. As shown in Fig. 24.4.3, the control logic deasserts the *Clear* signal when *activity* is high, and asserts it when *reset* is high; the *BW_Switch* replicates the *Clear* signal, with an additional $T_{settling}$ delay as required for the BM-LA AOC settling.

The auto reset/activity circuits were designed to accommodate new requirements of emerging 10G-GPONs: a FEC code is now mandatory in order to extend the optical power budget. In previous work [5], the reset generation circuit measured the time since the last received "1" level, and a reset was generated when this time exceeded the longest CID time. Although this technique works well at low BER (e.g. 10^{-10}), it starts to miss resets when the BER rises. In the new reset generation circuit (Fig. 24.4.4), two counters, a data counter and a clock counter, count the number of rising edges of the data stream (V_3) and the clock signal ClockLS, respectively. ClockLS has a clock period of the duration of the maximum CID. The data counter is compared to *CountData*, which represents the number of bit errors allowed during the auto-reset generation. The clock counter is compared to *CountClk*, which defines the data counting time. Both *CountData* and *CountClk* are programmable. When no more than *CountData* rising edges occur before *CountClk* clock periods expire, a reset signal is generated. In this way it is avoided that a reset is missed in case one or a few bits would be wrong at a pre-FEC BER [6].

The BM-TIA and BM-LA ICs are fabricated in a 0.13µm SiGe BiCMOS process. The BM-TIA and BM-LA consume 200 and 430mW, respectively, at 2.5V and 2.2V. Figure 24.4.5 shows BM-TIA output, BM-LA output and reset/activity CM signaling waveforms. Figure 24.4.6 shows the measured BERs with and without an off-chip reset signal. With an off-chip reset signal, the measured BM-RX settling time is 50ns over the whole input optical power range (-5dBm down to -31.2dBm). Allowing for 75ns of settling time, the sensitivity penalty from using the on-chip reset/activity generation instead of an off-chip reset signal is limited to 0.4dB at BER = 10^{-10}. The eye diagrams in Fig. 24.4.6 prove the superior CID tolerance: after 64-, 128- and 512-bit CID, the measured total jitter J_{pp} is 22.7ps, 23.1ps, and 23.8ps respectively. Fig. 24.4.7 shows die micrographs. The BM-TIA occupies 1.28×1.02mm^2 and the BM-LA occupies 1.21×.26mm^2.

Acknowledgement:
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[6] C. Mélange, et al., "Circuit for End-of-Burst Detection," US patent application US 2011/0069952 A1.

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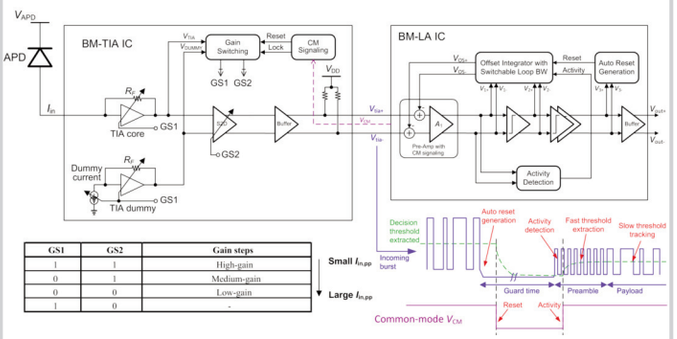


Figure 24.4.1: Top level architecture of BM-TIA and BM-LA.

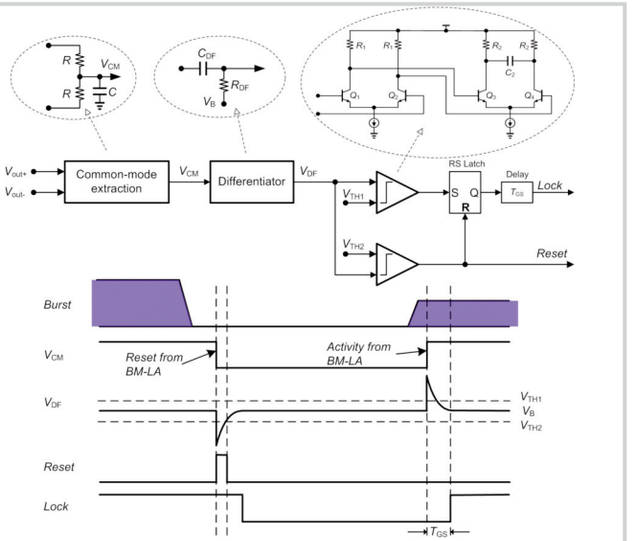


Figure 24.4.2: CM signaling detection circuit.

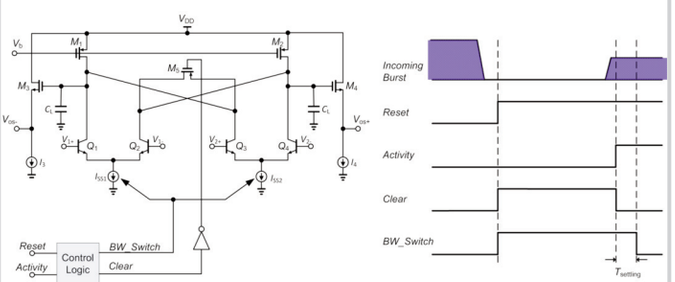


Figure 24.4.3: Offset integrator with switchable loop BW.

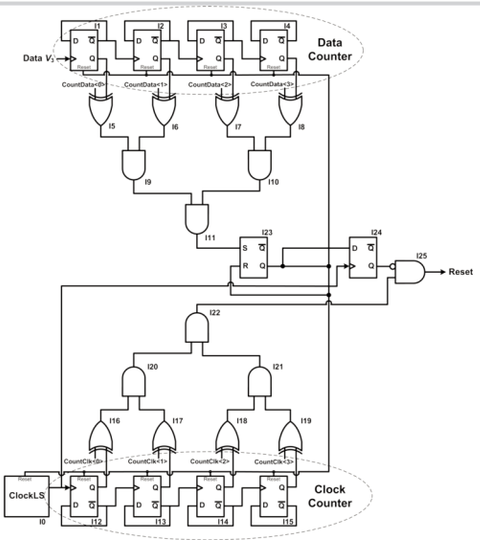


Figure 24.4.4: On-chip reset generation.

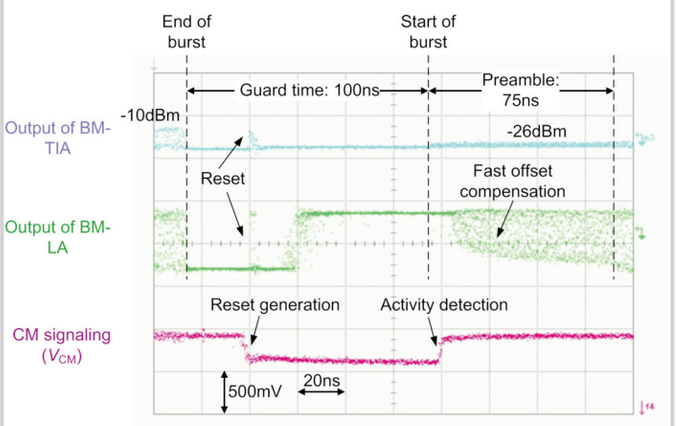


Figure 24.4.5: BM-TIA output, BM-LA output and reset/activity CM signaling waveforms.

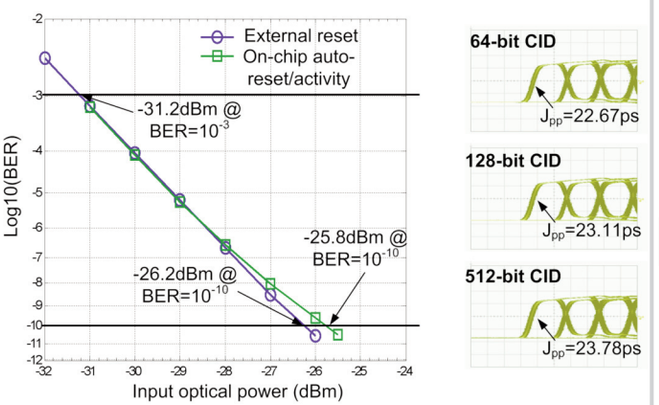
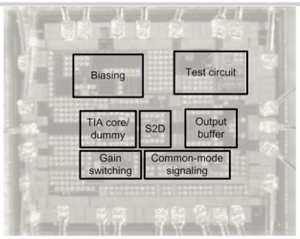
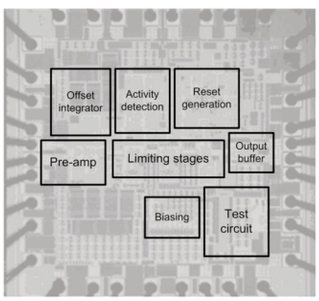


Figure 24.4.6: Measured BERs and total jitters.



BM-TIA



BM-LA

Figure 24.4.7: Die micrograph of BM-TIA and BM-LA.

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