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Active and passive component embedding into low-cost plastic substrates aimed at smart system applications

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Abstract

The technology development for a low-cost, roll-to-roll compatible chip embedding process is described in this paper. Target applications are intelligent labels and disposable sensor patches. Two generations of the technology are depicted. In the first version of the embedding technology, the chips are embedded in an adhesive layer between a copper foil and a PET film. While this results in a very thin (< 200 µm) and flexible system, the single-layer routing and the incompatibility with passive components restricts the application of this first generation. The double-sided circuitry embedding technology is an extension of the single-sided, foil-based chip embedding, where the PET film is replaced by a second metal foil. To obtain sufficient mechanical strength and to further reduce cost, the adhesive film is replaced by a substrate material which is compatible with the chip embedding concept. Both versions of the foil-based embedding technology are very versatile, as they are compatible with a broad range of polymer materials, for which the specifications can be tuned to the final application.

Key words

Chip embedding, System-in-Foil, smart system, low-cost.

I. Introduction

Key properties required for the broad acceptance of smart systems are low cost, thin, large area, lightweight, flexibility, conformability, and even stretchability [1]. Realizing a smart system that combines all these properties requires research and development of new integration technologies that take into account these requirements from the start. Integrating ultra-thin chips on low-cost plastic substrates offers cost reduction, increased flexibility, higher functional density and lower weight. Targeted application areas for these integration technologies range from smart packaging labels and medicine blisters to intelligent lighting systems and phototherapeutic devices.

The use of ultra-thin bare dies, having thicknesses down to 20 µm, allows for thin and flexible systems, but requires pitches that are not compatible with current state-of-the art printing technologies. Polyester films with copper metallization make pitches below 100 µm possible at a cost comparable to that of printed circuitry. The low thermal stability of the PET foils, however, puts serious constraints on the integration process and materials, rendering many conventional integration technologies unfeasible.

Recently, a foil-based chip embedding technology was jointly developed by Holst Centre and imec [2], [3]. In contrast to fan-out WLP [4] and chip embedding in rigid or flexible printed circuit boards [5], [6], where cost reduction is achieved by scaling to larger panel sizes, low-cost was a main development goal of this chip embedding technology. The roll-to-roll compatible process flow starts by placing naked dies and thin passive components on a bare copper foil using anisotropic and isotropic conductive adhesive, respectively. The actual embedding is performed by laminating a thermoplastic polyurethane film and a second copper sheet onto the copper foil with the components. Interconnections between the two metal foils are realized by laser drilling and metallization of the vias. In the final step, the copper is structured, resulting in a thin Cu-based

circuitry foil with embedded components. The advantages of this approach in comparison to other hybrid integration methods based on low-cost materials are the removal of temperature limitations for die bonding, mechanical and physical protection of the chip and the realization of a flat surface which allows for direct access to the contacts of the chip. This new approach was demonstrated in a complete flat, 250µm thick, flexible smart label, including two embedded chips, 10 embedded passives, integrated antenna and sensor circuitry, and two-layer routing.
This paper starts with a detailed description of two generations of the foil-based embedding technology. Section III describes the smart label demonstrator, which highlights the capabilities of the foil-based embedding technology.

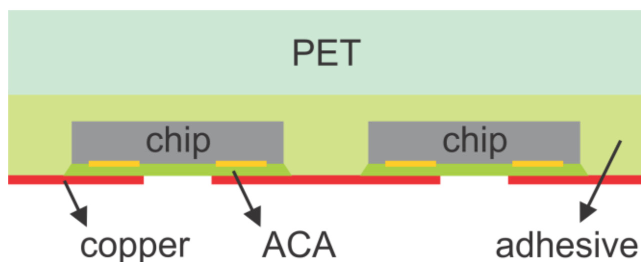

Fig. 1 Concept of single-layer, foil-based embedding

II. Foil-based embedding technology

Two generations of the foil-based embedding technology were developed. In the first version of the embedding technology (*Fig. 1*), the chips are embedded in an adhesive layer between a copper foil and a PET film. While this results in a very thin (< 200 µm) and flexible system, the single-layer routing and the incompatibility with passive components restricts the application of this first generation.
The double-sided circuitry embedding technology (*Fig. 2*) is an extension of the single-sided, foil-based chip embedding, where the PET film is replaced by a second metal foil. To obtain sufficient mechanical strength and to further reduce cost, the adhesive film is replaced by a substrate material which is compatible with the chip embedding concept.
The process flow for both generations starts with a single copper foil, including laser-drilled markings for the alignment of the following process steps. In the first step the components are mounted on a metal foil using isotropic or anisotropic conductive adhesive. In the double-sided circuitry embedding technology also thin passive components are embedded so the outer surface of the final system is completely flat.

1. Component placement on copper foil

2. Embedding

3. Structuring

4. Via drilling

5. Via filling

Fig. 2 Process flow for double-sided chip embedding

The actual embedding of the chips in the first generation of the technology is performed in a lamination step using PET film and a suitable adhesive[1]. Void-free lamination, ensuring a good encapsulation of the chips, is a crucial step in the chip embedding process. Due to the combination with PET film, the lamination temperature is limited to a maximum of 120 °C for a few minutes. The adhesive needs to combine good adhesion to copper and PET with a good flow behavior to successfully enclose the chips. Typical dimensions are a chip thickness of 30 µm, a 20 µm die bond adhesive layer, and a 50 µm thick PET film. The adhesive surrounding the chips will be about 70 µm to 100 µm in total, resulting in an overall thickness of less than 200 µm.
A significant number of different general-purpose industrial adhesive types were evaluated, ranging from pressure sensitive tapes, over thermoplastic or thermosetting film adhesives, to UV curing liquid adhesives. Details on the material selection process can be found in [2]. Overall, the pressure-sensitive tapes and the heat-activated films offered the best compromise between cost, processability and embedding performance.
Due to the limitation in adhesive thickness, it is not possible to embed thicker components, such as passives. This is a major restriction on the applicability of the technology, as the advantage of a flat and accessible surface are nullified by mounting the necessary passive components. Complex systems-in-foil may also require more than one signal layer.
Instead of laminating a PET film with a suitable adhesive,

[1] Unless explicitly mentioned otherwise, the word “adhesive” in the following always refers to the adhesive used to encapsulate the chips.

the embedding material now acts as a substrate layer, with a metal circuit layer on both sides. Next to a good flow for embedding and sufficient adhesion to the metal foil, the selection criteria for substrate materials also include the necessary properties for serving as a substrate for flexible electronic circuitry. Depending on the application, dimensional stability, thermal resistance, tear resistance and flexibility can be specified. All these parameters, along with the material cost, should be taken into account during the material selection. The method for applying the material to the metal foil with the chips depends on the nature of the polymer material. Laminating film materials is the preferred option.

A thermoplastic polyurethane film from Epurex is the embedding material of choice. The lamination parameters were optimized using the IPC-TM-650-2.3.17.1b flow test (*Resin Flow of Adhesive Coated Films and Unsupported Adhesive Films*). The goal of this optimization was to obtain good flow while minimizing squeeze-out of the material. The results show that the lamination time has more influence on the flow than the pressure, but a higher pressure can give more flow for short lamination times. The second part of the lamination parameter optimization is performed using dummy silicon chips of 50 µm thickness mounted on a 20 µm die attach tape. Laminating at a lower temperature (*easier handling*) and pressure (*less risk of chip cracking*) is preferred at the expense of a longer lamination time. More details on the lamination parameter optimization can be found in [3]. *Fig. 3* and *Fig. 4* show a good flow without voids for the embedding of dummy silicon chips and passive components, respectively.

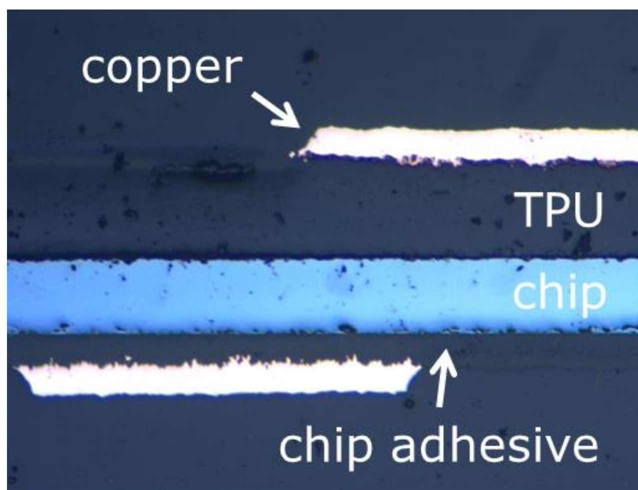

Fig. 3 Cross section of a dummy silicon chip (50 µm thickness) embedded in a thermoplastic polyurethane substrate between two copper layers

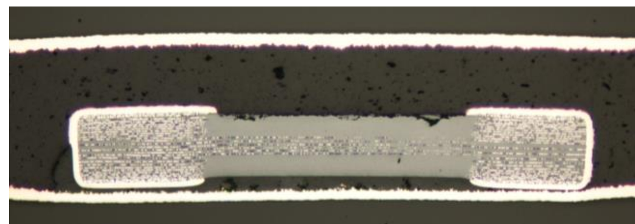

Fig. 4 Cross section of a 150 µm-thick passive component embedded in a thermoplastic polyurethane substrate between two copper layers

Interconnections between the two copper layers are realized by drilling blind via holes through the TPU substrate and subsequently filling these vias with a conductive paste. The via drilling is performed using a CO_2 laser followed by a cleaning step using a KrF excimer laser. The process for via filling that was developed at the Holst Centre has already proven its functionality and is thus the method of choice for realizing the via interconnections [7]. The conductive paste needs to combine a low viscosity for via filling with ensuring a reliable, low-resistance contact to both copper layers. Initial trials with the via interconnect process revealed undercutting due to excessive laser drilling and air entrapment after filling. Further optimization of both process steps resulted in a blind via with a desired tapering and void-free filling (*Fig. 5*).

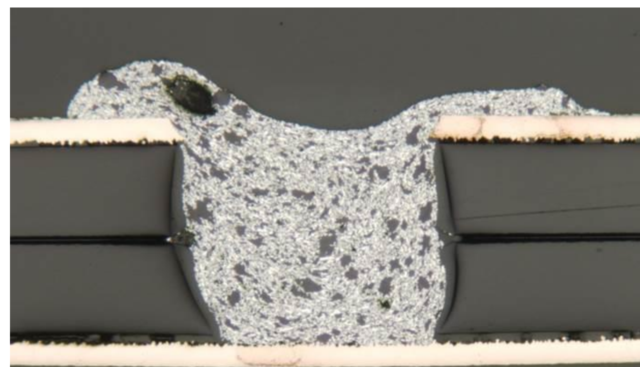

Fig. 5 Blind via interconnection with good filling

In a final step, the copper is structured using conventional PCB processes or alternative patterning technologies to define the circuitry. The end result is a thin foil with embedded components and copper interconnects. An important challenge with respect to the copper structuring is the dimensional stability of the TPU substrate. The consecutive temperature steps during processing introduce deformations, imposing limitations on the alignment budget. As a result, it is difficult to scale the technology to pitches below 100 µm.

III. Smart label demonstrator

Cost-effective intelligent sensor patches for use in a variety of smart packaging applications are a natural target for the foil-based embedding technology. The demonstrator of choice is a versatile smart sensing label that can be combined with a humidity, amine or ethylene sensor. The system design is the result of collaboration between the SiF and the WATS sensor program at the Holst Centre in Eindhoven [8]. The smart label consists of a microcontroller to perform the measurements, translate the electrical signals into data and store the data with a time stamp in a memory; together with a NFC radio chip that can transmit the data to most recent smart phones or to a dedicated reader. Next to the chips, a number of passive components, an integrated antenna, an integrated humidity sensor and a flexible battery are also part of the smart label.

Two chips and all 10 passive components are embedded in a complete flat, 250µm thick, flexible smart label. The die size of the micro controller (a Texas Instruments MSP430F1611) is 4.6 mm by 4.4 mm and the minimum pad pitch is 100 µm. The NFC radio chip (ST Microelectronics M24LR64-R) is a lot smaller (2.0 mm by 1.5 mm) and has only 10 I/Os. The passive components were selected based on their thickness and are a mixture of 01005 and 0201 components. The design includes an integrated planar antenna and an interdigitated humidity sensor circuitry. A total of 10 layer transitions are present. The transitions to the battery connection at the back and bridge for the antenna are realized by placing multiple vias in parallel.

Fig. 6 shows an overview of the functional smart label demonstrator, indicating the location of the micro controller, radio chip, antenna and humidity sensor. The close ups of the embedded micro controller and the radio chip, seen through the die attach adhesive, show the routing of the interconnections to the chips.

IV. Conclusion

Two generations of an embedding technology based on low-cost plastic materials are presented in this paper. The first generation of the technology embeds the chip between a copper foil and a PET film, offering maximum thickness reduction with single-layer routing. The second generation makes it possible to also embed passive components and allows for more complex routing schemes.

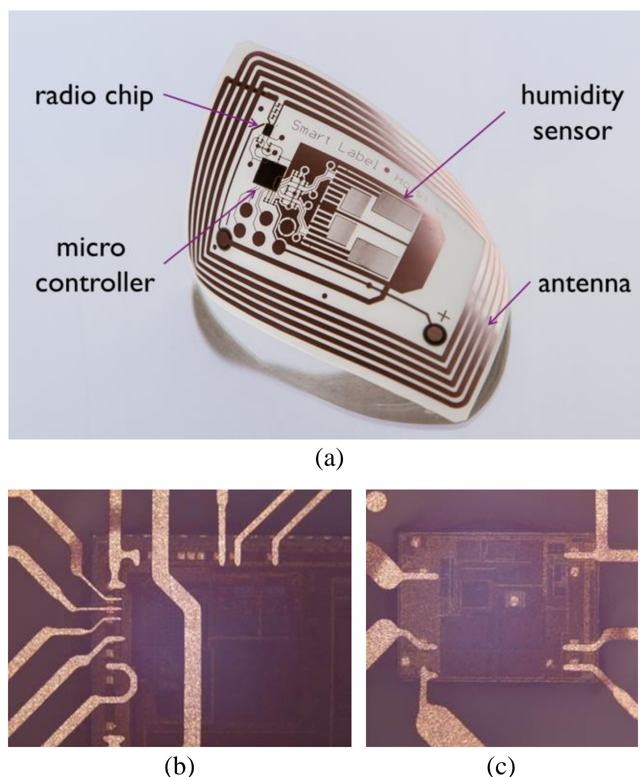

Fig. 6 Overview of the smart label demonstrator (a), with a close up the micro controller (b) and the radio chip (c)

A functional demonstrator is realized in the form of a smart label, capable of wireless monitoring of temperature and humidity. Two embedded chips, 10 embedded passives, and integrated antenna and sensor circuitry are all incorporated in a complete flat, 250µm thick, flexible smart label.

Preliminary stress testing indicates that further optimization of the technology, mainly with respect to material choice, is required to achieve the desired reliability. Only then, a cost comparison to alternative technologies for realizing smart labels can be made in a consistent manner.

The foil-based embedding technology is very versatile, as it is compatible with a broad range of polymer materials, for which the specifications can be tuned to the final application. By completely embedding all of the components into the substrate, mounting this system-in-foil to other subsystems becomes easier. The direct access to the contacts of the chip also helps to reduce the complexity of interconnecting multiple subsystems, such as power generating foils, sensor nodes or flexible displays.

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