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Experimental Validation of a Proposed Single-Phase Five-Level Active Rectifier Operating with Model Predictive Current Control

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Abstract—**This paper presents a model predictive current control applied to a proposed single-phase five-level active rectifier (FLAR). This current control strategy uses the discrete-time nature of the active rectifier to define its state in each sampling interval. Although the switching frequency is not constant, this current control strategy allows to follow the reference with low total harmonic distortion (THD$_F$). The implementation of the active rectifier that was used to obtain the experimental results is described in detail along the paper, presenting the circuit topology, the principle of operation, the power theory, and the current control strategy. The experimental results confirm the robustness and good performance (with low current THD$_F$ and controlled output voltage) of the proposed single-phase FLAR operating with model predictive current control.**

Keywords—Five-Level Active Rectifier; Model Predictive Current Control; Power Quality.

I. INTRODUCTION

The active rectifiers have many advantages when compared with the traditional solutions based on diode rectifiers, multi-pulse rectifiers, and hybrid passive rectifiers [1]. Sinusoidal input current with controlled power factor and controlled output voltage are the main advantages [1][2][3]. The best known converter that meets with these requirements is the power-factor-correction (PFC), i.e., a converter that is composed by diode-bridge rectifier followed by a dc-dc boost-type converter. The main PFC converters based in dc-dc converters, buck, boost, buck-boost, and forward are reviewed in [4]. More specifically, in [2] are reviewed some PFC converters only based in the dc-dc boost converter. Besides these converters, in the literature can also be found PFC converters based in the Cuk converter and in the three-state switching cell [5][6]. A set of PFC bridgeless converters that allow to reduce the switching and conduction losses, when compared with the conventional PFC, is proposed in [7]. In this context, in [8] is presented a review about bridgeless or dual-boost converters, i.e., the PFC symmetrical and asymmetrical bridgeless converters [9][10]. Another relevant PFC converter that can be found in the literature is the interleaved converter. This converter combines two or more conventional PFC converters [3]. Other relevant group of PFC converters are the multi-level converters. In references [11] and [12] exhaustive reviews about this type of converter are

presented. The main advantage of these converters is the possibility to reduce the volume and size of the passive filters. In counterpart, these converters require more resources of hardware and software. Globally, the fundamentals about active rectifiers are summarized in [13][14][15].

In this paper is proposed a single-phase five-level active rectifier (FLAR). Taking into account that this active rectifier is classified as multi-level, it allows to reduce the voltage stress in the semiconductors, and the volume and size of the passive filters [16]. Fig. 1 shows the circuit topology of the proposed FLAR. This converter is composed by four IGBTs and four diodes, by a split dc-link voltage, and by an inductive filter to couple the FLAR to the power grid. This converter is based in the PFC asymmetrical bridgeless (one leg of IGBTs and other of diodes), however, it is uses a bidirectional cell between the active leg (IGBTs) and the middle point of the dc-link.

The classical current control strategies for active rectifiers are based in predictive strategies, hysteresis-band, linear-control, sliding mode, and so on [17][18]. In the scope of this paper, it is used the model predictive current control with finite control set to define the state of the active rectifier in each sampling interval [19][20]. Model predictive control has been successful applied to power electronics converters, e.g., dc-dc, H-bridges, and matrix [21][22][23]. For such purpose, it is used the discrete-time model of the converter and a cost function. In this paper, during each sampling period, a function cost is used to minimize the error between the measured current and its reference [23]. In section II is presented the circuit topology and the principle of operation of the proposed active rectifier, while in section III is described the model

Fig. 1. Circuit topology of the single-phase five-level active rectifier (FLAR).

Fig. 2. Operation stages of the single-phase five-level active rectifier (FLAR): (a)-(c) When $v_g>0$; (d)-(f) When $v_g<0$.

predictive current control. In section IV are presented the experimental validation for a rated power of 450 W, and in section V the main conclusions are presented.

II. PRINCIPLE OF OPERATION

This item presents the principle of operation of the proposed single-phase FLAR. As presented in Fig. 2, there are six operation stages that defining the state of the active rectifier (three for each semi cycle). These six states and the correspondent voltage v_{cv} (voltage produced by the FLAR) are presented in the Table I.

TABLE I
POSSIBLE STATES OF THE FIVE-LEVEL ACTIVE RECTIFIER (FLAR)

	g1	g2	g3	g4	v_{cv}
$v_g>0$	0	0	0	0	$+V_{CC}$
	0	0	1	0	$V_{CC}/2$
	1	0	0	0	0
$v_g<0$	0	1	0	0	0
	0	0	0	1	$-V_{CC}/2$
	0	0	0	0	$-V_{CC}$

During the positive semi cycle the active rectifier can produce three distinct voltage levels: 0, $+V_{CC}/2$ and $+V_{CC}$. When the voltage varies between 0 and $+V_{CC}/2$: (a) The inductor L stores energy from the power grid and the current circulates through the diode $d1$ and the IGBT $g1$ (cf. Fig. 2(a)); (b) The inductor L delivers energy to the dc-link capacitor $C1$ and the current circulates through the diodes $d1$ and $d3$, and the IGBT $g3$ (cf. Fig. 2(b)). When the voltage varies between $+V_{CC}/2$ and $+V_{CC}$: (a) The inductor L stores energy from the power grid and the current circulates through the diodes $d1$ and $d3$, and the IGBT $g3$ (cf. Fig. 2(b)); (b) The inductor L delivers energy to the dc-link capacitors $C1$ and $C2$ through the diode $d1$ and the reverse diode of the IGBT $g2$ (cf. Fig. 2(c)). Fig. 3 shows in detail the grid current (i_g) and the gate pulses of the IGBTs $g1$, $g2$, $g3$ and $g4$. More specifically, in Fig. 3(a) when the voltage varies between 0 and $+V_{CC}/2$, and in Fig. 3(b) when the voltage varies between $+V_{CC}/2$ and $+V_{CC}$.

During the negative semi cycle the active rectifier can produce another set of voltage levels: 0, $-V_{CC}/2$ and $-V_{CC}$. When the voltage varies between 0 and $-V_{CC}/2$: (a) The inductor L stores energy from the power grid and the current circulates through the diode $d2$ and the IGBT $g2$ (cf. Fig. 2(d)); (b) The inductor L delivers energy to the dc-link capacitor $C2$ and the current circulates through the diodes $d2$ and $d4$, and the IGBT $g4$ (cf. Fig. 2(e)). When the voltage varies between $-V_{CC}/2$ and $-V_{CC}$: (a) The inductor L stores energy from the power grid and the current circulates through the diodes $d2$ and $d4$, and the IGBT $g4$ (cf. Fig. 2(e)); (b) The inductor L delivers energy to the dc-link capacitors $C1$ and $C2$ through the diode $d2$ and the reverse diode of the IGBT $g1$ (cf. Fig. 2(f)). Fig. 4 shows in detail the grid current (i_g) and the gate pulses of the IGBTs $g1$, $g2$, $g3$ and $g4$. More specifically, in Fig. 4 (a) when the voltage varies between 0 and $-V_{CC}/2$, and in Fig. 4 (b) when the voltage varies between $-V_{CC}/2$ and $-V_{CC}$.

III. MODEL PREDICTIVE CURRENT CONTROL

The control of the FLAR is structured in three main steps: (a) The power theory for obtaining the grid current reference; (b) The predictive model based in the circuit equations; (c) The cost function for minimizing the error between the grid current and its reference. In order to the proposed converter operates as an active rectifier, the grid current must be directly proportional to the power grid voltage. Therefore, the grid current reference should be in accordance with:

$$i_g{}^* = G\, v_g ,\qquad(1)$$

where G denotes a conductance seen from the power grid. Taking into account that the proposed converter operates with unitary power factor, the active power in the ac side is defined by:

$$P_G = V_G\, I_G ,\qquad(2)$$

where, V_G and I_G denotes the rms values of the power grid voltage and current, respectively. Therefore, the conductance G is defined by:

$$G = \frac{P_G}{V_G{}^2}.\qquad(3)$$

Fig. 3. Detail of the grid current (i_g) and gate pulses of the IGBTs $g1$, $g2$, $g3$ and $g4$: (a) When the voltage (v_{cv}) varies between 0 and $+V_{CC}/2$; (b) When the voltage varies between $+V_{CC}/2$ and $+V_{CC}$.

Fig. 4. Detail of the grid current (i_g) and gate pulses of the IGBTs $g1$, $g2$, $g3$ and $g4$: (a) When the voltage (v_{cv}) varies between 0 and $-V_{CC}/2$; (b) When the voltage varies between $-V_{CC}/2$ and $-V_{CC}$.

The power P_G can be divided between the power to maintain the dc-link regulated (P_C) and the dc power in the load (P_{DC}). Therefore, (3) can be rewritten by:

$$G = \frac{P_C + P_{DC}}{V_G{}^2}, \tag{4}$$

where, P_C is obtained from a PI controller. Substituting (4) in (1), the instantaneous reference for the grid current is defined by:

$$i_g{}^* = \frac{P_C + P_{DC}}{V_G{}^2} v_g. \tag{5}$$

Using this reference of current, if the power grid voltage has harmonic content, then the grid current will also have. In order to avoid this drawback, it is used a phase-locked loop algorithm. From Fig. 1, analyzing the voltages and currents between the power grid and the active rectifier it can be established that:

Fig. 5. Example of the state selection during the positive semi cycle.

$$v_g = v_L + v_{cv}, \tag{6}$$

where, v_L denotes the voltage across the input L filter and v_{cv} the voltage produced by the active rectifier. Substituting the voltage across the input L filter by the time derivative of its current multiplied by its inductance, it can be established:

$$v_g = L\frac{dv_L}{dt} + v_{cv}. \tag{7}$$

Using the forward Euler method, (7) can be rewritten in terms of discrete samples according to:

$$v_g[k] = L\left(\frac{i_g[k+1] - i_g[k]}{T_s}\right) + v_{cv}[k]. \tag{8}$$

Taking into account that the grid current is the variable that must be controlled during the next sampling period, (8) can be rewritten by:

$$i_g[k+1] = i_g[k] + \frac{T_s}{L}\left(v_g[k] - v_{cv}[k]\right).. \tag{9}$$

The final stage of the control is to minimize the error between the predicted current ($i_g[k+1]$) and the reference of current ($i_g^*[k+1]$). As presented in [19], the reference of current in the instant $[k+1]$ can be extrapolated from the samples in the instants $[k]$, $[k-1]$, $[k-2]$, and $[k-3]$, according by:

$$i_g{}^*[k+1] = 4i_g{}^*[k] - 6i_g{}^*[k-1] +$$
$$+ 4i_g{}^*[k-2] - i_g{}^*[k-3]. \tag{10}$$

During each sampling period, the cost function for minimizing the error is defined by:

$$g[k+1] = \left\| i_g{}^*[k+1] - i_g[k+1] \right\|^2. \tag{11}$$

The error is zero when the cost function defined in (11) is zero. In each sampling period is selected a state of the FLAR to minimize the error. As aforementioned, there are three states for the positive semi cycle and also three states for the negative semi cycle. Fig. 5 shows an example of the state selection during the positive semi cycle. As it can be seen, between the three possible states, the slightest error (Δi_{g2}) is obtained when is selected the state defined by {0,0,1} (i.e., when the IGBT $g3$ is on).

IV. EXPERIMENTAL VALIDATION

Fig. 6 shows the experimental setup used during the experimental validation of the FLAR. The model predictive control is implemented in the DSP TMS320F28335 from

Fig. 6. Experimental setup used for experimental validation of the FLAR.

TABLE II
SPECIFICATION OF THE EXPERIMENTAL SETUP

Parameters	Value	Unit
Power Grid Voltage	115	V
Grid Frequency	50	Hz
Maximum Output Power	450	W
Dc-link Voltage	170	V
Total Power Factor @ Full Load	0.99	-
THD$_F$% @ Full Load	2.8	-
Maximum Switching Frequency	20	kHz
Inductor L	3	mH
Dc-link Capacitors C_1, C_2	2	mF

Texas Instruments. The voltages and currents are measured with the LEM sensors LV-25 P and LA-55 P, respectively. The power converter uses the IGBTs FGA25N120ANTD from Fairchild Semiconductors and the diodes IR HFA15PB60 from International Rectifier. The gate drivers are based in the optocoupler HCPL3120 from Avago Technologies and the isolated dc-dc sources NMV1515SC from Murata.

The experimental results were obtained with a digital Yokogawa DL708E digital oscilloscope and a Fluke 435 Power Quality Analyzer. The FLAR was connected to a power grid voltage of 115 V, 50 Hz and the experimental results were obtained for a load power of 450 W. The specification of the experimental setup and value of the passive filters are shown in Table II. Fig. 7 shows the dc-link voltage, i.e., the voltage in each capacitor. As it can be seen, there are three stages until the dc-link voltage reach the maximum value of 170 V. In a first stage, initially the dc-link voltage is zero and when the active rectifier is connected to the power grid the dc-link voltage increases until it reaches about 160 V. In this process, an auxiliary pre-charge circuit is used. In a second stage, the dc-link voltage is slowly regulated to the maximum value of 170 V. In a third stage, the load is connected to the active rectifier and, as it can be seen, the dc-link voltage in each capacitor remains controlled. Fig. 8 shows in detail the grid current, the power grid voltage (v_g), and the voltage produced by the FLAR (v_{cv}) for a power of 450 W. In this case, the minimum current ripple is 0.47 A and the maximum switching frequency is 10 kHz. It is also important to refer that the grid current (i_g) is in phase with the power grid voltage (v_g), i.e., the proposed active rectifier operates with unitary power factor. Fig. 9 shows the spectral analysis and THD$_F$ (2.8%) of the grid current (i_g). Fig. 10 shows the power grid voltage (v_g), the grid current (i_g), the voltage produced by the converter (v_{cv}), and the

Fig. 7. Experimental results of the dc-link voltage (V_{DC1} and V_{DC2}: 20 V/div) showing the three stages until the dc-link voltage reach the rated value of 170 V (85 V in each capacitor).

Fig. 8. Experimental results showing in detail the grid current (i_g: 1 A/div), the power grid voltage (v_g: 50 V/div) and the voltage produced by the FLAR (v_{cv}: 50 V/div).

dc-link voltage (V_{DC1} and V_{DC2}). Fig. 10(a) shows that the grid current is sinusoidal even when the power grid voltage has harmonic content (THD$_F$% of 2.7%). It is also possible to observe that the power grid voltage (v_g) and the grid current (i_g) are in phase. Fig. 10(b) shows the output voltage produced by the FLAR. In this figure, it is possible to observe the five distinct voltages, i.e., $+V_{CC}$, $+V_{CC}/2$, 0, $-V_{CC}/2$, and $-V_{CC}$. Fig. 10(c) shows the dc-link voltage, i.e., the voltage in each capacitor. As it can be seen, the voltage in each capacitor is controlled for 85 V in order to obtain a dc-link voltage of 170 V. Fig. 11 shows in detail the voltage produced by the converter (v_{cv}), the grid current (i_g), and the digital values of the grid current (i_g) in comparison with its reference (i_g*). The grid current changes during each sampling period, however, the

Fig. 9. Experimental results showing the spectral analysis and THDi% (2.8%) of the grid current (i_g).

Fig. 10. Experimental results of the power grid voltage (v_g: 100 V/div), grid current (i_g: 5 A/div), voltage produced by the converter (v_{cv}: 100 V/div), and dc-link voltage (V_{DC1} and V_{DC2}: 20 V/div).

Fig. 11. Experimental results of the voltage produced by the converter (v_{cv}: 50 V/div), grid current (i_g: 2 A/div), and digital values of the grid current (i_g) in comparison with its reference (i_g*).

Fig. 12. Experimental result of the grid current reference (i_g*: 5 A/div) and grid current (i_g: 5 A/div) in X-Y mode.

switching frequency is not equal to the switching sampling. As aforementioned, when $v_g > 0$, during the state {0,0,0,0} the voltage produced by the FLAR is $+V_{DC}$, during the state {0,0,1,0} the voltage produced is $+V_{DC}/2$, and during the state {1,0,0,0} the voltage produced is 0. On the other hand, when $v_g < 0$, during the state {0,0,0,0} the voltage produced by the converter is $-V_{DC}$, during the state {0,0,0,1} the voltage produced is $-V_{DC}/2$, and during the state {0,1,0,0} the voltage produced is 0. Fig. 12 shows the grid current (i_g) in function of its reference (i_g*). These results were obtained in order to show that the grid current (i_g) varies linearly with its reference.

Using the model predictive current control applied to the FLAR, the switching frequency is not fixed. Moreover, during a power grid cycle, the total number of switching is not equal for all the IGBTs. In order to verify this situation it was implemented a digital algorithm to count each switching of each IGBT. Fig. 13 shows the voltage produced by the converter (v_g), the grid current (i_g), and the number of switching of each IGBT ($g1$, $g2$, $g3$, and $g4$). These experimental results were obtained with a digital-to-analogue

converter. Fig. 13(a) shows the voltage produced by the active rectifier (v_{cv}). Fig. 13(b) shows the grid current (i_g). Fig. 13(c) shows the number of commutations of the IGBT $g1$. The registered number of commutations was 40 when $v_g > 0$. Fig. 13(d) shows the number of commutations of the IGBT $g2$. In this case, the registered number of commutations was 40 when $v_g < 0$. Fig. 13(e) shows the number of commutations of the IGBT $g3$. This IGBT is only used when $v_g > 0$ and the registered number of commutations was 100. Fig. 13(f) shows the number of commutations of the IGBT $g4$. This IGBT is only used when $v_g < 0$ and the registered number of commutations was also 100. These values of commutation, are due to the inductance value and the switching sampling, e.g., increasing the inductance value will increase the number of commutations.

Fig. 13. Experimental results of the voltage produced by the active rectifier (v_{cv}: 40 V/div), the grid current (i_g: 5 A/div), and the number commutations of each IGBT ($g1$, $g2$, $g3$, and $g4$).

V. CONCLUSION

This paper proposes a single-phase five-level active rectifier (FLAR) operating with model predictive current control. Along the paper is described in detail the implementation and the principle of operation of the FLAR, as well as the power theory for obtaining the grid current reference, the predictive model based in the circuit equations, and the cost function for minimizing the error between the grid current and its reference. The experimental results show that the control algorithm is suitable to regulate the dc-link voltages, to obtain the five-level voltages, and to track the reference of the current. The model predictive current control allows to follow the reference with low total harmonic distortion (THD_F). With the active rectifier connected to a power grid voltage of 115 V and for an operating power of 450 W, the measured current THD_F was 2.8%. Globally, the experimental results confirm that the proposed FLAR, operating with model predictive current control, is suitable for obtaining a low current THD_F and controlled output voltage.

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REFERENCES

[1] Bhim Singh, Brij N. Singh, Ambrish Chandra, Kamal Al-Haddad, Ashish Pandey, Dwarka P. Kothari, "A Review of Single-Phase Improved Power Quality AC-DC Converters," IEEE Trans. Ind. Electron., vol.50, no.5, pp.962-981, Oct. 2003.

[2] Oscar García, José A. Cobos, Roberto Prieto, Pedro Alou, Javier Uceda, "Single Phase Power Factor Correction: A Survey," IEEE Trans. Power Electron., vol.18, no.3, pp.749-755, May 2003.

[3] Fernando Beltrame, Leandro Roggia, Luciano Schuch, José Renes Pinheiro, "A Comparison of High Power Single-Phase Power Factor Correction Pre-Regulators," IEEE ICIT Industrial Technology, pp.625-630, Mar. 2010.

[4] Huai Wei, Issa Batarseh, "Comparison of Basic Converter Topologies for Power Factor Correction," IEEE Proceedings of Southeastcon, pp.348-353, Apr. 1998.

[5] Bo-Tao, Yim-Shu Lee, "Power-Factor Correction Using Cuk Converters in Discontinuous-Capacitor-Voltage Mode Operation," IEEE Trans. Ind. Electron., vol.44, no.5, pp648-653, Oct. 1997.

[6] Grover Victor Torrico-Bascopé, Ivo Barbi, "A single phase PFC 3 kW converter using a three-state switching cell", IEEE Power Electronics Specialists Conference, vol.5, pp.4037–4042, June 2004.

[7] André De Bastiani Lange, Thiago Batista Soeiro, Márcio Silveira Ortmann, Marcelo Lobo Heldwein, "Three-Level Single-Phase Bridgeless PFC Rectifiers," IEEE Trans. Power Electron., vol.30, no.6, pp.2935-2949, June 2015.

[8] From Duplicate 2 (Performance Evaluation of Bridgeless PFC Boost Rectifiers - Huber, Laszlo; Jang, Yungtaek; Jovanovic, Milan M.) Laszlo Huber, Yungtaek Jang, Milan Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifier," IEEE Trans. Power Electron., vol.23, no.3, pp.1381-1390, May 2008.

[9] Roberto Martinez, Prasad N. Enjeti, "A High-Performance Single-phase Rectifier with Input Power Factor Correction," IEEE Trans. Power Electron., vol.11, no.2, pp.311-317, Mar. 1996.

[10] Jee-Woo Lim, Bong-Hwan Kwon, "A Power-Factor Controller for Single-Phase PWM Rectifiers," IEEE Trans. Ind. Electron., vol.46, no.5, pp.1035-1037, Oct. 1999.

[11] José Rodríguez, Jih-Sheng Lai, Fang Zheng Peng, "Multilevel Inverters: A Survey of Topologies, Controls, and Applications," IEEE Trans. Ind. Electron., vol.49, no.4, pp.724-738, Aug. 2002.

[12] Jih-Sheng Lai, Fang Zheng Peng, "Multilevel Converters-A New Breed of Power Converters," IEEE Trans. Ind. Appl., vol.32, no.3, pp.509-517, May 1996.

[13] Johann W. Kolar, Thomas Friedli, "The Essence of Three-Phase PFC Rectifier Systems—Part I," IEEE Trans. Power Electron., vol.28, no.1, pp.176-198, Jan. 2013.

[14] Thomas Friedli, Michael Hartmann, Johann W. Kolar, "The Essence of Three-Phase PFC Rectifier Systems—Part II," IEEE Trans. Power Electron., vol.29, no.2, pp.543-560, Feb. 2014.

[15] T. B. Soeiro, T. Friedli, J. W. Kolar, "SWISS Rectifier – A Novel Three-Phase Buck-Type PFC Topology for Electric Vehicle Battery Charging," IEEE Applied Power Electronics Conference and Exposition, pp. 2617-2624, Feb. 2012. .

[16] Rasoul Shalchi Alishah, Daryoosh Nazarpour, Seyed Hossei Hosseini, Mehran Sabahi, "Novel Topologies for Symmetric , Asymmetric , and Cascade Switched-Diode Multilevel Converter With Minimum Number of Power Electronic Components," IEEE Trans. Ind. Electron., vol. 61, no.10, pp.5300–5310, Oct. 2014.

[17] Leonardo Augusto Serpa, "Current Control Strategies for Multilevel Grid Connected Inverters," PhD Thesis, Swiss Federal Institute of Technology, Zurich, 2007.

[18] Patricio Cortés, Marian P. Kazmierkowski, Ralph M. Kennel, Daniel E. Quevedo, José Rodríguez, "Predictive Control in Power Electronics and Drives," IEEE Trans. Ind. Electron., vol.55, no.12, pp.4312–4324, Dec. 2008. .

[19] Venkata Yaramasu, Marco Rivera, Bin Wu, Jose Rodriguez, "Model Predictive Current Control of Two-Level Four-Leg Inverters—Part I: Concept, Algorithm, and Simulation Analysis," IEEE Trans. Power Electron., vol.28, no.7, pp.3459-3468, July 2013.

[20] Marco Rivera, Venkata Yaramasu, Jose Rodriguez, Bin Wu, "Model Predictive Current Control of Two-Level Four-Leg Inverters—Part II: Experimental Implementation and Validation," IEEE Trans. Power Electron., vol.28, no.7, pp.3469-3478, July 2013. .

[21] Petros Karamanakos, Tobias Geyer, Stefanos Manias, "Direct Model Predictive Current Control of DC-DC Boost Converters," EPE/PMEC International Power Electronics and Motion Control Conference, pp.1-8, Sept. 2012.

[22] Patricio Cortés, Alan Wilson, Samir Kouro, Jose Rodriguez, Haitham Abu-Rub, "Model Predictive Control of Cascaded H-Bridge Multilevel Inverters," IEEE Trans. Power Electron., vol.57, no.8, pp.2691-2699, Aug. 2010.

[23] Samir Kouro, Patricio Cortés, René Vargas, Ulrich Ammann, José Rodríguez, "Model Predictive Control — A Simple and Powerful Method to Control Power Converters," IEEE Trans. Ind. Electron., vol.56, no.6, pp.1826–1838, June 2009.