Etched Parallelogram Patterns with Sides Along <100> and <n10> Directions in 25 wt % TMAH

Milče M. Smiljanić, Žarko Lazić, Branislav Radjenović, Marija Radmilović-Radjenović, Vesna Jović
Milena Rašljić, Katarina Cvetanović Zobenica, Ana Filipović,

***Abstract*— In this paper, we present and analyze etching of parallelogram patterns in the masking layer on a (100) silicon in 25 wt % TMAH water solution at the temperature of 80 ^{0}C. Sides of parallelogram islands in the masking layer are designed along <n10> and <100> crystallographic directions. A 3D simulation of the profile evolution from these patterns during etching of silicon using the level set method is also presented. We determined all crystallographic planes that appear during etching in the experiment and obtained simulated etching profiles of these 3D structures. A good agreement between dominant crystallographic planes through experiments and simulations is obtained.**

***Index Terms*—silicon; wet etching; TMAH; simulation; level set method.**

I. INTRODUCTION

Because of its advantages to other etchants (high selectivity to thermal oxide, very smooth etching surface, integrated circuits process compatibility), wet etching of a (100) silicon substrate in tetramethylammonium hydroxide (TMAH) water solution was intensively studied [1-26]. Etched silicon shapes are limited by the mask pattern designs and the etching anisotropy of TMAH water solution. Because of the differences in etch rates [2-8] during anisotropic wet etching some crystallographic planes will appear, while others will disappear. The most used etching patterns in the masking layer in the fabrication of various sensors and actuators were rectangular patterns with sides along <110> and <100> crystallographic directions. In the previous studies of silicon wet etching [1-26], processes were conducted using various etching solutions of TMAH at different temperatures and silicon wafers of various crystallographic orientations. Etching of square patterns with sides along <100> crystallographic directions was analyzed in [9,25]. Etching of octagonal patterns with sides along <210>, <310> and <410> crystallographic directions was discussed in [9] for TMAH water solutions. In our previous paper [25], we studied silicon etching of square and circle patterns in the masking layer when 25 wt % TMAH water solution is used at the temperature of 80 ^{0}C. The sides of square patterns in the masking layer were designed along predetermined <n10> crystallographic directions. Authors in [26] explored etching of a (110) silicon using parallelogram patterns with sides along <110> and <210> crystallographic directions.

This paper presents our further work on a (100) silicon etching in 25 wt % TMAH water solution at the temperature of 80 ^{0}C. For the first time etching of parallelogram patterns in the masking layer with sides that are designed along determined crystallographic directions <n10> (1<n<10) and <100> is analyzed. A 3D simulation of the profile evolution from these patterns islands during etching of silicon based on the level set method is presented. The level set method for evolving interfaces belongs to the geometric type of methods, and it is specially designed for profiles that can develop sharp corners, change of topology and undergo orders of magnitude changes in speed. All simulations are performed using a three-dimensional (3D) anisotropic etching simulator based on the sparse field method for solving the level set equations, described in our previous publications [27-33]. Pictures of the simulated etching profiles are rendered by Paraview visualization package [34]. We presented the simulated etching profiles and SEM micrographs to demonstrate all exposed crystallographic planes. Our aim is to observe and analyze the appearance of crystallographic planes and verify agreement of simulation with experimental results. Knowing the evolution of crystallographic planes during etching enables easy fabrication of various 3D silicon structures that can be used in the design of sensors and actuators.

II. EXPERIMENTAL WORK

Phosphorus-doped {100} oriented 3” silicon wafers (Wacker, SWI) with mirror-like single or double side polished

---

Milče M. Smiljanić is with the Institute of Chemistry, Technology and Metallurgy-Centre of Microelectronic Technologies (IHTM-CMT), University of Belgrade, Njegoševa 12, 11000 Belgrade, Serbia (e-mail: smilce@nanosys.ihm.bg.ac.rs).

Žarko Lazić is with the Institute of Chemistry, Technology and Metallurgy-Centre of Microelectronic Technologies (IHTM-CMT), University of Belgrade, Njegoševa 12, 11000 Belgrade, Serbia (e-mail: zlazic@nanosys.ihm.bg.ac.rs).

Branislav Radjenović is with the Institute of Physics, University of Belgrade, Pregrevica 118, 11080 Belgrade, Serbia (e-mail: bradjeno@ipb.ac.rs).

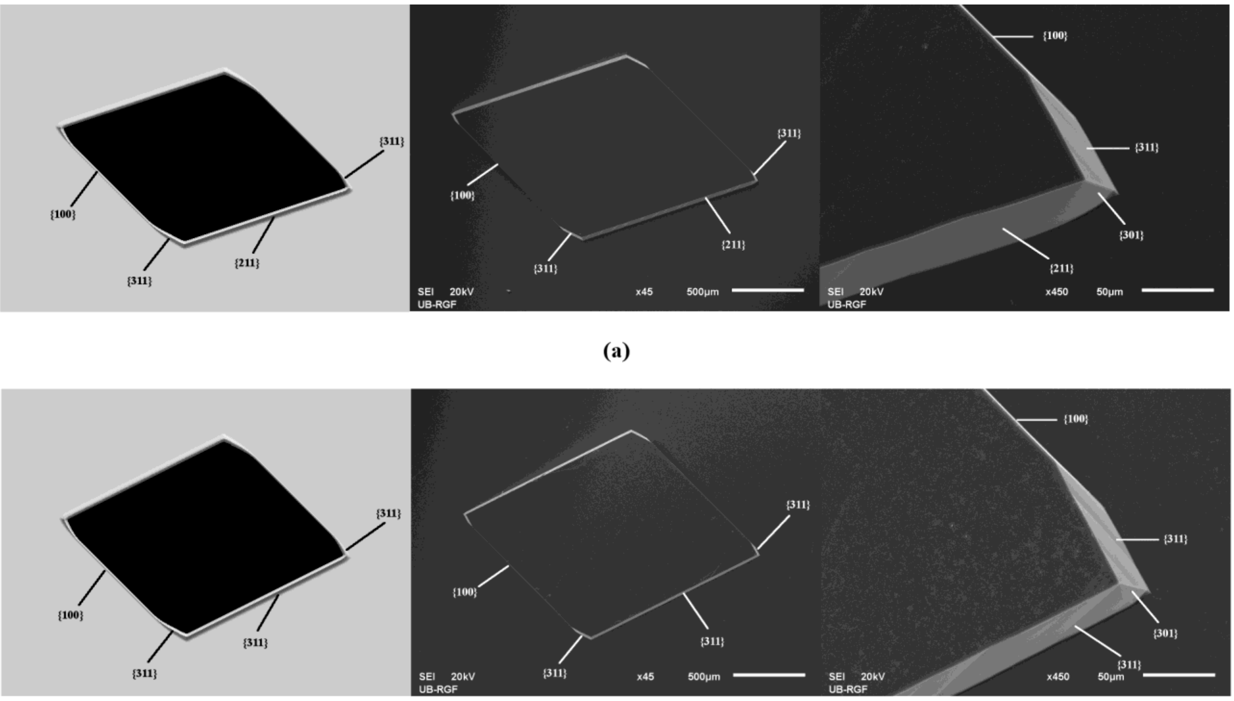
Marija Radmilović-Radjenović is with the Institute of Physics, University of Belgrade, Pregrevica 118, 11080 Belgrade, Serbia (e-mail: marija@ipb.ac.rs).

Vesna Jović is with the Institute of Chemistry, Technology and Metallurgy-Centre of Microelectronic Technologies (IHTM-CMT), University of Belgrade, Njegoševa 12, 11000 Belgrade, Serbia (e-mail: vjovic@nanosys.ihm.bg.ac.rs).

Milena Rašljić is with the Institute of Chemistry, Technology and Metallurgy-Centre of Microelectronic Technologies (IHTM-CMT), University of Belgrade, Njegoševa 12, 11000 Belgrade, Serbia (e-mail: milena@nanosys.ihm.bg.ac.rs).

Katarina Cvetnović Zobenica is with the Institute of Chemistry, Technology and Metallurgy-Centre of Microelectronic Technologies (IHTM-CMT), University of Belgrade, Njegoševa 12, 11000 Belgrade, Serbia (e-mail: katarina@nanosys.ihm.bg.ac.rs).

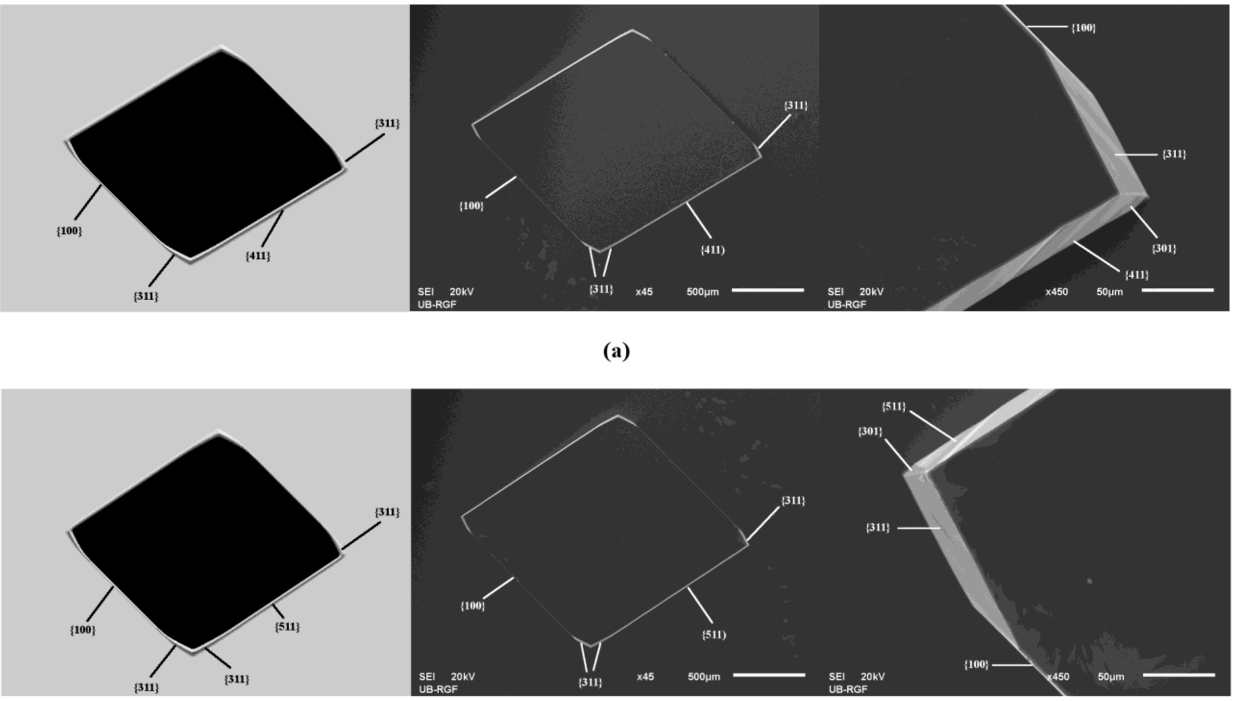
Ana Filipović is with the Institute of Chemistry, Technology and Metallurgy-Centre of Microelectronic Technologies (IHTM-CMT), University of Belgrade, Njegoševa 12, 11000 Belgrade, Serbia (e-mail: ana@nanosys.ihm.bg.ac.rs).



(a)

(b)

Fig. 1. Simulated etching profiles and SEM micrographs of the etched parallelogram patterns with sides along <100> and: (a) <210> directions; (b) <310> directions. Enlarged details of etched acute angles in the masking layer in both cases.



(a)

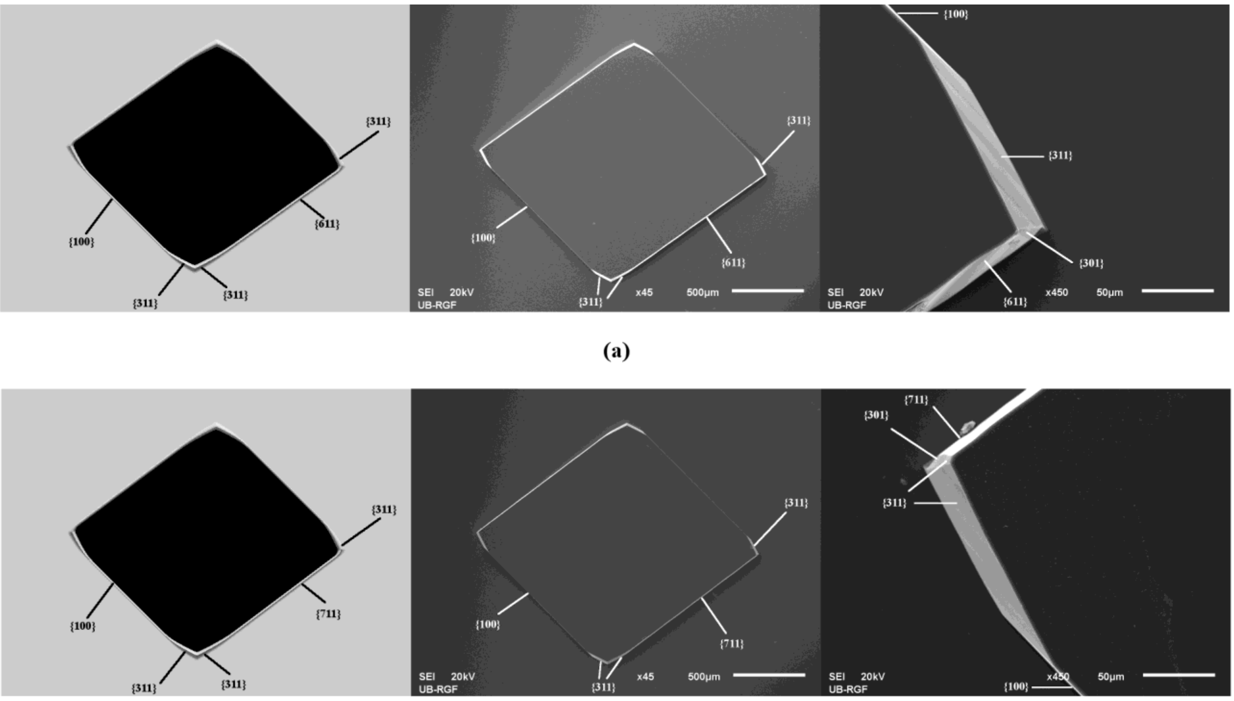
(b)

Fig. 2. Simulated etching profiles and SEM micrographs of the etched parallelogram patterns with sides along <100> and: (a) <410> directions; (b) <510> directions. Enlarged details of etched acute angles in the masking layer in both cases.

surfaces and 1-5 Ωcm resistivity have been used. Anisotropic etching has been done in pure TMAH 25 wt. % water solution (Merck). The etching temperature was 80 ^{0}C. Wafers were standard cleaned and covered with SiO_2 thermally grown at 1100 ^{0}C in an oxygen ambient saturated with water vapour (at least 1 μm thick). SiO_2 was etched in BHF in a photolithographic process in order to define parallelogram patterns along determined crystallographic directions. Again, wafers were subjected to standard cleaning procedure and were dipped before etching for 30 s in HF (10 %) to remove native SiO_2 followed by rinsing in deionized water. Etching of whole 3” wafer was carried out in a thermostated glass vessel containing about 0.8 dm^3 of the solution with electronic temperature controller stabilizing temperature within ±0.5 ^{0}C. The vessel was on the top of a hot plate and closed with a teflon lid that included a water-cooled condenser to minimize evaporation during etching. The wafer was oriented vertically in a teflon basket inside the glass vessel. Throughout the process, the solution was electromagnetically stirred with a velocity of 300 rpm. After reaching the desired depth, the wafer was rinsed in deionized water and dried with nitrogen.

III. RESULTS AND DISCUSSION

Parallelogram patterns in the masking layer are designed with sides that are along determined crystallographic directions <n10> (1<n<10) and <100>. The acute corners of islands in the masking layer formed by <n10> and <100> crystallographic directions are larger than 45^0 and smaller than 90^0. The values of acute corners are given in Table 1. Different 3D shapes are obtained during etching of silicon in 25 wt %. In the cases of n<7 during etching initial acute angles are split into two angles in the masking layer. In the case of n=2, they are acute and obtuse angles. In the case of n=3, they are right and obtuse angles. In other cases, we have two obtuse angles. The sidewalls of the first convex corners angle are defined only by {n11} and {311}-{301} (or {401}-{203}) families at the beginning of etching [25], as shown in Fig. 1-3. This is similar to the etching of square patterns in the masking layer with sides along <n10> crystallographic directions [25]. The sides of obtuse convex corners angles are defined by {100} and {311} families at the beginning of etching. In the cases of 6<n<10 during etching initial acute angles are split in three obtuse angles in the masking layer The sidewalls of the central convex corners angles are defined by two planes of {311} families at the beginning of etching [25], as shown in Fig. 3-4. This is similar to the etching of square pattern in the masking layer with sides along <100> crystallographic directions [25]. The sidewalls of two other obtuse convex corners angles are defined by {100} and {311} families or {n11} and {311}-{301} (or {401}-{203}) families. The etch depth in Fig. 1-4 is 55 μm. Appearance of {301} families is hard to observe in the simulated etching profiles. These planes have smaller surface areas than the dominant ones. The planes obtained in the simulation are more round and the edges of the convex corners tend to soften [12-13,25].



(a)

(b)

Fig. 3. Simulated etching profiles and SEM micrographs of the etched parallelogram patterns with sides along <100> and: (a) <610> directions; (b) <710> directions. Enlarged details of etched acute angles in the masking layer in both cases.

TABLE I
THE VALUES OF ACUTE ANGLES OF THE PARALLELOGRAMS

Crystallographic direction <n10>	Acute angle [^{o}]
<210>	63.4
<310>	71.6
<410>	76
<510>	78.7
<610>	80.5
<710>	81.9
<810>	82.9
<910>	83.7

The etching of island obtuse corners in the masking layer is the same for all cases except n=2, as shown in figures 1-4. During etching initial obtuse angles are split into three obtuse angles in the masking layer. The sidewalls of the first obtuse angle are defined by {311} and {n11} planes. The sidewalls of the second obtuse angle are defined by two planes of {311} family. This is similar to etching of square pattern in the masking layer with the sides along <100> crystallographic directions [25]. The sidewalls of the third obtuse angle are defined by {311} and {100} planes. For the case of n=2, the obtuse convex corner split only into two obtuse angles. The sidewalls of the first obtuse angle are defined by {311} and {211} planes. The second obtuse angle is defined by planes of {311} and {100} families.

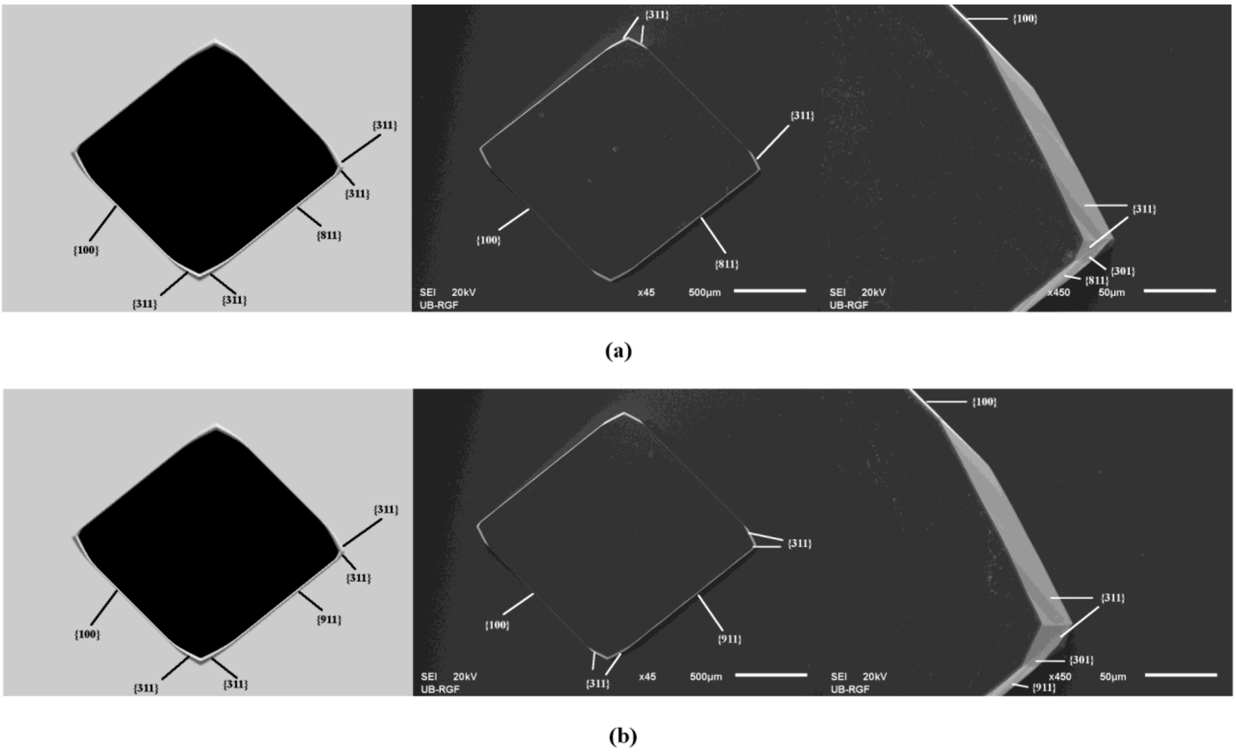


Fig. 4. Simulated etching profiles and SEM micrographs of the etched parallelogram patterns with sides along <100> and: (a) <810> directions; (b) <910> directions. Enlarged details of etched acute angles in the masking layer in both cases.

As etching continues sides planes of {311} family from the nearby convex corners become dominant and planes of {n11} (n>2) and {100} families disappear. The obtained shape is a truncated pyramid with the sidewalls defined by {311} and {301} families. The base of the pyramid in the masking layer is parallelogram with the sides along <310> crystallographic directions. In the case of n=2, the sidewalls are defined by {211}, {311} and {301} families. The base of the pyramid in the masking layer is parallelogram with sides along <310> and <210> crystallographic directions.

IV. CONCLUSION

In this paper, we studied silicon etching of parallelogram patterns in the masking layer in 25 wt % TMAH water solution at the temperature of 80 ^{0}C. The sides of parallelogram islands were designed along <n10> and <100> crystallographic directions. We analyze the etching of islands in the masking layer using both the experiments and the simulations. All the crystallographic planes that appear during etching of silicon structures are determined. A good agreement between dominant crystallographic planes through experiments and simulations is obtained. A comprehensive insight into the evolution of parallelogram patterns for different crystallographic directions can provide new ideas for the successful mask design of silicon microdevices.

ACKNOWLEDGMENT

This work has been partially funded by the Serbian Ministry of Education and Science within the framework of the project TR32008 and O171036.

REFERENCES

[1] V. Lindroos, M. Tilli, A. Lehto , T Motooka, “Wet Etching of Silicon” in *Handbook of Silicon Based MEMS Materials and Technologies*, William Andrew, Elsevier, 2010. https://www.elsevier.com/books/handbook-of-silicon-based-mems-materials-and-technologies/tilli/978-0-8155-1594-4

[2] J. Frühauf, *Shape and Functional Elements of the Bulk Silicon Microtechnique*, Springer-Verlag, Berlin, 2005. http://www.springer.com/gp/book/9783540221098

[3] M. Shikida, K. Sato, K. Tokoro, D. Uchikawa, “Differences in anisotropic etching properties of KOH and TMAH solutions”, *Sensors and Actuators A* vol. 80 no. 2, pp. 179-188, Mar. 2000. https://doi.org/10.1016/S0924-4247(99)00264-2

[4] K. Sato, M. Shikida, T. Yamashiro, K. Asaumi, Y. Iriye, M. Yamamoto, “Anisotropic etching rates of single-crystal silicon for TMAH water solution as a function of crystallographic orientation”, *Sensors and Actuators A* vol. 73 no. 1-2, pp. 131-137, Mar. 1999. https://doi.org/10.1016/S0924-4247(98)00271-4

[5] D. Resnik, D. Vrtacnik, U. Aljancic, S. Amon, “Wet etching of silicon structures bounded by (311) sidewalls”, *Microelectronic Engineering* vol. 51-52 pp. 555-566, May 2000. https://doi.org/10.1016/S0167-9317(99)00519-5

[6] D. Resnik, D. Vrtacnik, S. Amon, “Morphological study of {311} crystal planes anisotropically etched in (100) silicon: role of etchants and etching parameters”, *J. Micromech. Microeng.* vol. 10 no.3 pp. 430-439, Apr. 2000. https://doi.org/10.1088/0960-1317/10/3/319

[7] H. Yang, M. Bao, S. Shen, X. Li, D. Zhang, G. Wu, “A novel technique for measuring etch rate distribution of Si”, *Sensors and Actuators A* vol. 79 no. 2 pp.136-140, Feb. 2000. https://doi.org/10.1016/S0924-4247(99)00270-8

[8] L.M. Landsberger, S. Naseh, M. Kahrizi, M. Paranjape, “On Hillocks Generated During Anisotropic Etching of Si in TMAH”, *IEEE J. Microelectromech. Syst.* vol. 5 no. 2 pp. 106-116, Jul. 1996. DOI: 10.1109/84.506198

[9] I. Zubel, I. Barycka, K. Kotowska, M. Kramkowska, “Silicon anisotropic etching in alkaline solution IV: The effect of organic and inorganic agents on silicon anisotropic etching process”, *Sensors and Actuators A* vol. 87 no. 3 pp. 163-171, Jan. 2001. https://doi.org/10.1016/S0924-4247(00)00481-7

[10] Trieu, H.K.;Mokwa, W. A generalized model describing corner undercutting by the experimental analysis of TMAH/IPA, *J. Micromech. Microeng.*, 1998, 8, 80-83. https://doi.org/10.1088/0960-1317/8/2/009

[11] Sarro, P.M.; Brida, D.; Vlist, W.v.d.; Brida, S. Effect of surfactant on surface quality of silicon microstructures etched in saturated TMAHW solutions, *Sensors and Actuators A*, 2000, 85, 340-345. https://www.sciencedirect.com/science/article/pii/S0924424700003174

[12] M.M. Smiljanić, V. Jović, Ž. Lazić, “Maskless convex corner compensation technique on a (100) silicon substrate in a 25 wt. % TMAH water solution”, *J. Micromech. Microeng.* vol. 22 no.11 pp. 115011, Sep. 2012. https://doi.org/10.1088/0960-1317/22/11/115011

[13] M.M. Smiljanic, B. Radjenović, M. Radmilović-Radjenović , Ž. Lazić, V. Jović, “Simulation and experimental study of maskless convex corner compensation in TMAH water solution”, *J. Micromech. Microeng.* vol. 24, no. 11 pp. 115003, Oct. 2014. https://doi.org/10.1088/0960-1317/24/11/115003

[14] R. Mukhiya, A. Bagolini, B. Margesin, M. Zen, S. Kal, “<100> bar corner compensation for CMOS compatible anisotropic TMAH etching”, *J. Micromech. Microeng.* vol. 16 no. 11 pp. 2458-2462, Oct. 2006. https://doi.org/10.1088/0960-1317/16/11/029

[15] A. Bagolini, A. Faes, M. Decarli, “Influence of Etching Potential on Convex Corner Anisotropic Etching in TMAH Solution”, *IEEE J. Microelectromech. Syst.* vol. 19 no. 5 pp. 1254-1259, Oct. 2010. **DOI:** 10.1109/JMEMS.2010.2067436

[16] R. Mukhiya, A. Bagolini, T.K. Bhattacharyya, L. Lorenzelli, M. Zen, “Experimental study and analysis of corner compensation structures for CMOS compatible bulk micromachining using 25 wt% TMAH”, *Microelectronics Journal*, 2011, 42, 127-134. https://doi.org/10.1016/j.mejo.2010.08.018

[17] A. Merlos, M.C Acero, M.H. Bao, J. Bausells, J. Esteve, “A study of the undercutting characteristics in the TMAH-IPA system”, *J. Micromech. Microeng.* 1992, 2, 181-183. https://doi.org/10.1088/0960-1317/2/3/014

[18] A. Merlos, M.C Acero, M.H. Bao, J. Bausells, J. Esteve, “TMAH/IPA anisotropic etching characteristics”, *Sensors and Actuators A*, 1993, 37–38, 737-743 . https://doi.org/10.1016/0924-4247(93)80125-Z

[19] P. Pal, K. Sato, M. Shikida, M.A. Gosalvez, “Study of corner compensating structures and fabrication of various shape of MEMS structures in pure and surfactant added TMAH”, *Sensors and Actuators A* vol. 154 no.2 pp. 192-203, Sep. 2009. https://doi.org/10.1016/j.sna.2008.09.002

[20] P. Pal, K. Sato, S. Chandra, “Fabrication techniques of convex corners in a (100)-silicon wafer using bulk micromachining: a review”, *J. Micromech. Microeng.* vol. 17 no. 10 R111-R133, Sep. 2007. https://doi.org/10.1088/0960-1317/17/10/R01

[21] O. Powell, H.B. Harrison “Anisotropic etching of {100} and {110} planes in (100) silicon”, *J Micromech. Microeng.* vol. 11 no. 3 pp. 217-220, Feb. 2001. http://iopscience.iop.org/article/10.1088/0960-1317/11/3/309

[22] P.Pal, K. Sato,“A comprehensive review on convex and concave corners in silicon bulk micromachining based on anisotropic wet chemical etching”, *Micro Nano Syst. Lett.*, vol. 3 pp. 1-42, May 2015. https://mnsl-journal.springeropen.com/articles/10.1186/s40486-015-0012-4

[23] P. Pal, S. Haldar, S. S. Singh, A. Ashok, X. Yan, K. Sato, “A detailed investigation and explanation to the appearance of different undercut profiles in KOH and TMAH”, J Micromech. Microeng., vol.24 no.9 pp. 095026 (1-9), Avg 2014. http://iopscience.iop.org/article/10.1088/0960-1317/24/9/095026/meta

[24] P. Pal, K. Sato, M.A. Gosalvez, M Shikida, “Study of rounded concave and sharp edge convex corners undercutting in CMOS compatible anisotropic etchants”, J Micromech. Microeng., 2007, 17, 2299–2307. https://doi.org/10.1088/0960-1317/17/11/017

[25] M.M. Smiljanic, B. Radjenović, M. Radmilović-Radjenović, Ž. Lazić, V. Jović, “Evolution of Si crystallographic planes-etching of square and circle patterns in 25 wt % TMAH”, *Micromachines*, *10*(2), 102, Jan. 2019. https://doi.org/10.3390/mi10020102

[26] P. Pal, M. A. Gosalvez, K. Sato5, H. Hida, Y. Xing, “Anisotropic etching on Si{1 1 0}: experiment and simulation for the formation of microstructures with convex corners”, *J. Micromech. Microeng.* vol. 24, no. 12 pp. 125001, 2014. https://doi.org/10.1088/0960-1317/24/12/125001

[27] S. Osher, J.A. Sethian, “Fronts Propagating with Curvature Dependent Speed: Algorithms Based on Hamilton-Jacobi Formulations”, *J. Comp. Phys.* vol. 79 no. 1 pp. 12-49, Nov. 1988. https://doi.org/10.1016/0021-9991(88)90002-2

[28] B. Radjenović, J.K. Lee, M. Radmilović-Radjenović, “Sparse field level set method for non-convex Hamiltonians in 3D plasma etching profile simulations”, *Computer Physics Communications* vol. 174 no.2 pp. 127–132, Jan. 2006. https://doi.org/10.1016/j.cpc.2005.09.010

[29] B. Radjenović, M. Radmilović-Radjenović, M. Mitrić, “Non-convex Hamiltonians in 3D level set simulations of the wet etching of silicon”, *Appl. Phys. Lett.* Vol. 89 no. 21 pp. 213102 (1-2), Oct. 2006. https://doi.org/10.1063/1.2388860

[30] B. Radjenović, M. Radmilović-Radjenović, “3D simulations of the profile evolution during anisotropic wet etching of silicon”, *Thin Solid Films* vol. 517 no. 14 pp. 4233–4237, May 2009. https://doi.org/10.1016/j.tsf.2009.02.007

[31] B. Radjenović, M. Radmilović-Radjenović, M. Mitrić, “Level Set Approach to Anisotropic Wet Etching of Silicon”, *Sensors* vol. 10 no.5 pp. 4950-4967, May 2010. doi:10.3390/s100504950

[32] C. Montoliu, N. Ferrando, M.A. Gosalvez, J. Cerda, R.J. Colom, “Level set implementation for the simulation of anisotropic etching: application to complex MEMS micromachining”, *J. Micromech. Microeng.* vol. 23 no.7 pp. 075017, Jun. 2013. https://doi.org/10.1088/0960-1317/23/7/075017

[33] C. Montoliu, N. Ferrando, M.A. Gosalvez, J. Cerda, R.J. Colom, “Implementation and evaluation of the Level Set method - Towards efficient and accurate simulation of wet etching for microengineering applications”, *Computer Physics Communications* vol. 184 no. 10 pp. 2299–2309, Oct. 2013. https://doi.org/10.1016/j.cpc.2013.05.016

[34] http://www.paraview.org/