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SOI PIEZORESISTIVE LOW PRESSURE SENSOR FOR HIGH TEMPERATURE ENVIRONMENTS

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Abstract: *A prototype of piezoresistive low pressure sensors for high temperature environments has been fabricated on the Silicon-On-Insulator (SOI) wafers utilizing a novel maskless wet etching technique. The prototype has a structured square diaphragm with a concentric boss. The SOI pressure sensors have piezoresistors dielectrically isolated from each other and from the substrate by silicon dioxide. A high temperature transducer prototype has been made utilizing the fabricated sensor. A high temperature method for pressure measurements has been formed. The transducer prototype performance was measured at temperatures up to 300 ^{0}C. These SOI pressure sensors are intended for extreme environmental conditions and high operating temperatures that are often needed in military-grade applications and where it is necessary to perform sensitive low pressure measurements. Some examples include aerospace applications like aircraft engines, wind tunnels, various missiles, etc.*

Key words: *pressure sensor, piezoresistivity, SOI, low pressure, high temperature*

1. INTRODUCTION

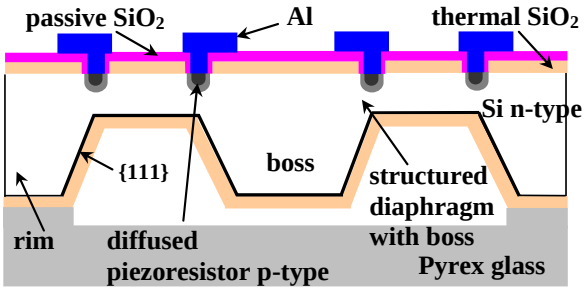
Pressure sensors intended for extreme environmental conditions and high operating temperatures are required in military-grade applications, industry applications and oil, gas and geo-thermal explorations and drilling. Very often, it is necessary to perform sensitive low pressure measurements. At the IHTM-CMTM, we have started the development of a SOI piezoresistive low pressure silicon sensor for high temperature environments SP-11.

Piezoresistors of the standard IHTM-CMTM piezoresisitive low pressure sensors comprise a diffused p-type region in an n-type silicon substrate, as shown in picture 1a). Standard low pressure sensors have a limited operation temperature range because the leakage currents of the pn junction become unaccaptable at temperatures above about 120^{o}C. Because of the limited temperature range new piezoresistive pressure sensors have been developed. Pressure sensors with an expanded operation temperature range are fabricated by standard microelectronic technology and micromachining at Silicon-On-Insulator (SOI) wafers [1-7]. The SOI pressure sensors have piezoresistors dielectrically isolated from each other and from the substrate by SiO_2, as shown in picture 1b), [1-7]. A low pressure sensor has a structured square diaphragm [8] with a concentric boss, picture 1. Both piezoresistors and structured diaphragm are fabricated on the SOI wafers utilizing a novel maskless etching technique [9, 10].

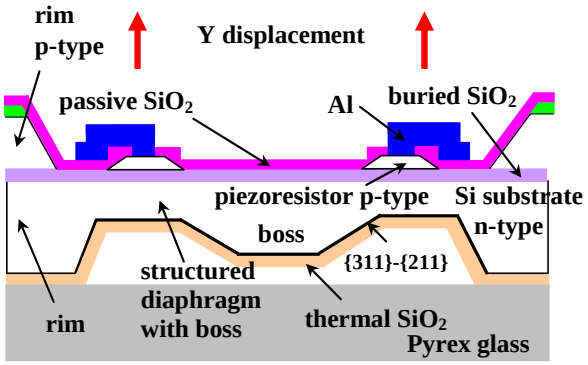
This paper gives an insight in the research and development of the SOI SP-11 pressure sensors - fabrication, preliminary measurement results and problems that should be solved in the future work.

2. FABRICATION

Fabrication of a piezoresistive low pressure sensors for high temperatures starts with the first thermal oxidation of SOI wafers. SOI wafers consist of an active silicon layer, a buried silicon dioxide and a silicon substrate. We use SOI wafers with ~6.5 μm thick active layer, ~1,5 μm thick buried silicone dioxide and ~470μm thick silicon substrate. Both the active silicon layer and the silicon substrate are (100) oriented silicon. The active layer is a heavily doped p^+-type silicon (resistivity 0.01-0.04 Ωcm). The silicon substrate is n-type silicon (resistivity 3-5 Ωcm). After the first thermal oxidation and the first photolihtographic step to define sensor diaphragm, the second thermal oxidation is performed. The second photolithographic step determines the SiO_2 masking layer of the boss. The next process is maskless wet chemical etching to obtain a structured diaphragm.



a)

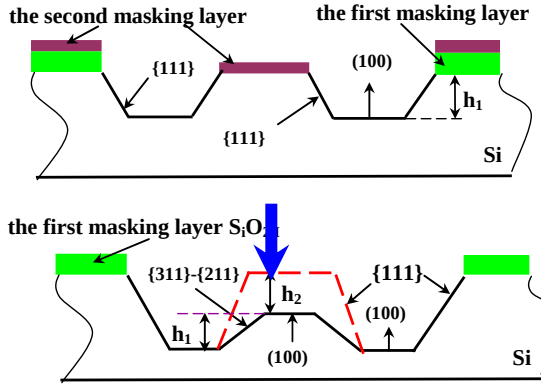


b)

Picture 1. IHTM-CMTM pressure sensors. a) Schematic cross-section of the standard IHTM-CMTM piezoresistive low pressure sensor. b) Schematic cross-section of a SOI SP-11 piezoresistive low pressure sensor for high temperature environments.

Maskless etching tecnhique is based on wet chemical etching of a (100) silicon in 25 wt % TMAH (TetraMethylAmmonium Hydroxide) water solution at temperatures of 80°C and 60°C. Maskless wet chemical etching can be divided in two steps [9, 10]. The first step is called masked etching. It is conventional wet anisotropic etching with a masking layer. The depth of masked etching is h_1, as shown in picture 2a). The second step is called maskless etching. It is in fact wet anisotropic etching after the masking layer (SiO_2 from the boss and the piezoresistors) is removed from the already structured substrate, as shown in picture 2a). The depth of maskless etching is h_2. This micromachining technique is developed to obtain a structured diaphragm with a boss as a regular truncated pyramid defined by the {311} and {211} crystallographic planes. The boss, the diaphragm and the rim of the low pressure sensor are fabricated in a SOI substrate by etching in 25 wt % TMAH water solution at a temperature of 80°C as a multilevel silicon structure, as shown in pictures 1b), 2b). The multilevel silicon structure solves the problem of the accidental electrostatic bonding of the standard IHTM-CMTM pressure boss defined by the {111} planes to the glass substrate during anodic bonding process for packaging, as shown in picture 1a). The reduced boss excludes the process of glass etching which is necessary to prevent accidental anodic bonding.

After the third thermal oxidation and the third photolithographic step for the determination of the rims in an active layer, the fourth thermal oxidation is performed. The fourth photolithographic step determines the SiO_2 masking layer for the piezoresistors. The next process is maskless wet chemical etching to obtain piezoresistors and rims in an active layer. Maskless etching of SOI active layer in 25 wt % TMAH water solution at the temperature of 60°C enables very good control of the dimensions of the piezoresistors and the rims. The fabricated piezoresistors and rims are p-type silicon mesa structures on buried silicon dioxide, as shown in picture 3. The obtained height of the piezoresistor is 0.7 μm. The rims are designed for an overload protection that we will study in our future work.



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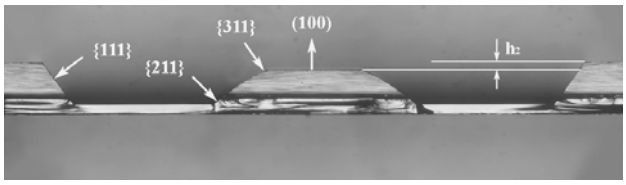
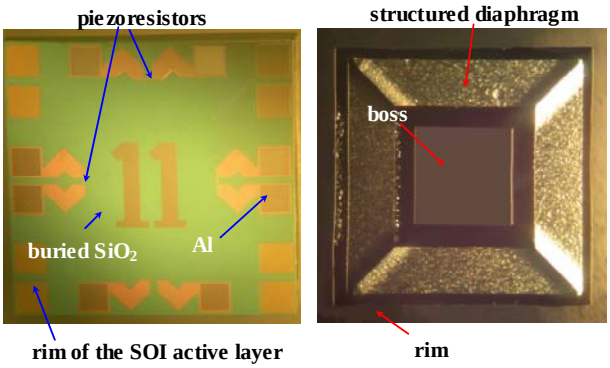


b)

Picture 2. Maskless etching. a) Schematic cross-section of maskless etching steps. The first step is masked etching. It is conventional wet anisotropic etching with a masking layer. The second step is maskless etching, which is in fact wet anisotropic etching after the masking layer (from the boss) is removed from the already structured substrate. b) Photo of the cross section of the three-level silicon structure in the <110> direction.



Picture 3. Fabricated SOI SP-11 lo pressure sensor for high temperatures. The front side of the sensors has piezoresistors and rims as mesa structures on the buried silicon dioxide. The back side of the sensors has a structured diaphragm with a concentric boss. The shape of the boss is a regular truncated pyramid defined by the {311} and {211} planes.

The next process is passive oxidation for protection of piezoresistors. In order to make openings for metalization

in passive silicon dioxide, the fifth photolithographic step is done. After the metallization of the Al layer in the sputtering system, the sixth photolithographic step is performed to obtain electrical contacts. The last process is alloying of Al contacts and silicon piezoresistors.

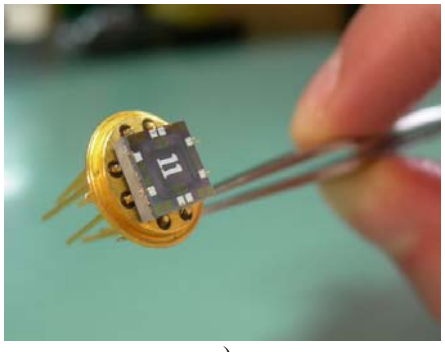
At the end of the technological cycle, the prototype chip is anodically bonded to Pyrex^R glass and glued to a TO8 housing, as shown in picture 4a). As the boss height is reduced, the problem of the accidental electrostatic bonding during anodic bonding process for packaging does not exit any more. The Al pads are bonded to TO8 pins by gold wires with a diametar of 25 μm.

3. MEASUREMENTS AND RESULTS

A housing of a high temperature pressure transducer prototype is made of steel. The SOI SP-11 chip on the TO8 housing is partially welded to the steel housing and sealed with high temperature silicon gel Loctite 5398. The TO8 pins are spot-welded with Ni wires which are coated with high temperature ceramic isolation, as shown in picture 4b). A steel pipe is mounted on the transducer steel housing, as shown in picture 4b), and sealed with copper rings. Copper rings are used because they can withstand high temperatures meauserements.

The high temperature transducer is placed inside a furnace, as shown in picture 4c). Pressure and temperature are applied at the same time. The applied temperatures were: 20, 100, 140, 180, 220, 240, 260 i 290^{o}C. The accuracy of the Tempress model 201 furnace is ±1^{o}C. We used a steel pipe for pressure connection and Keller LP pressure calibrator to apply pressure inside the furnace, as shown in picture 4c). The applied pressures were: 0, 50, 100, 150 i 200 mbar. The accuracy of the Keller LP pressure calibrator is ±1 mbar. We measured the Wheatstone bridge output without external passive temperature compensation. The applied constant current was 1 mA.

SOI SP-11 transducers show good linearity. Their nonlinearity is less than 0.6% full scale output (FSO) for all measured temperatures. Temperature depedence of the nonlinearity for a typical SOI SP-11 transducer is shown in picture 5a). Its nonlinearity is less than 0.35% for all measured temperatures. The temperature dependence of the offset and the FSO for this transducer are shown in picture 5b). The transducer prototype performance was satisfactory at temperatures as high as 300^{o}C [7]. For temperatures above 300^{o}C the SOI piezoresistive pressure sensor has lost its function.



a)

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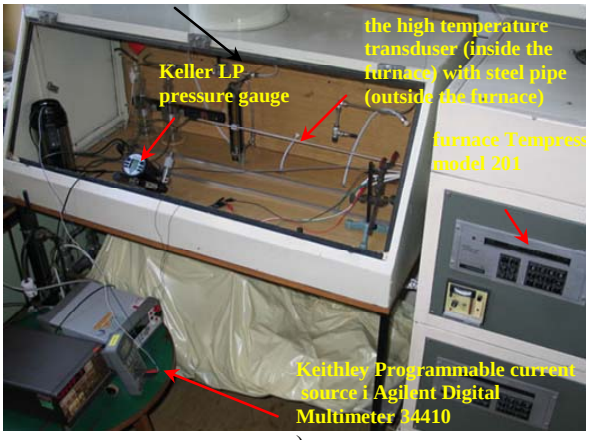
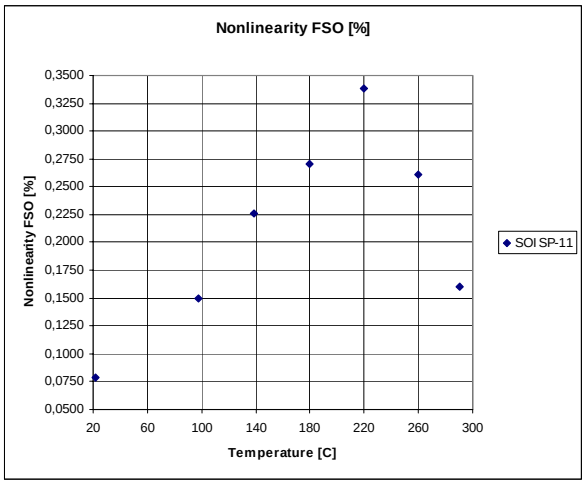


c)

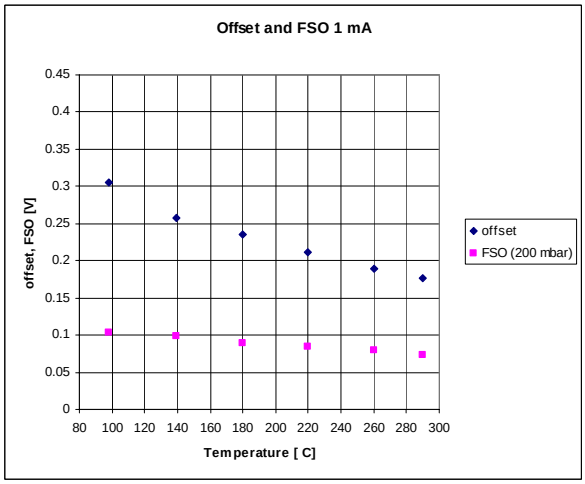
Picutre 4. a) SOI SP-11 chip glued to TO8 housing. b) The high temperature pressure transducer prototype. c) Pressure and temperature are simultaneously applied . We used Keller LP pressure calibrator to apply pressure inside the furnace Tempress model 201.

The previously designed high temperature IHTM-CMTM SOI pressure sensors [4, 5] had FSO characteristics with a distinct saddle between 140^{o}C and 200^{o}C. This effect is not noticeable in the FSO temperature dependence in picture 5b). On the other hand, the temperature infuence can be noticed in the offset and the nonlinearity temperature dependence, as shown in picture 5. A SOI SP-11 shows lower values of the offset at higher temperatures and higher nonlinearity between 140^{o}C and 220^{o}C. This effect is caused by anodic bonding process for packaging [11]. Silicon chip and Pyrex^R glass are bonded at temperature of 350^{o}C. At this temperature, a Si-Pyrex^R glass structure is stress-free because thermal expansion coefficients of both materials have very close values [11]. The thermal expansion coefficients of Si and Pyrex^R glass have different values at lower temperatures and additional thermo-mechanical stress appears. A result of our simulation of additional thermo-mechanical stress in the sensor diaphragm without applied pressure is given in picture 6a). The simulation is performed by finite element analysis software COMSOL. The used dimensions of the Si-Pyrex^R glass structure are the same as the ones of the fabricated SOI SP-11 chip. Picture 6a) shows that at the highest temperature, Si-Pyrex^R glass structure is almost stress-free and the offset has the smallest value, as shown in picture 5b).

Picture 6b) shows y-displacement of the diaphragm (see picutre 1b)) when various temperatures are applied. The shape of the curvature and temperature dependence correspond to the nonlinearity temperature dependence, as shown in picture 5a). We suppose that nonlinearity temperature dependence of SOI SP-11 is influenced by additional thermo-mechanical stresses in the Si-Pyrex^R glass structure.

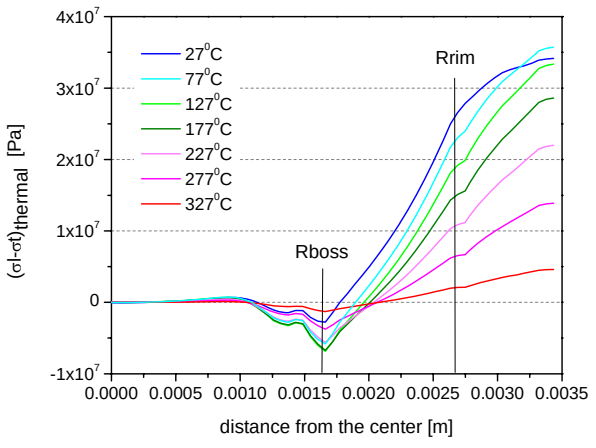


a)

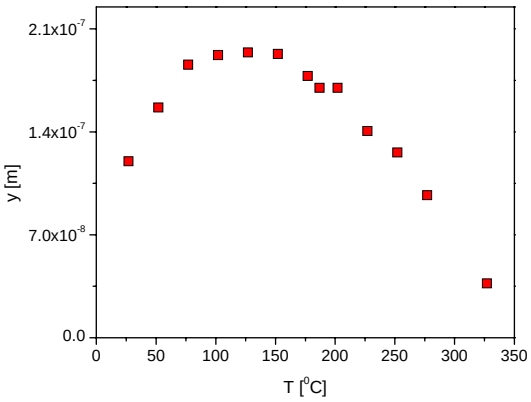


b)

Picture 5. Characteristics of a SOI SP-11 high temperature transducer. a) The temperature dependence of the nonlinearity for FSO (200 mbar). b) The temperature dependence of the offset and FSO (200 mbar).



a)



b)

Picture 6. Results of simulation when no pressure is applied. a) Adittional thermo-mechanical stress in sensor diaphragm without applied pressure. The position of the piezoresistors-near boss and near rim of the sensor. b) y-displacement of the diaphragm (Si-Pyrex^R glass structure) when various temperatures are applied.

5. CONCLUSION

A prototype of high temperature piezoresistive low pressure sensors SOI SP-11 has been fabricated by the standard microelectronic technology and maskless wet etching technique on the SOI wafers. The prototype has a structured square diaphragm with a concentric boss and its piezoresistors are dielectrically isolated by SiO_2 from each other and from the substrate. The height of the boss is reduced and the problem of the accidental electrostatic bonding during anodic bonding process for packaging is solved.

A high temperature transducer prototype has been made. The transducer prototype performance was satisfactory at temperatures as high as 300^{o}C. The offset and nonlinearity temperature dependence of SOI SP-11 are caused by additional thermo-mechanical stresses of Si-Pyrex^R glass structure. At temperatures above 300^{o}C the SOI SP-11 piezoresistive low pressure sensor ceases to function.

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