Master's Thesis

Double-Floating-Gate van der Waals Transistor for High-Precision Synaptic Operations

Hoyeon Cho

Department of Materials Science and Engineering

Ulsan National Institute of Science and Technology

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Approved by

Advisor

Joonki Suh

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This certifies that the thesis/dissertation of Hoyeon Cho is approved.

12.13.2022 of submission

Signature

Advisor: Joonki Suh

Signature

Hongsik Jeong

Signature

Tae-Sik Yoon

Abstract

Two-dimensional materials and their heterostructures have thus far been identified as leading candidates for nanoelectronics owing to the near-atom thickness, superior electrostatic control, and adjustable device architecture. These characteristics are indeed advantageous for neuro-inspired computing hardware where the precise programming is strongly required. However, its successful demonstration fully utilizing all of the given benefits remains to be further developed. Herein, we present van der Waals (vdW) integrated synaptic transistors with multi-stacked floating gates, which are reconfigured upon surface oxidation. When compared with a conventional device structure with a single floating gate, our double-floating-gate (DFG) device exhibits better non-volatile memory performance, including a large memory window (100 V), high on–off current ratio (10^7), relatively long retention time (5000 s), and satisfactory cyclic endurance (500 cycles), all of which can be attributed to its increased charge-storage capacity and spatial redistribution. This facilitates highly effective modulation of trapped charge density with a large dynamic range. Consequently, the DFG transistor exhibits an improved weight update profile in long-term potentiation/depression synaptic behavior for nearly ideal classification accuracies of up to 96.12% (MNIST) and 81.68% (Fashion-MNIST). Our work adds a powerful option to vdW-bonded device structures for highly efficient neuromorphic computing.

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List of Abbreviations

2D	Two-dimensional
AFM	Atomic force microscopy
ANNs	Artificial neural networks
BF	Bright-field
c-AFM	Conductive atomic force microscopy
CMOS	Complementary metal-oxide-semiconductor
DFG	Double-floating-gate
EDS	Energy dispersive X-ray spectroscopy
EFM	Electrostatic force microscope
EPSC	Excitatory postsynaptic current
FIB	Focused ion beam
F-N	Fowler-Nordheim
HAADF	High-angle annular dark-field
HRS	High resistance state
LRS	Low resistance state
LTD	Long-term depression
LTP	Long-term potentiation
ML	Machine learning
MNIST	Modified National Institute of Standards and Technology
NPLC	Number of power line cycle
NVM	Non-volatile memory
PDMS	Polydimethylsiloxane
PSC	Postsynaptic current
SFG	Single-floating-gate
SMU	Source measure unit
SRDP	Spike-rate-dependent plasticity

STDP	Spike-timing-dependent plasticity
STEM	Scanning transmission electron microscopy
vdW	van der Waals

Chapter 1. Introduction

1.1 Neuromorphic architecture and next-generation electronics

In the modern information age, data-intensive tasks such as image classification and segmentation are of considerable technological significance and have become increasingly complicated.[1] With recent advancements in artificial neural networks (ANNs) and machine learning (ML), development of specialized hardware to efficiently process complex and unstructured data is thus considered an utmost urgency and necessity.[2,3] The currently available von Neumann architecture causes enormous energy consumption in ANNs and ML algorithms operating on digital complementary metal-oxide-semiconductor (CMOS) circuitry.[4] Conversely, the typical human brain, which has only ~100 billion neurons interconnected through several quadrillion synapses, expends only 20 W of power in small volumes for logic-in-memory operations.[5,6] Therefore, as an alternative to the conventional CMOS technology, brain-inspired neuromorphic architecture and related devices are being actively investigated as next-generation electronics for massively parallel memory processing.[7-10] As shown in Figure 1.1, the logarithmic graph illustrates the complexity relationship between the architecture and environment with reference to von Neumann and Neuromorphic architecture.[11]

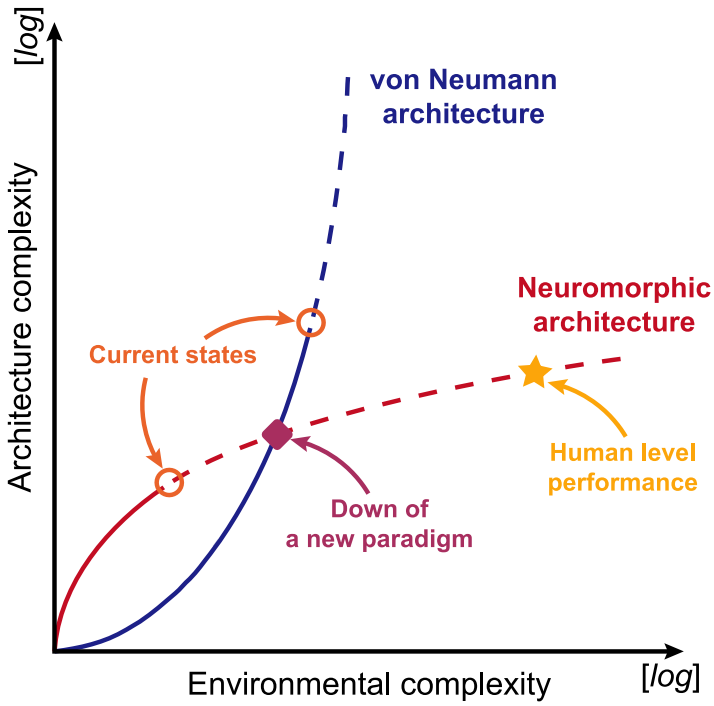

Figure 1.1. Relationship of architecture complexity and environmental complexity. The von Neumann and the Neuromorphic architecture as tracked in blue and red line, respectively.

To improve the realization of ANNs and ML algorithms, accurately mimicking synaptic behavior is still highly desirable, including the high-precision and high-fidelity synaptic weight update process between neighboring neurons.[12] To fulfill these prerequisites, three-terminal synaptic transistors have been developed owing to their excellent control over synaptic weights (channel conductance) via independent presynaptic input (gating) with the decoupled write and read operations.[13,14] However, the non-ideal characteristic issues, including abrupt weight change and limited dynamic range, are still the main obstacles to obtaining high accuracy with ANN simulation in learning tasks as shown in Figure 1.2.[15] This is due to the structural limitations of three-terminal transistors, which make it difficult to achieve linear output changes with identical input signals.[16] Typically, linearity and symmetry of weight updates, which are realized via a highly precise programming process, offer training accuracy, network capacity, and discrimination among input signals in neuromorphic computing systems.[17]

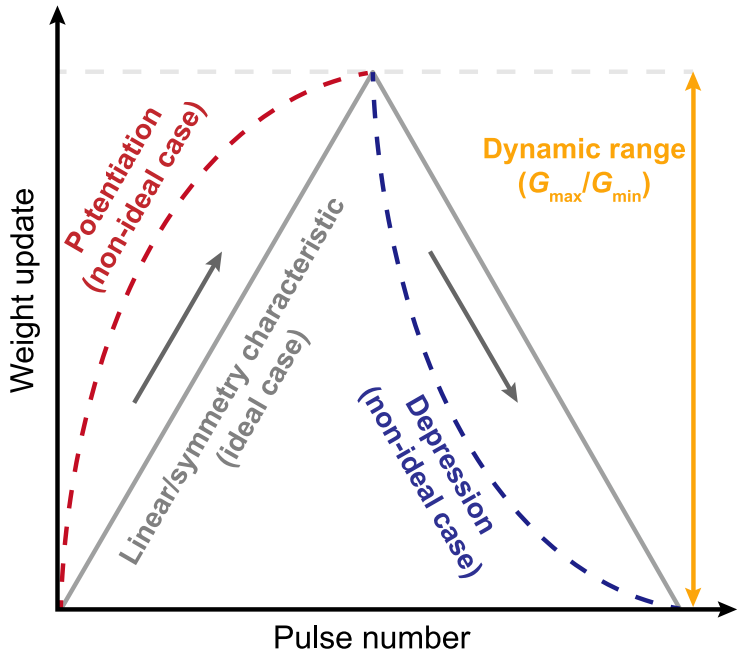

Figure 1.2. Weight update characteristics of artificial synapse with (non-)ideal case.

1.2 Two dimensional materials for artificial synapse

Two-dimensional (2D) materials provide new opportunities for post-CMOS technology owing to their extraordinary intrinsic properties, including the atomically thin structure and lack of surface dangling bonds, which ensure active external manipulations such as gating and minimized interface trapped charges.[18-25] Consequently, heterostructures composed of 2D materials have been widely proposed as promising candidates for artificial synapses. Device performance in these structures has advanced owing to easy electronic tunability and a variety of van der Waals (vdW) device architectures.[26-32] Herein, we present a vdW heterostructure-based double-floating-gate (DFG) synaptic transistor where the bi-layer unit of tunnel barrier and floating gate are vertically stacked as a charge storage media (Figure 1.3). It has the advantages of a large memory window, high on–off current ratio, long retention time, and good cyclic endurance performance in non-volatile memory (NVM) characteristics. We propose the mechanism of charge (de-)trapping in the DFG device with energy-band diagrams, which confirm highly effective modulation and reliable retention of trapped charge density due to charge redistribution. Based on our results, DFG transistors are also able to demonstrate a relatively high dynamic range and synaptic plasticity behavior of long-term potentiation/depression that is more linear and symmetrical than single-floating-gate (SFG) devices. Through an ANN simulation using the synaptic DFG transistor, the pattern recognition in Modified National Institute of Standards and Technology (MNIST) and Fashion-MNIST exhibited recognition accuracies of 96.12% (+4.13%, in comparison to SFG) and 81.68% (+6.39 %, in comparison to SFG), respectively.

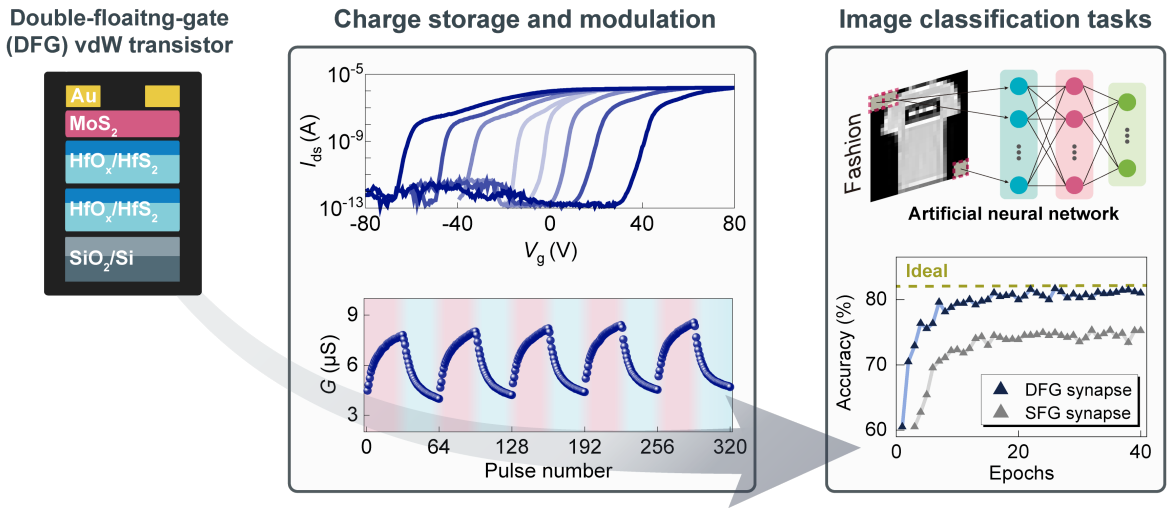

Figure 1.3 DFG device with 2D vdW heterostructures. Charge storage and modulation properties and image classification performance of DFG transistor.

Chapter 2. Double-Floating-Gate (DFG) Transistor Based on van der Waals (vdW) Heterostructures

2.1 HfS_2 oxidation

Figure 2 collectively illustrates the proposed device configuration of three-terminal vdW synaptic transistors with the floating gate storage node. The key ingredient of floating gate memory is charge-storing element, which corresponds to HfO_x/HfS_2 stacks in our device. HfS_2 is chosen as an efficient and robust floating gate where electron charges are trapped. Thanks to its sensitivity to the ambient environment,[33,34] albeit often regarded as problematic, HfO_x can be formed controllably and homogeneously by an O_2 plasma treatment on top surface of HfS_2, designed for thin tunneling oxide.[26] The surface of O_2-plasma-treated flake exhibits a change of phase contrast in electrostatic force microscope (EFM) images, revealing that the whole HfS_2 surface is uniformly oxidized, as shown in Figure 2.1. Each unit device consists of transistor channel (few-layer MoS_2), floating gate storage stacks (HfO_x/HfS_2, further details to be discussed below), gate dielectric (SiO_2), and control gate (p^{++}-Si) as shown in Figure 2.2a and 2.2b. They were heterogeneously and vertically assembled by top-down manipulation, *i.e.*, initiated from mechanical isolation from lab-grown bulk crystals and completed upon transfer to thermally oxidized Si substrate (Figure 2.3).

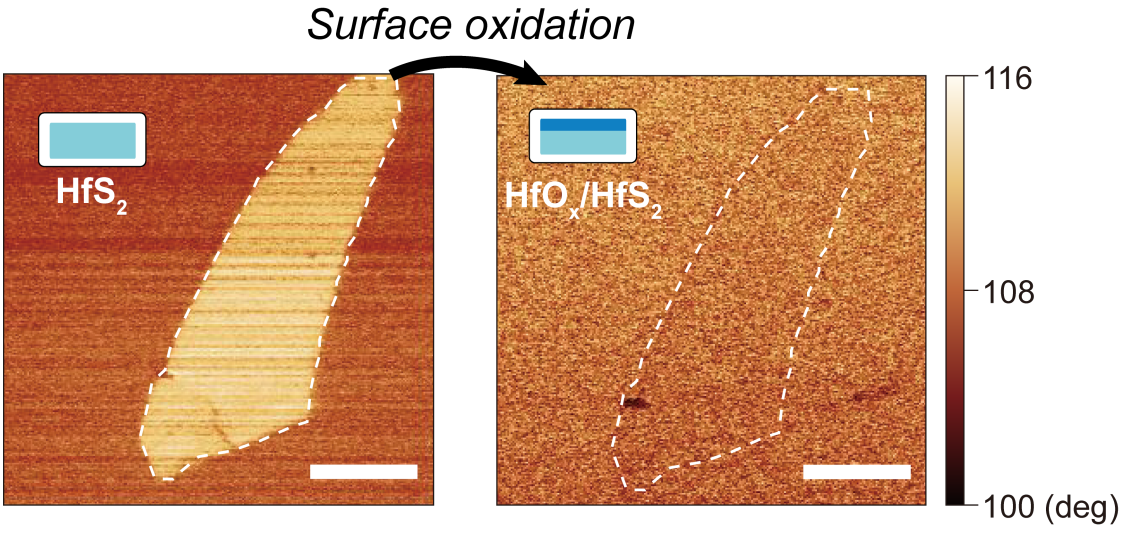

Figure 2.1. EFM phase images of HfS_2 flake on SiO_2/Si substrate before and after surface oxidation. Scale bar, 5 μm.

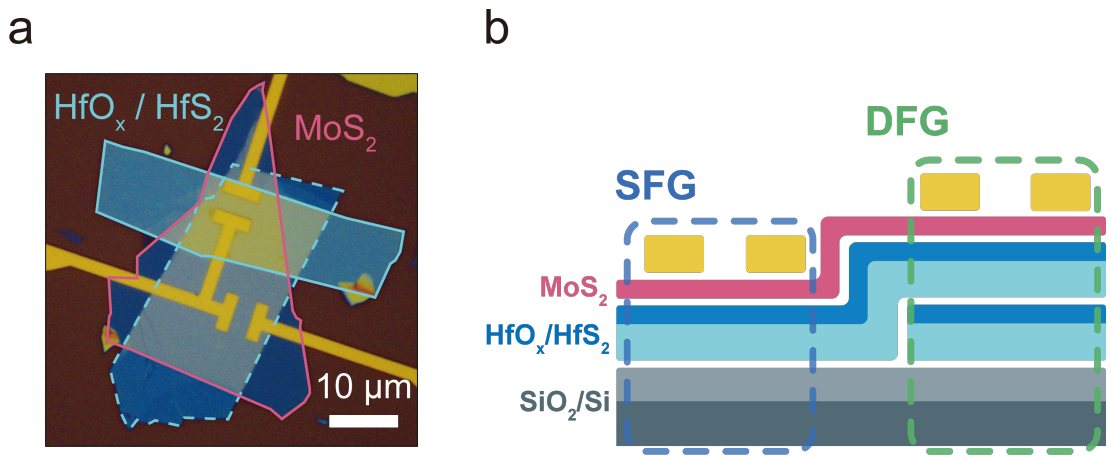

Figure 2.2. vdW heterostructure-based synaptic transistor with double floating gates. (a) Optical microscope image of the as-assembled floating gate devices. Few-layer MoS_2 flake (red solid line) is the shared channel layer for both SFG and DFG devices. HfO_x/HfS_2 stacks (blue solid and dotted lines) are employed as floating gate storage node, defining DFG (top) and SFG (bottom) memory, respectively. (b) A schematic model of the vdW transistors (side view of (a)).

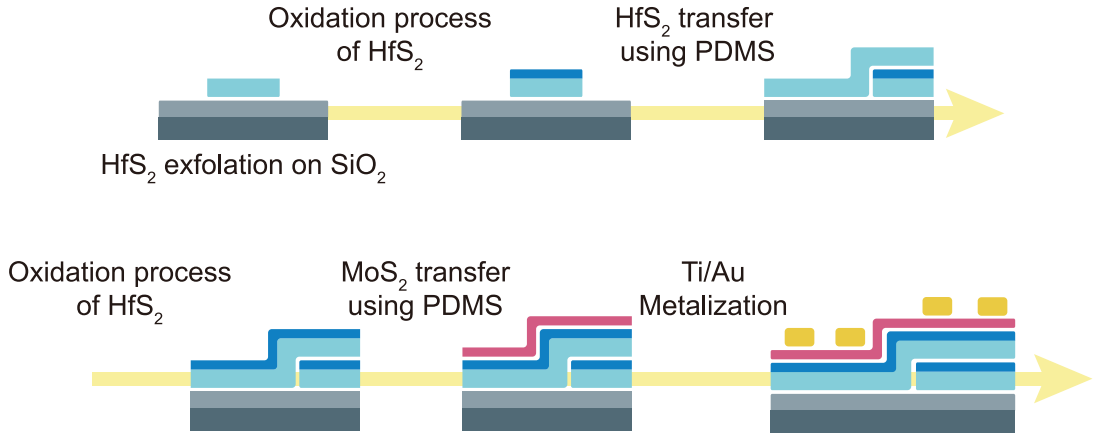

Figure 2.3. Schematic illustration of the fabrication process of the SFG and DFG devices.

2.2 DFG transistor built from two-dimensional(2D) materials

After being simultaneously processed and stacked, two devices were then defined by e-beam lithography and following Ti/Au (10/60 nm) metallization steps. We managed to have two floating gate transistors that share all identical device components including the channel of uniform thickness/length/width (5.2 nm/3 μm/6 μm) except one additional HfO_x/HfS_2 stack exclusively added to one of them (top in Figure 2.2a) which has double floating gates while the other one (bottom in Figure 2.2a) remains with single floating gate. These experimental approaches enabled us to comparatively investigate their electrical and synaptic characteristics depending on whether they have a single or multiple (double in the case of our experiments) charge-storage stack(s).

2.3 Cross-sectional scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDS) analysis

The as-fabricated device was examined via cross-sectional scanning transmission electron microscopy (STEM), which revealed that HfO_x was grown on HfS_2 to a thickness of ~6 nm without any visible contamination and voids (Figure 2.4a). The MoS_2 and HfS_2 layers had interlayer distances of 0.65 nm and 0.59 nm, respectively, corresponding to their (001) plane. The cross-sectional STEM images together with bright-field (BF) and high-angle annular dark-field (HAADF) images at higher magnification also confirmed a smooth and ultraclean interface between HfS_2 and HfO_x (Figure 2.5). Additionally, corresponding energy-dispersive X-ray spectroscopy (EDS) element mapping was performed to investigate the elemental compositions of the 2D vdW heterostructure (Figure 2.4b). The HfO_x layers were completely converted from HfS_2 as required, as shown by the EDS maps, which displayed Hf and O elements with no S signal.

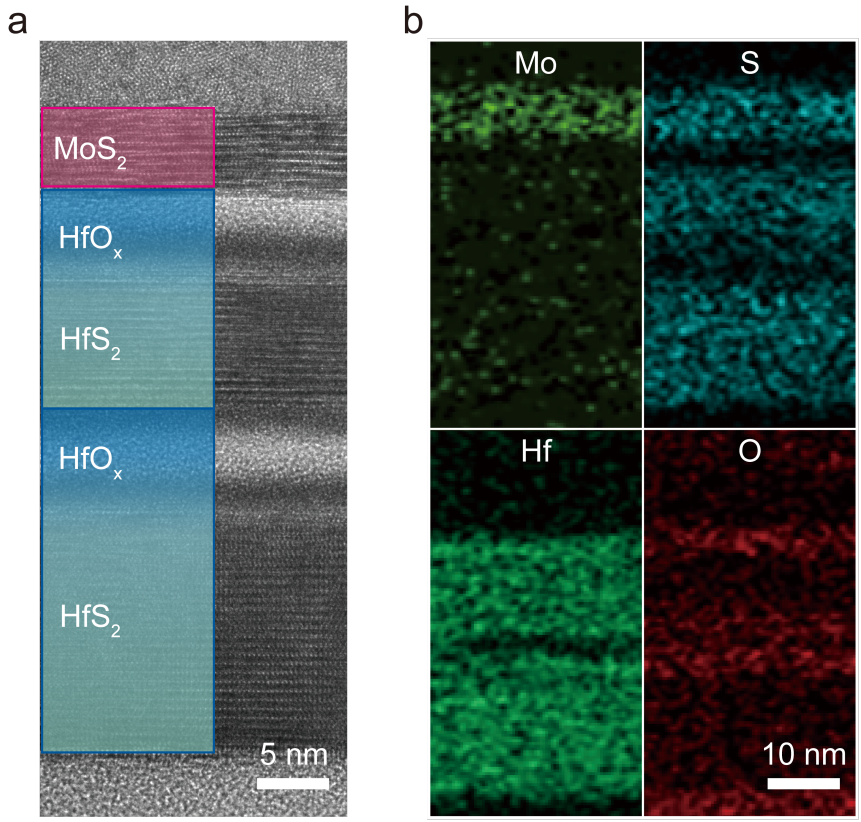

Figure 2.4. (a) Cross-sectional STEM image of the MoS_2-based DFG device assembled with two HfO_x/HfS_2 flakes. (b) Corresponding EDS elemental mapping confirming chemical contents of each layer. Notably, sulfur is completely replaced by oxygen in HfO_x layer upon oxidation treatment.

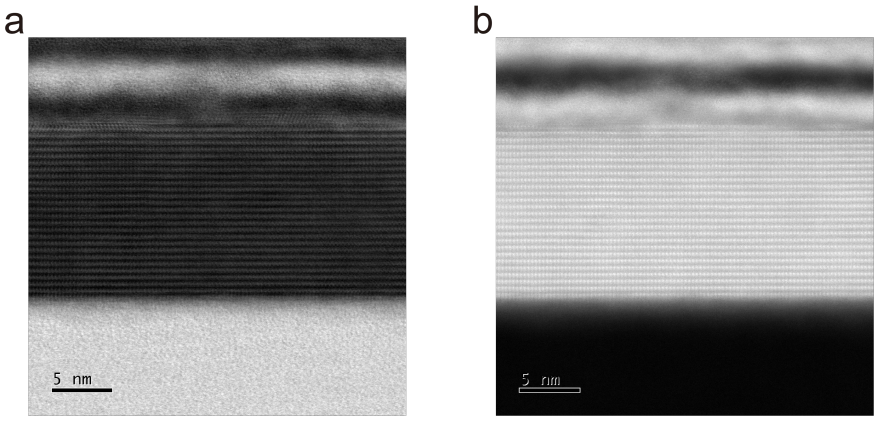

Figure 2.5. The cross-sectional (a) BF- and (b) HAADF-STEM images.

2.4 Experimental method

2.4.1 MoS_2 and HfS_2 crystal growth

The MoS_2 and HfS_2 single crystals were grown by a chemical vapor transport (CVT) method with iodine (I_2) as a transporting agent. Stoichiometric ratio of high-purity (99.99%) Mo, Hf, S elemental powders were put into a quartz ampoule, respectively, evacuated to a low-pressure level (< 10^{-6} Torr) by a diffusion pump, and then securely sealed using hydrogen oxide flame. For MoS_2 crystal, the growth was completed under a temperature gradient from 1050 ℃ (reaction zone) to 935 ℃ (growth zone) for 500 hours, similarly done in our previous reports.[35,36] HfS_2 crystals were prepared with a slightly modified condition: 800 ℃ (reaction zone) and 650 ℃ (growth zone) for 350 hours.

2.4.2 Device fabrication

For the vdW stacked hetero-structures, HfS_2 flakes were mechanically exfoliated from the bulk crystal using the scotch-tape method and transferred onto the 300 nm-thick SiO_2 oxide layer on heavily boron-doped Si substrate using polydimethylsiloxane (PDMS) stamping method to avoid contamination. The O_2 plasma treatment process was carried out on the HfS_2 flakes by the plasma system (FemtoScience, CUTE). The oxidation process conditions are as follows: power frequency (10 W, 50 kHz), base pressure (50 mTorr), O_2 flow rate (~10 sccm) and oxidation time (60 s). Next, the channel MoS_2 flake was transferred onto the stacked structure ($HfO_x/HfS_2/HfO_x/HfS_2$) using the PDMS stamping. The source and drain electrodes were patterned by e-beam lithography, followed by 10 nm-thick Ti and 50 nm-thick Au deposition processes via an e-beam evaporator under about 10^{-7} Torr.

2.4.3 STEM and atomic force microscopy (AFM) characterization

A specimen for cross-sectional image of DFG device was first prepared by a dual beam focused ion beam system (FEI, Helios NanoLab 450HP). After a carbon protection layer was deposited on top of the DFG device, the surrounding channel region was milled. Cross-sectional STEM images and EDS elemental mapping of the corresponding device were then acquired using a JEOL JEM-ARM300F working at 200 kV. EFM and c-AFM were performed using Oxford Instruments MFP-3D AFM with conductive tips (Adama, AD-40-AS).

Chapter 3. Non-Volatile Memory (NVM) Characteristics

3.1 Charge storage capability

To verify and understand the charge-storage capability of the vdW floating gates, the fundamental electrical transport properties of the fabricated devices were investigated. Figure 3.1 shows the corresponding transfer curves of the SFG and DFG transistors, which were controlled by various back-gate voltage (V_g) sweeping ranges while being held under a drain-source bias (V_{ds}) at +0.1 V. The observed clockwise hysteresis, which indicates the charge tr apping mechanism, created a memory window (ΔV_{th}), and an apparent ΔV_{th} between the devices was observed as the $V_{g,max}$ was gradually expanded. Notably, the ΔV_{th} and on–off current ratio of the DFG device reached >100 V and ~10^7, respectively, demonstrating its excellent NVM performance. The electrons trapped in the HfS_2 floating gate offset the electric field strength of the V_g. Its enhanced memory window (+37.3%, in comparison to SFG at 80 $V_{g,max}$) indicates that the total number of trapped charges was greater in the DFG than in the SFG at the given $V_{g,max}$, as the DFG-based geometry could provide more density of states for charge carriers. The extracted ΔV_{th} as a function of $V_{g,max}$ is provided in Figure 3.2, and this trend was monitored and confirmed using additional sets of SFG and DFG transistors (Figure 3.3). The transfer characteristics of MoS_2 field-effect transistors (FETs) without floating gates that were fabricated on SiO_2 or HfO_x (entirely oxidized HfS_2 flake) are also presented in Figure 3.4 for a better understanding of the crucial function of the floating gate and the origin of the ΔV_{th} shift. These results indicate that the trap sites at the MoS_2/SiO_2 and MoS_2/HfO_x interfaces are the cause of the relatively small ΔV_{th} shift.[37] Consequently, the DFG transistor exhibited better on–off current performance between the low resistance state (LRS) and high resistance state (HRS) during the electrical programming/erasing process after applying a V_g of +60 V or −60 V for a 2-s pulse duration, reading at V_{ds} = +0.1 V (Figure 3.5). Particularly, the DFG transistor reached an on–off current ratio of ~10^7 at V_{ds} = ±0.1 V, whereas the SFG transistor exhibited unstable HRS operations when the V_{ds} was changed from negative to positive values.

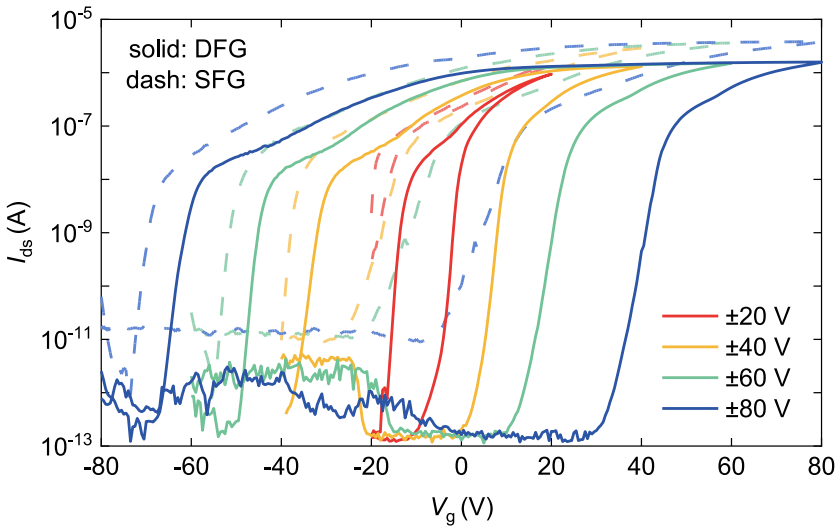

Figure 3.1. The I_{ds}–V_g transfer characteristics acquired from SFG and DFG memories under various $V_{g,max}$.

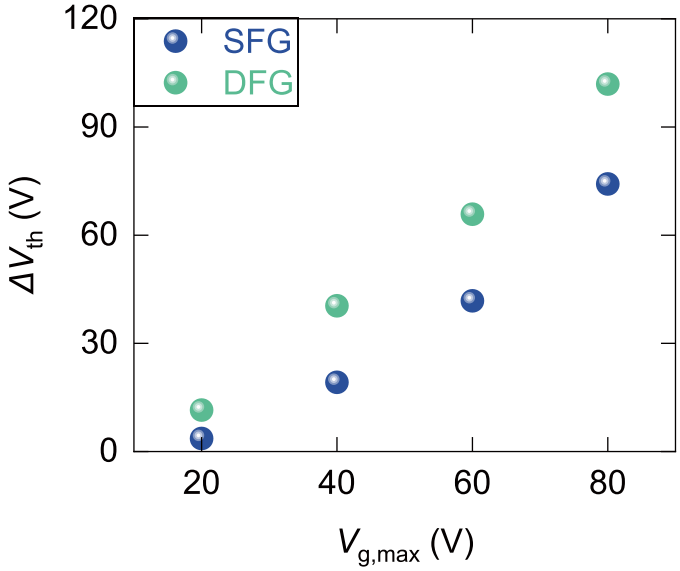

Figure 3.2 . Variation of extracted ΔV_{th} from the transfer characteristics depending on $V_{g,max}$.

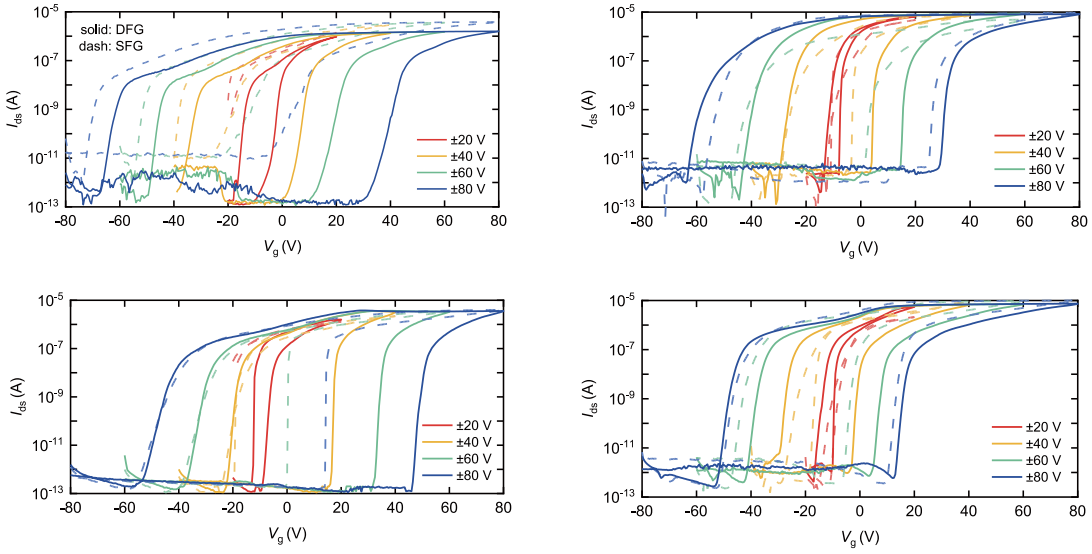

Figure 3.3. The I_{ds}−V_g transfer characteristics of additional SFG and DFG devices under various $V_{g,max}$.

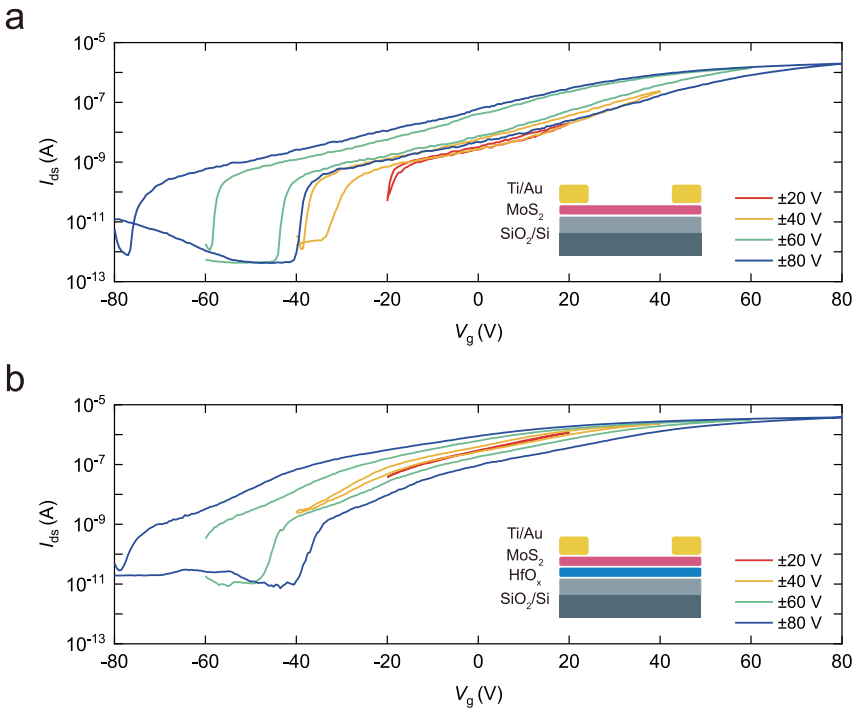

Figure 3.4. The transfer characteristics of MoS_2 FETs fabricated on SiO_2 or HfO_x insulator.

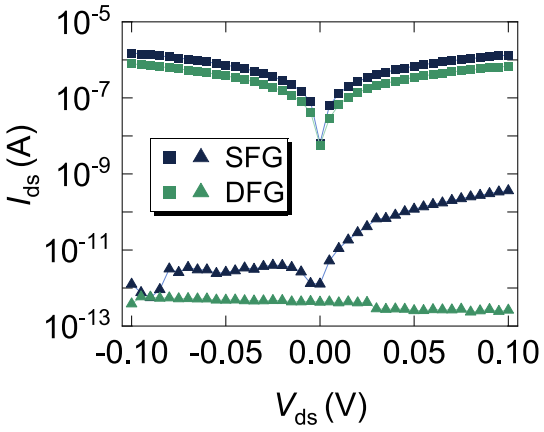

Figure 3.5. (a) Output characteristics at LRS (square) and HRS (triangle) of SFG and DFG devices after applying a pulse of V_g = −60 V or +60 V for 2 s.

3.2 NVM performance

To evaluate their NVM performance, we measured the charge retention properties and cyclic endurance of LRS and HRS at V_{ds} = +0.1 V after programming (V_g = +80 V) or erasing (V_g = −80 V) for a 2-s pulse duration (Figures 3.6a and b). The DFG transistor exhibited greater stability and reliability than the SFG transistor in both the retention performance (over 5000 s [time interval = 100 s]) and the cyclic endurance performance (up to 500 cycles). Notably, the SFG device exhibited charge loss after an elapsed time of 1500 s during the retention characteristic test. The low charge-storage capacity of the SFG device enabled trapping of electrons into spatially and energetically shallow traps, whereas the DFG device enabled trapping of electrons into trap sites spatially far from the channel owing to its high charge-storage capacity, which will be discussed in detail in the next section. In addition to such secure charge storage, the multilevel capability of eight discrete conductance states was demonstrated for 30 s in the DFG transistor (Figure 3.7). This indicates that the density of trapped electrons in the isolated DFG could be effectively and stably modulated under an identical pulse train, which is promising for concise neuromorphic systems. To enable multilevel storage, the current along the device channel was read at V_{ds} = +0.1 V after applying programming pulses with amplitudes varying from V_g = 45 to V_g = 75 V (1-s pulse duration). Thus, the DFG memory device exhibited better NVM characteristics as well as increased charge-storage capacity, both of which can be attributed to the additional pair of the floating gate and tunneling oxide layer.

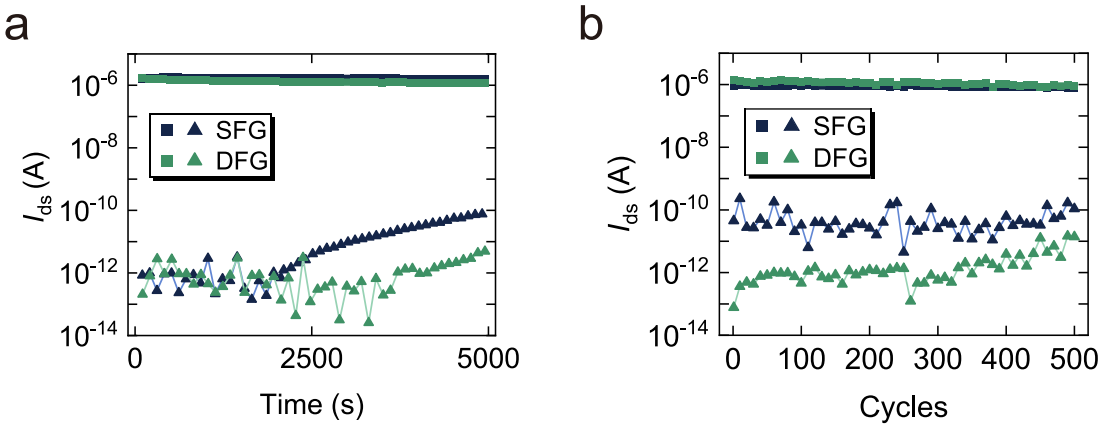

Figure 3.6. (a) Retention behavior of storage charges at LRS (square) and HRS (triangle) of SFG and DFG devices up to ~5 × 10^3 s. (b) Cyclic endurance characteristics during 500 cycles of switching operation. LRS (square) and HRS (triangle) were achieved by V_g = −80 V and +80 V with a pulse duration of 2 s.

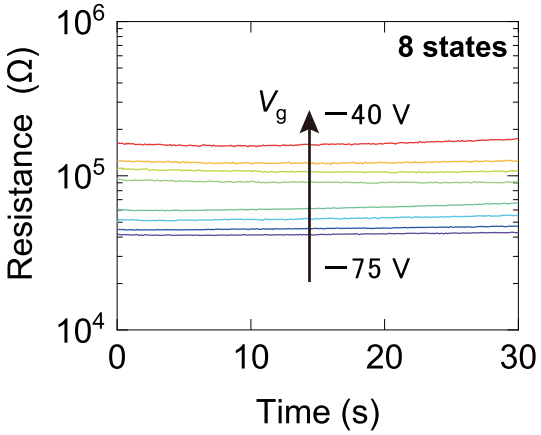

Figure 3.7. Multi-level storage capability of DFG memory for 8 distinct states. All the data were collected using a reading voltage, V_{ds} = +0.1 V.

3.3 NVM characteristic measurement

The NVM characteristic measurement of the devices were obtained by a semiconductor parameter analyzer (Keithley, 4200A-SCS). All the measurements were performed at room temperature and under vacuum condition (< 10^{-4} Torr) using the probe station (Lakeshore, CRX-4K).

Chapter 4. Proposed Operation Principle of DFG Transistor

4.1 Fowler-Nordheim tunneling behavior

Figure 4.1 shows the measured tunneling current and $ln(I/V^2)$ versus $1/V$ curve for linear fitting by the Fowler–Nordheim (F–N) tunneling model using conductive atomic force microscopy (c-AFM).[38] The well-fitted curve revealed that the tunneling current through the HfO_x tunneling oxide layer at a high bias can be explained using the F–N tunneling model.

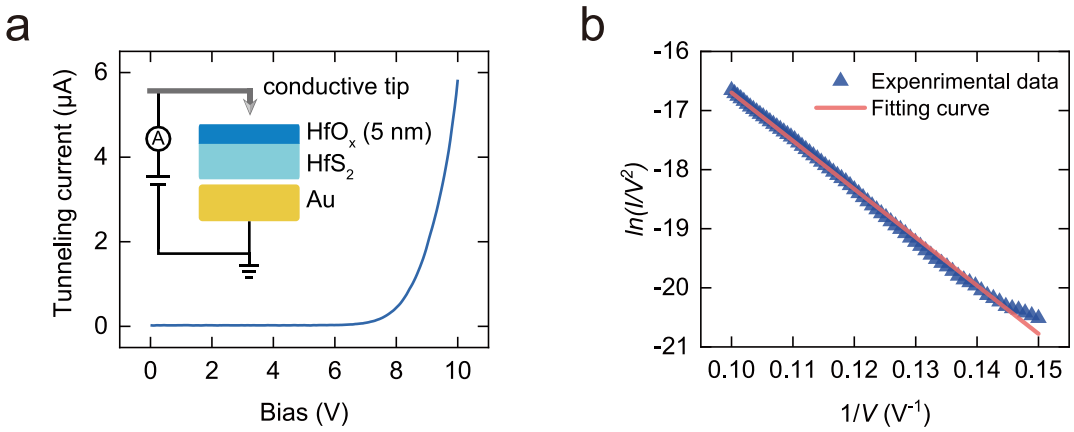

Figure 4.1. (a) Tunneling current measurement using C-AFM in 5nm-thick HfO_x/HfS_2 flake (b) $ln(I/V^2)$ versus $1/V$ plot for linear fitting of F-N tunneling model.

4.2 Energy band diagram

To better understand the effect of DFG and its improved memory performance, the corresponding energy-band diagrams and relevant tunneling behavior were considered (Figure 4.2). The electron affinity (χ) and energy band gap (E_g) under the flat-band condition were ~4.2 and ~1.2 eV for the multilayered MoS_2, 4.8 and 2.0 eV for the mutilayered HfS_2, 2.4 and 5.6 eV for the HfO_x, and 0.6 and 8.9 eV for the SiO_2 (Figure 4.2a).[26,39] Therefore, the barrier heights for electrons through the HfO_x (Φ_1, Φ_2) were estimated to be ~2.4 and ~1.9 eV, respectively. For the SFG device, electrons could tunnel into the floating gate through the HfO_x layer when the high positive back-gate voltage ($V_g > 0$ V) was applied. Consequently, the high electron density (within the HfS_2 floating gate) and corresponding large electric field were constructed between the HfO_x and MoS_2. Subsequently, when removing gate voltage, high leakage current (charge loss) was induced via F–N tunneling (Figure 4.2b). Based on the observed

outstanding memory performances, including a large window of ΔV_{th} and reliable charge retention (Figure 3.2 and 3.6b), the DFG device is expected to effectively and securely trap more charges. Similar to SFG devices, once the high positive gate voltage is applied to the gate, electrons can tunnel into the DFG through one or two HfO_x layers (Figure 4.2c). After removing the gate voltage, trapped electrons in the HfS_2 that are adjacent to the SiO_2 can be transferred to the other HfS_2 via F–N tunneling to balance the potential difference between the two separate floating gates. Compared with a single thicker tunneling barrier, such two independent thin tunneling barriers can provide a stronger electric field at a lower bias for efficient F–N tunneling. The low charge loss in the DFG device can be attributed to charge redistribution between two floating gates, which can prevent high leakage current via F–N tunneling from HfS_2 to MoS_2. This trend is further supported by synaptic operations in DFG devices, which will be later explained in detail.

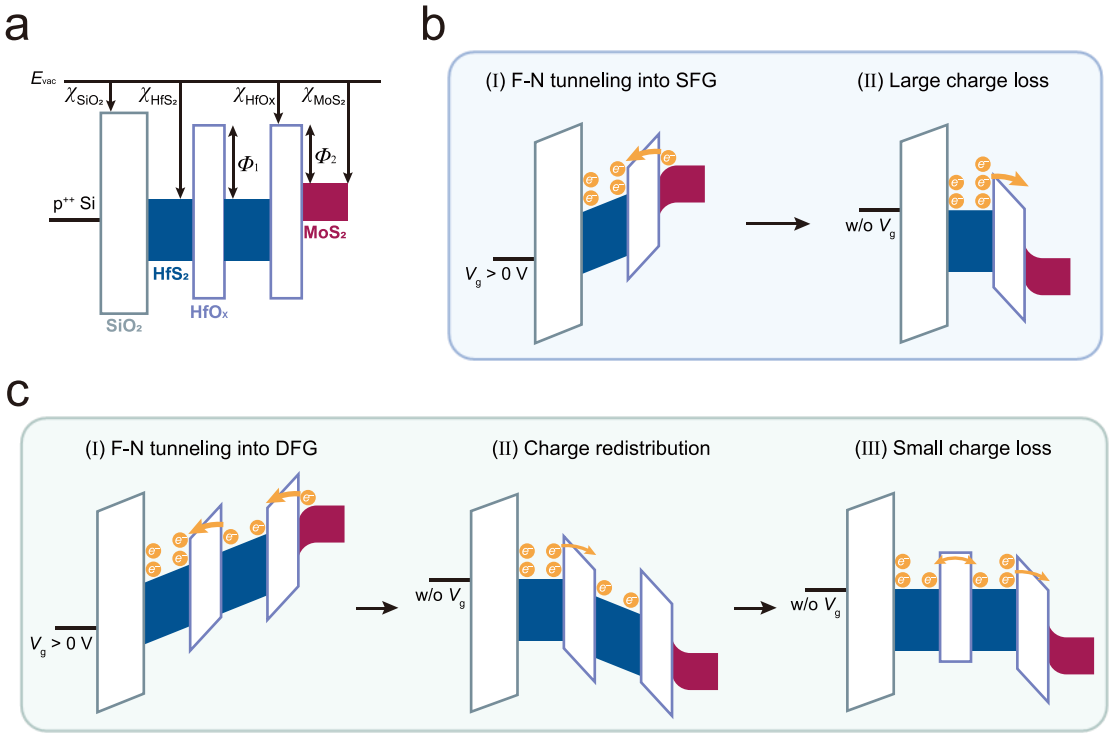

Figure 4.2. Energy band diagrams and F-N tunneling behavior schematic. (a) Energy band diagram in flat band state of the DFG device. E_{vac}, χ, and Φ are vacuum level, electron affinity, and barrier height, respectively. (b) Energy band diagrams of electron transfer state of SFG device (under (I) F-N tunneling into single floating gate and (II) high charge loss) (c) Energy band diagrams of electron transfer state of DFG device (under (I) F-N tunneling into double floating gates, (II) charge redistribution, and (III) low charge loss).

Chapter 5. Emulating Artificial Synaptic Functions

5.1 Principles of synaptic transmission

Inspired by the multilevel storage characteristics realized in the DFG transistor, we further investigated the electronic synaptic functions emulating biological synapses connected to neuronal junctions using charge (de-)trapping events (Figure 5.1). The enlarged region shows synaptic transmission between the axon terminal of the presynaptic neuron and dendrite of the postsynaptic neuron. When a nerve impulse (also known as action potential or spike) reaches the presynaptic neuron, chemical neurotransmitters in the synaptic vesicle are released to the postsynaptic receptors through the synaptic cleft.[40,41] Subsequently, the induced electrical signal and event, including postsynaptic membrane potential and postsynaptic action potential, are generated. Generally, the synaptic weight (connection strength between neighboring neurons) is determined by the resting postsynaptic membrane potential and corresponding postsynaptic current (PSC) level.[42]

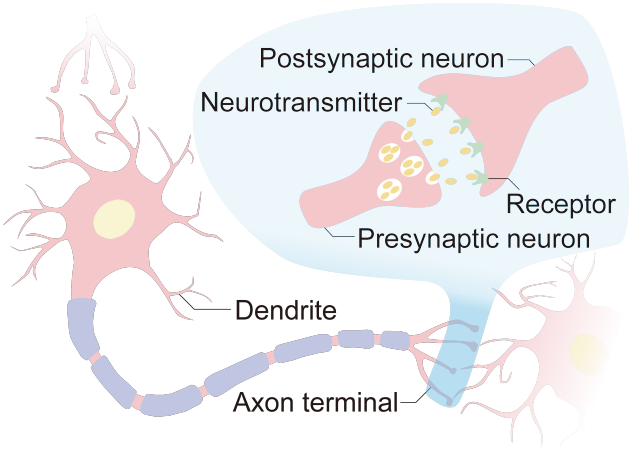

Figure 5.1. Schematic illustration of a biological synapse between the pre- and postsynaptic neurons.

5.2 Artificial synaptic properties

By modulating the amplitude and duration conditions of the negative presynaptic V_g pulse, the DFG transistor can effectively fine-tune the synaptic weight, as shown in the excitatory PSC (EPSC) behavior in Figures 5.2a and b. As different spike amplitudes were applied from $V_g = -20$ to -30 V with the fixed spike duration (100 ms), the EPSC values continuously increased owing to more electrons de-trapped in the floating gates. Consequently, the EPSC values under longer spike duration conditions with the

fixed spike amplitude (V_g = −25 V) increased. These results are conceptually similar to the case of a biological synapse, where greater presynaptic spikes with higher amplitude and longer duration increase the EPSC value.[42,43] Figure 5.3 further reflects the relationship between synaptic strength and presynaptic spike frequencies from 0.5 to 5 Hz under six spike-fixed amplitudes (−25 V) and a pulse duration of 100 ms. The data indicates that the spike-rate-dependent plasticity (SRDP), or higher EPSC, is associated with more frequent presynaptic action potentials.[44]

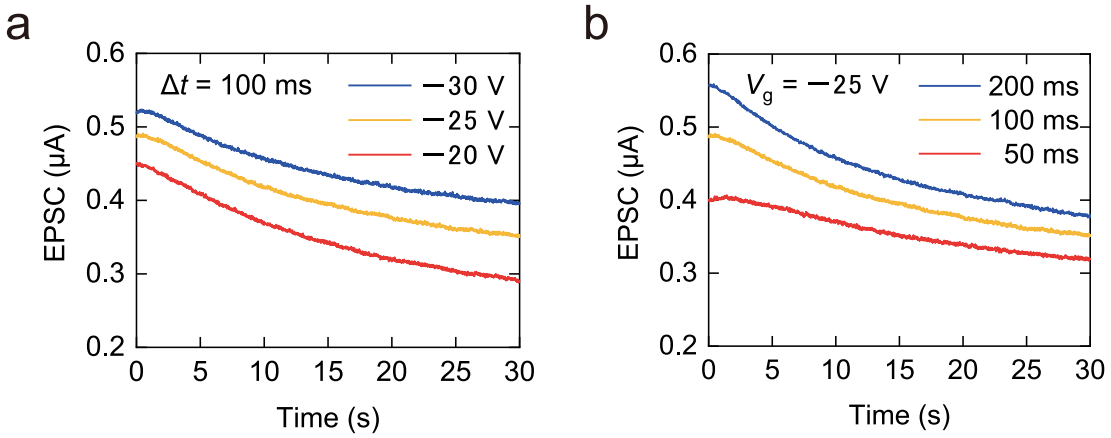

Figure 5.2. (a) EPSC generated with different amplitudes from −20 to −30 V. The pulse duration is set as 100 ms. (b) EPSC generated with different pulse duration from 50 to 150 ms. The amplitudes are set as −25 V.

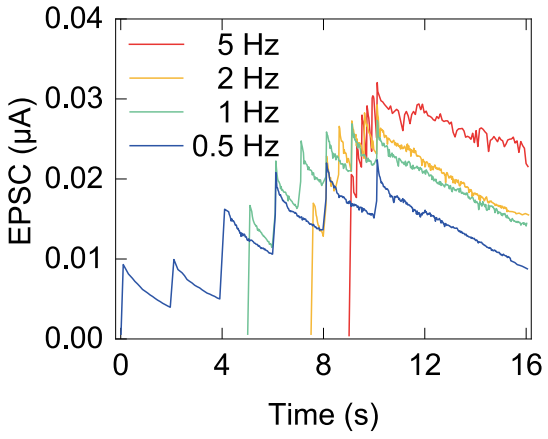

Figure 5.3. The SRDP behavior obtained in DFG synaptic transistor with six presynaptic spikes (pulse duration 100 ms, amplitude −25 V) from 0.5 to 5 Hz.

Spike-timing-dependent plasticity (STDP) is another essential synaptic function in learning and memory.[45] According to STDP, the strength of synaptic connections depends on the time interval between the presynaptic and postsynaptic spikes.[46] To demonstrate STDP implementation in the DFG transistor, the paired V_g pulse spikes (−25 V, 100 ms) with a time interval ($\Delta t = t_{pre} - t_{post}$) between presynaptic and postsynaptic spikes were applied (Figure 5.4). The synaptic weight change ($\Delta w = \Delta PCS / PCS$) was measured as a function of Δt, and the curves of Δw versus Δt could be fitted with the STDP learning rule inspired by biological synapse behavior.[47] When the presynaptic spike preceded the postsynaptic spike ($\Delta t > 0$), the connection strength increased to a greater extent with decreasing Δt, causing long-term potentiation (LTP). However, when the postsynaptic spike preceded the presynaptic spike ($\Delta t < 0$), the connection strength decreased to a greater extent with decreasing Δt, causing long-term depression (LTD). To confirm the LTP and LTD properties, the conductance states of the channel were measured for both the SFG and DFG devices through a set of pulse trains consisting of 32 identical pulses (time interval = 100 ms) for potentiation (−25 V, 100 ms) and depression (20 V, 100 ms), respectively (Figure 5.5). When the negative voltage pulse train was applied for potentiation, the conductance of the DFG transistor increased more linearly, whereas the conductance of the SFG transistor initially increased rapidly and then reduced owing to its low charge-storage capacity due to non-linearity, asymmetry, and low dynamic range. Thus, the G_{max} value of conductance, *i.e.*, the maximum conductance value indicating the available range of conductance modulation, was greater in the DFG transistor. Similarly, when the positive voltage pulse train was applied for depression, the conductance of the DFG gradually decreased, whereas the conductance of the SFG unsteadily decreased while inducing short-term plasticity at G_{max}. Notably, the excellent linearity and symmetry of conductance states in the DFG transistor are attributed to the separated double tunneling barriers, which provide efficient charge (de-)trapping in floating gates. Furthermore, by demonstrating the cycled LTP and LTD processes, good stability and reproducibility were observed in the DFG transistor (Figure 5.6). The linearity and symmetry of the DFG transistor can also be programmatically tuned via modulation of pulse amplitude for continuous learning[48] (Figure 5.7). These results imply that the synaptic behavior of biological neural systems was well emulated in the synaptic DFG transistor.

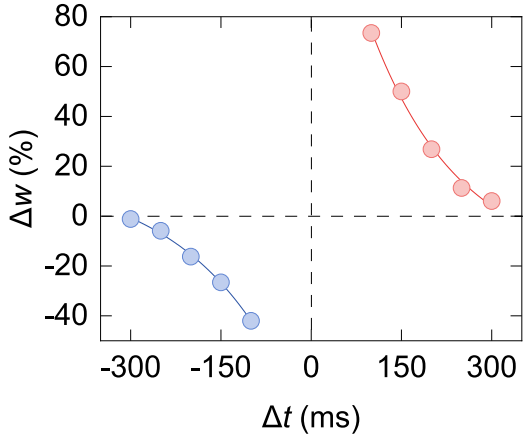

Figure 5.4. The STDP behavior obtained in DFG synaptic transistor and the corresponding fitting curves based on the model of biological STDP rules.

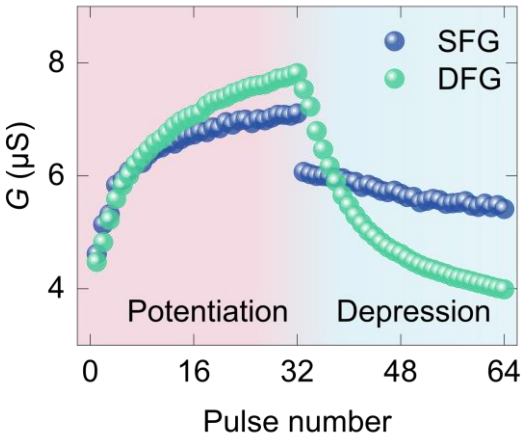

Figure 5.5. Potentiation and depression properties. The potentiation and depression process consist of 32 potentiation pulses, followed by the 32 depression pulses.

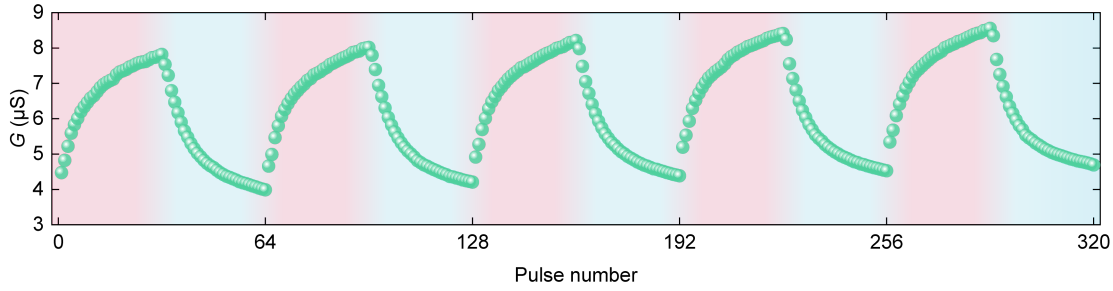

Figure 5.6. Cyclic endurance test for the synaptic device in 5 LTP-LTD cycles. All the data of *G* were collected using a reading voltage (V_{ds} = +0.1 V).

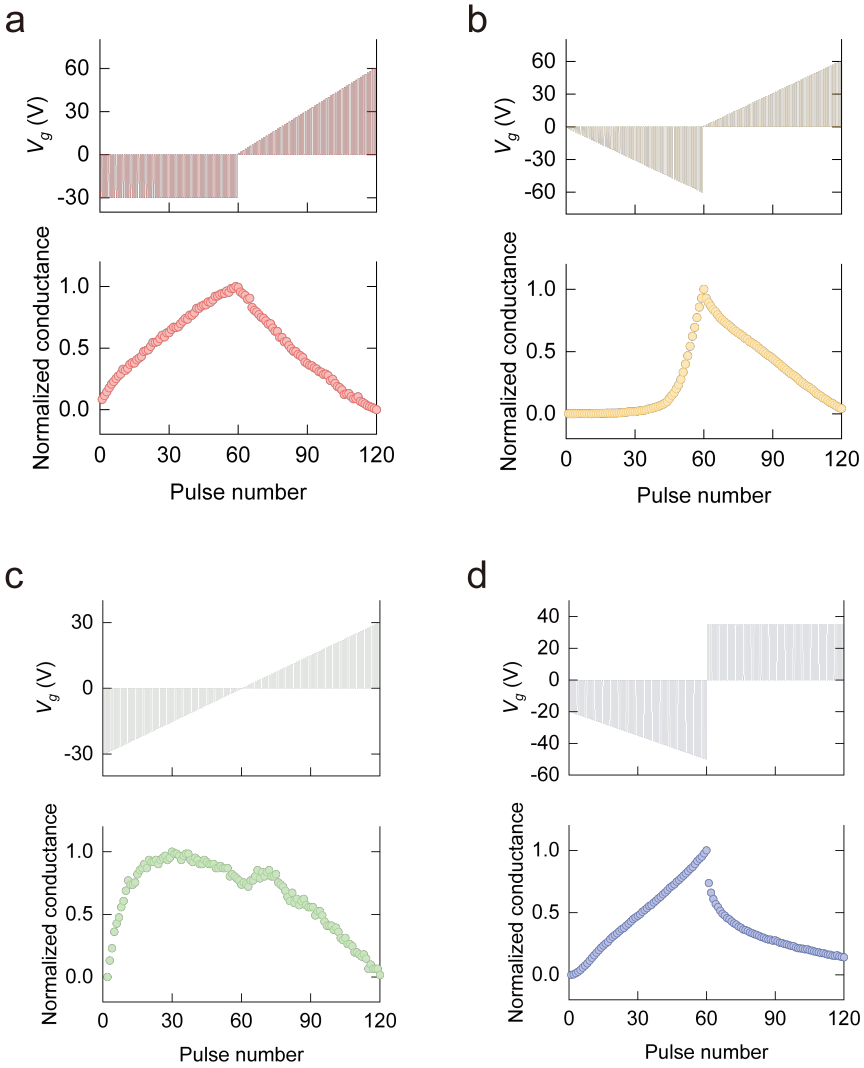

Figure 5.7. The LTP and LTD learning properties by pulse amplitude modulation with fixed pulse duration (100 ms) and time interval (100ms) in DFG device. The pulse train in the shape of (a) equal and increased, (b) only increased, (c) decreased and increased, and (d) increased and equal amplitude.

5.3 Synaptic operating system

The electric-stimulated synaptic characteristics of the devices were obtained by a source-meter (Keithley 2636B) with customized software. To generate various pulse shapes and measure synaptic properties of three-terminal devices, we have designed customized software using LabVIEW as shown in Figure 5.8. This customized software consists of Pulse List Mode, Voltage Bias Mode, two graphs, Measure Exclusion Range, Elapsed Time, Voltage Value, Current Value panels, and Increment Mode panels. In the Pulse List Mode panel, we should configure a source measure unit (SMU), On Time (pulse duration in this paper), Off Time, Bias, Pulse List (when a large number of pulses need to be configured, it can be generated using Increment Mode panel.), Compliance, Number of Power Line Cycle (NPLC), Iteration, and Measure Range. In the Voltage Bias Mode panel, another SMU is automatically selected, and we should configure bias, compliance, and measure range. If there is a problem with the pulse measurement due to the large measurement delay, the pulse measurement can be excluded using the exclusion range setting in the measurement exclusion range panel. In the upper and bottom graph panels, measured voltage (from SMU A(or B)) and current (from SMU B(or A)) values are displayed, respectively, in real time. Also, we can confirm the elapsed time and voltage and current numerical values in Elapsed Time, Voltage Value, and Current Value panel, respectively.

Figure 5.8. Keithley 2636B customized software using LabVIEW for synaptic measurements by pulse modulation.

Chapter 6. Neuromorphic Computing Simulation

6.1 Modified national institute of standards and technology (MNIST) and Fashion-MNIST image classification

Subsequently, image classification tasks were performed as a function of the training epoch to verify and further compare the potentials of SFG and DFG devices as artificial electronic synapses. Input, hidden, and output layers of our artificial neural network structure were each embedded with 784, 200, and 10 neurons, respectively (Figure 6.1). Two different datasets, MNIST (hand-written digits with 10 different classes) and Fashion-MNIST (Zalando's article images consisting of 10 different clothing classes), were used to fully investigate how long-term synaptic characteristics of SFG and DFG devices manifest themselves under two distinct environments. Both MNIST and Fashion-MNIST contain 60,000 train and 10,000 test images of 28 × 28 pixels.

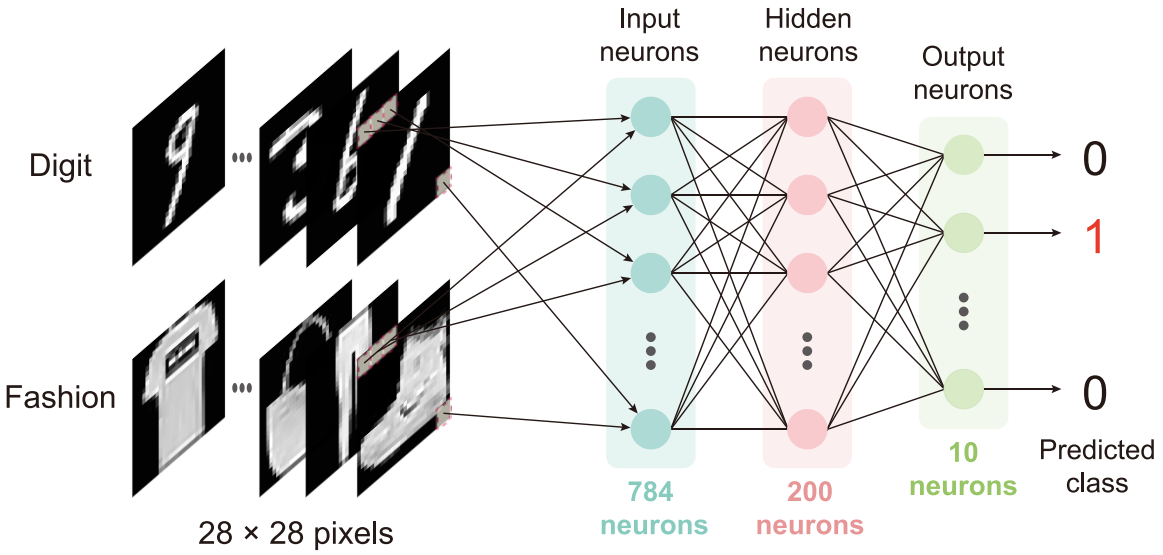

Figure 6.1. The scheme of artificial neural network for image classification on both MNIST and Fashion-MNIST dataset. The structure of the artificial neural network is three fully-connected layers with 784-200-10 neurons.

To adaptively apply the LTP/LTD curves (Figure 5.5) to such an ANN, the conductance values were first normalized (−0.1, +0.1). The intrinsic differences in conductance values between the SFG and DFG were maintained during normalization, upholding the overall shape of the normalized conductance

curves. This is possible because our SFG and DFG devices were fabricated to share the back gate and channel for precise floating-gate-effect comparison. For instance, the conductance G_{max}/G_{min} ratio of LTD was narrower than LTP in the case of the SFG, which is expected to limit the diversity and flexibility of synaptic weights, accordingly impacting its classification accuracy. To handle the inherent noise and variance (*e.g.*, cycle-to-cycle variation and device-to-device variation) from the device, we fitted our conductance curves using the following widely adopted fitting equations:[49-51]

$$G^+ = G^+_{min} + \frac{G^+_{max} - G^+_{min}}{1 - e^{-v^+ \cdot PN_{max}}} \cdot \left(1 - e^{-v^+ \cdot P}\right) + \sigma \quad (1)$$

$$G^- = G^-_{min} + \frac{G^-_{max} - G^-_{min}}{1 - e^{-v^- \cdot PN_{max}}} \cdot \left(1 - e^{-v^- \cdot (P - PN_{max})}\right) + \sigma \quad (2)$$

where G^+ (G^-) is the normalized conductance of LTP (LTD), P is pulse number, PN_{max} is the maximum pulse number applied to LTP or LPD, σ is normal distribution noise for device variance, and v^+ (v^-) is the coefficient of LTP non-linearity (LTD). Here, the coefficients v^+ (v^-) of our SFG and DFG devices were determined to be 0.11 (−0.02) and 0.09 (−0.10), respectively. The zero coefficient ($v^{+ \text{ or } -} = 0$) represents a perfect linear conductance learning curve.

6.2 Artificial neural network based on DFG device

Our training simulation was then conducted using the differential method, which uses 2-device for LTP and LTD. The conventional 2-device method, which is designed to implement negative synaptic weight values from positive-only conductance values of the devices, was applied to our SFG- and DFG-based artificial neural networks.[51-53] Furthermore, we controlled the conductance states using a single pulse in every update session to train the network moderately, avoiding unnecessary and wasteful device operations in a unidirectional manner of LTP/LTD changes. Figure 6.2 shows the accuracy curves of two datasets. In the case of hand-written digits, the accuracy achieved by the DFG was ~96.12%. However, the conductance of the SFG reached only ~91.99%. Similarly, for the Fashion-MNIST dataset, the result of the DFG (81.68%) was much more promising than that of the SFG (75.29%). The gray dashed line represents the ideal state (96.32% for MNIST, 83.98% for Fashion-MNIST), which is achieved by the pure linear conductance curve ($v^+ = v^- = 0$).

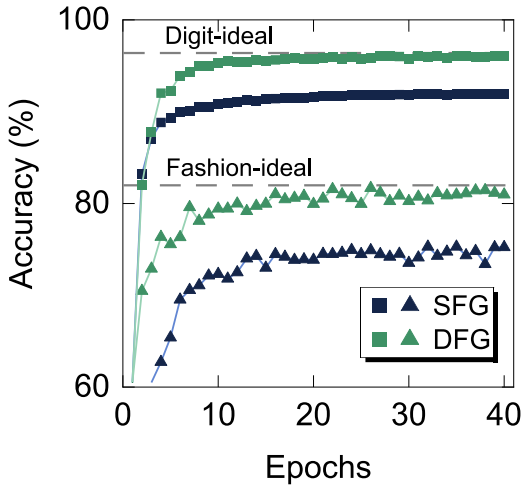

Figure 6.2. The classification accuracy of SFG and DFG device on MNIST and Fashion-MNIST dataset. The gray dashed lines represent accuracy of ideal cases without device effects (non-linearity) for the same network.

The training error comparison depicted in Figure 6.3 reveals the superiority of the DFG over the SFG as the DFG was suppressed close to that of the ideal, whereas the error of the ideal case was increased in the Fashion-MNIST dataset owing to the innate complexity in inter-class and intra-class images as compared with the MNIST dataset. To confirm the high dynamic range of the DFG, the trained synaptic weight distributions were compared (Figure 6.4). The weight distribution ranges of the SFG and DFG were ~0.082 and ~0.180 in the MNIST and Fashion-MNIST datasets, respectively. The fact that both datasets had the same ranges implies that the SFG and DFG synaptic neural networks fully utilize their conductance range capacity. The wider weight distribution in the DFG indicates an enhancement in the representation power of synaptic weights. Therefore, the DFG outperformed the SFG in terms of image classification. In other words, improved linearity, symmetry, and dynamic range driven by the same pulse were realized in the multiple (double in this study) charge-storage stacks for future synaptic devices as a promising platform for neuromorphic computing systems.

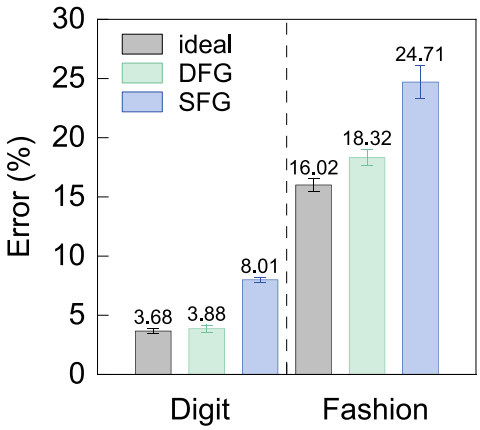

Figure 6.3. The error bar with standard deviation on MNIST and Fashion-MNIST dataset, which is obtained through three training trials.

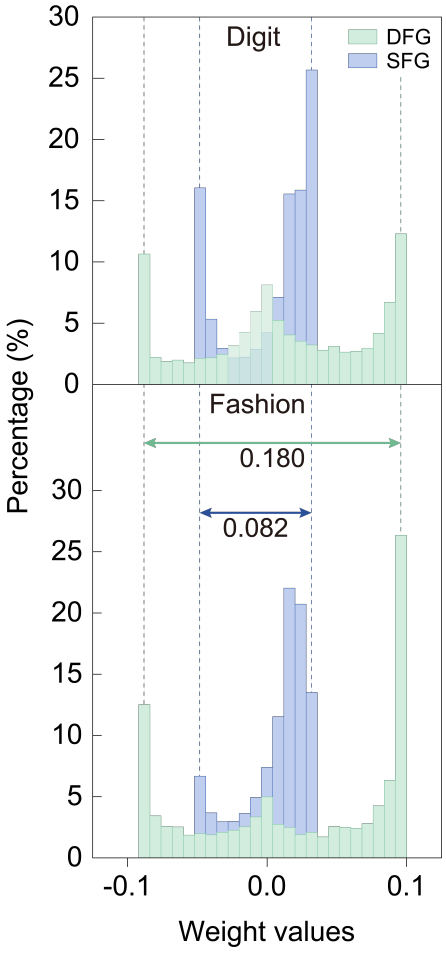

Figure 6.4. The weight distributions of two datasets and two devices after training session. The vertical dashed lines illustrate the minimum and maximum values of weight values.

6.3 Pattern recognition simulations

In order to confirm the learning capability of our SFG/DFG devices, we built the network structure as three fully-connected (FC) layers with 784, 200, and 10 neurons. We controlled the conductance states by only using a single pulse in every update session to train the network moderately, avoiding unnecessary and wasteful device operations in a unidirectional manner of LTP/LTD changes. The above pattern recognition training was implemented with Python using MNIST and Fashion-MNIST dataset.

Chapter 7. Conclusion

We introduced an artificial synaptic DFG transistor concept built from 2D materials and vdW heterostructures using the charge (de-)trapping mechanism. This type of memory has excellent performance with the benefits of a large memory widow (100 V), high on–off current ratio (10^7), long retention performance (5000 s), and substantial cyclic endurance (500 cycles). Furthermore, we propose a tunneling behavior for DFG devices using energy-band diagrams that indicate how double floating gates prevent high charge loss and precisely control charge (de-)trapping events while storing more charges. Future exploration of the basic functions of biological synapses, including EPSC, SRDP, STDP, LTP, and LTD, could be emulated. Moreover, the DFG transistor exhibited improved linearity, symmetry, and dynamic range of synaptic weight update owing to the double tunneling barriers and floating gates for charge redistribution. High classification accuracies of up to 96.12% and 81.68% were achieved for MNIST and Fashion-MNIST, respectively. Consequently, the artificial synaptic DFG transistor could support next-generation neuromorphic computing based on precise charge modulation and robust charge storage.

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