2009, Porto, Portugal.

Comparisons between Synchronizing Circuits to Control Algorithms for Single-Phase Active Converters

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***Abstract* – This paper presents a comparative analysis between synchronizing circuits applied to control algorithms for single-phase active converters. One of these synchronizing circuits corresponds to the single-phase PLL (Phase Locked Loop), implemented in α-β coordinates, whereas the other one corresponds to the E-PLL (Enhanced PLL). These synchronizing circuits are compared in several aspects as processing and settling time and memory space requirements. Moreover, the performance of a single-phase back-to-back converter is also presented, with its control algorithm based on these Synchronizing Circuits. Each one of the control algorithms were implemented in a DSP microprocessor TMS320F2812F from Texas Instruments. Simulation and experimental results, through a back-to-back converter prototype, are presented.**

I. INTRODUCTION

The proliferation of nonlinear loads in residences, offices and industries has contributed to increase the harmonic pollution observed in the power grid. Moreover, the harmonic current-components consumed by these nonlinear loads results in harmonic voltage-drop on the supply line impedances, which deteriorates the waveform of the voltages delivered to the load [1]. There are also other events as voltage sags or voltage swells that are resulted, respectively, from connection or disconnection of large loads [2] [3]. All of these events are the most responsible ones for the observed problems in sensitive loads as improperly shut down, reduced lifetime, malfunction, and so others.

Power quality problems can be overcome, in real time, through the utilization of "Custom Power" devices. In this paper a back-to-back converter is used, which is composed by two power converters that are connected in series and in shunt with the power grid. The shunt converter consists in an active rectifier that injects or absorbs energy from the power grid, in order to keep the dc-link voltage regulated. The series converter is responsible to compensate the major power quality problems related with the system voltages, such that the voltage delivered to the load remain regulated and with low harmonic distortion.

To control these converters, control algorithms based on the instantaneous power theory (*p – q Theory*) are applied [4] together with a synchronizing circuit. The synchronizing circuit is responsible to produce, in real time, sinusoids that are synchronized with the fundamental component of the system voltage. Thus it can be observed its importance, since the voltage produced by the series converter depends, directly, on the generated sinusoid by the synchronizing circuit.

Due to the importance of the synchronizing circuit, this paper investigates two different topologies. The first one corresponds to the single-phase PLL (Phase - Locked - Loop) [4] [5] [6] [7] [8], implemented in α-β coordinates, whereas the other one corresponds to the E-PLL (Enhanced PLL) [9] [10] [11].

The comparison involving these PLL topologies is focused in processing and settling time and memory space requirements. Both controllers where implemented in a DSP microprocessor TMS320F2812F from Texas Instruments. Being a real time processing system, computing speed and memory usage, as well as the settling time are important issues. These characteristics must be enhanced; moreover, they most provide compensated voltages that comprises with the power quality standards [12]. Simulation and experimental results, through a back-to-back converter prototype, are presented.

II. HARDWARE CONFIGURATION

As aforementioned in this paper and indicated in Fig. 1, the back-to-back converter is composed by two power converters that are connected in series and in shunt with the power grid. A step-down transformer (5 kVA – 230 V//115 V) is used to provide galvanic isolation between the power converters and the power grid. Another step-down transformer, with the same characteristics, is used to connect the shunt converter with the power grid. The series converter is directly connected with the power grid.

Each one of the single-phase power converters is composed by two branches (4 IGBTs with anti-parallel diodes) from model Semikron SKM-50GB063D [13]. The IGBTs of this power module present as main features a collector-emitter voltage of 600 V and a collector current of 50 A (peak value).

The dc-link is composed by three 4700 μF capacitors connected in series, which corresponds to an equivalent capacitor of, approximately, 1566.67 μF. Each one of these capacitors presents a dc-voltage rating of 450 V.

The RLC coupling filter of the series converter is composed by a 15 Ω resistor (R_{fs}), an 8.8 μF capacitor (C_{fs}), and an air-core inductor of 0.6 mH (L_{fs}). The RLC filter of the

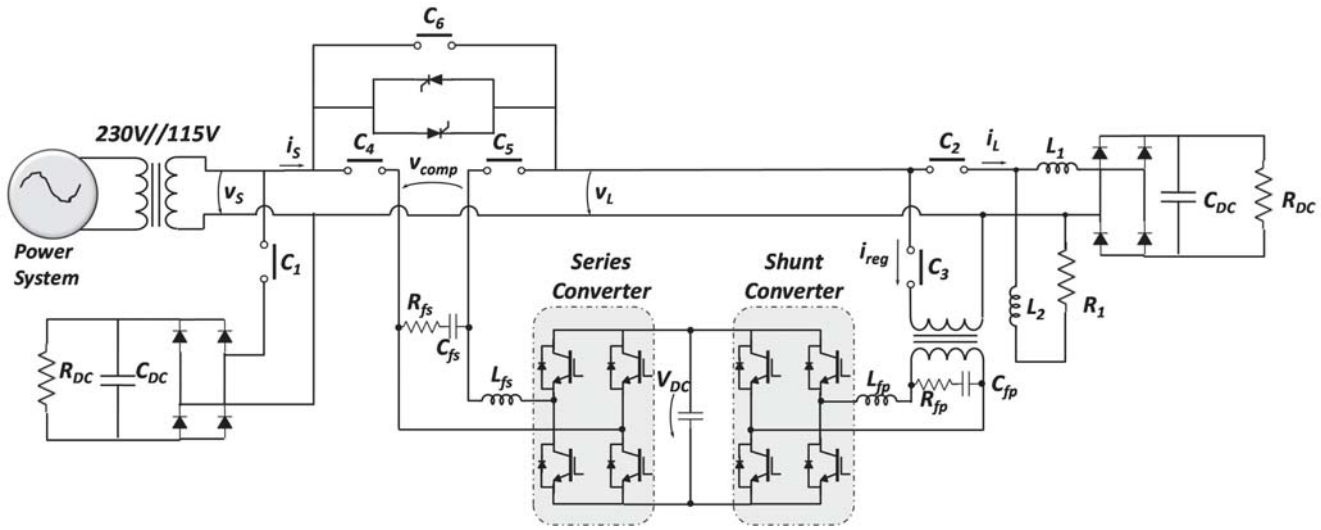

Fig. 1. Electrical Diagram of the Single-Phase Back-to-Back Converter.

shunt converter is comprehended by a 0.6 mH inductor (L_{fp}), an 4 Ω resistor (R_{fp}), and an 2.2 μF capacitor (C_{fs}).

The nonlinear load consists of a single-phase diode rectifier, with a RC Load on the dc-side (C_{DC} = 4,7 mF and R_{DC} = 25 Ω). To smooth the current waveform, it is used a 3 mH inductor (L_1). There is also a linear load, connected in shunt with the nonlinear load, composed by a 30Ω resistor (R_1) and a 650 μH inductor (L_2).

A diode rectifier, similar to the nonlinear load, is used to increase the harmonic distortion of the supply voltage. This rectifier is located between the transformer, connected in series with the power grid, and the series converter.

A soft-start circuit was implemented to suppress the lack of electric isolation of a coupling transformer that is present in the majority of series converters [13]. It also acts as a protection system to overloads and short-circuits. Moreover, contactors are employed to connect the shunt (C_3) and series (C_4, C_5, C_6) power converters, as well as to connect the loads with the electrical system (C_1, C_2).

The supply voltage is represented in Fig. 1 as being v_S, and the load voltage is v_L. The produced voltage by the series converter is represented as v_{comp}. The load and source currents are represented as i_L and i_S, respectively. The controlled current (i_{reg}) is produced by the shunt converter in order to regulate the DC link voltage.

III. Controller of the Back-to-Back Converter

As introduced in section I the controller of the back-to-back converter is constituted by control algorithms to determine the reference signals to be produced by the power converters, plus switching algorithms to command the IGBTs. The control algorithms to determine the reference signals are comprehended by a synchronizing circuit, an algorithm to determine the compensating currents and an algorithm to determine the compensating voltages. In Fig. 2 is shown a block diagram that represents the control algorithms to determine the reference signals. The control algorithms denominated in Fig. 2 as "Current-Reference Algorithm" and "Voltage-Reference Algorithm" are based on the concepts involving the instantaneous power theory (*p – q Theory*) with some simplifications. Hereafter, these control algorithms are described, and, in sequence, the investigated synchronizing circuits are introduced.

A. Current-Reference Algorithm

Since there are no power sources on the dc side of the power converter, a controller that keeps the dc-link voltage regulated has to be implemented. It is worth to notice that, with only this control algorithm, the shunt converter does not provide active filtering. In this case, the shunt converter can be considered as an active rectifier. Based on the dc-link voltage (v_{DC}), the control signal p_{Reg} is determined as described as follows:

$$p_{Reg} = (v_{Ref} - v_{DC}) \cdot (k_{p\_dc} + \frac{k_{i\_dc}}{s}) \quad . \tag{1}$$

The control signal p_{Reg} can be understood as an amount of energy, per time unit, that is drained or injected by the shunt converter in order to keep the dc-link voltage regulated. As indicated in (1), the control signal v_{Ref} corresponds to the

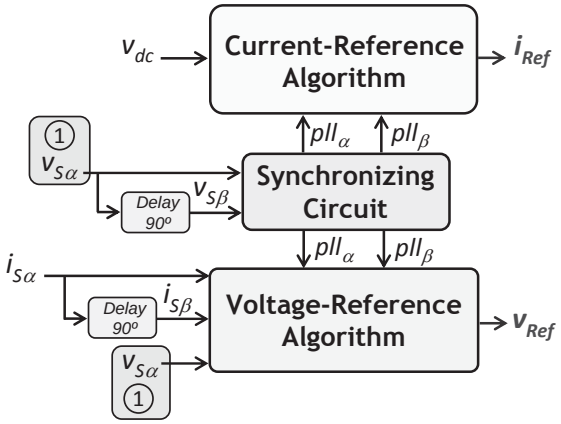

Fig. 2. General control scheme of the algorithms that determine the reference signals.

reference value of the dc-link voltage, and the control signals $\square_{p\square dc}$ and $\square_{i\square dc}$ represent, respectively, to the proportional and integral gains of the PI-Controller.

In sequence, the mathematical methodology to determine the reference signal i_{Ref} is described. Since this algorithm is based on the $p-q$ *Theory*, consider that is necessary to determine the reference signals in αβ coordinates ($i_{Ref\square\alpha}$, $i_{Ref\square\beta}$) as described as follows:

$$\begin{bmatrix} i_{Ref\square\alpha} \\ i_{Ref\square\beta} \end{bmatrix} = \frac{1}{pll_\alpha^2 + pll_\beta^2} \cdot \begin{bmatrix} pll_\alpha & pll_\beta \\ pll_\beta & -pll_\alpha \end{bmatrix} \cdot \begin{bmatrix} p_{Reg} \\ 0 \end{bmatrix} \quad , \tag{2}$$

where, the signals pll_α and pll_β are generated by the synchronizing circuit. For now, it is assumed that these signals are sinusoidal waveforms, with unitary amplitude, and are in phase with the fundamental frequency of the control signals $v_{S\alpha}$ and $v_{S\beta}$, respectively. After some simplifications in equation (2), $i_{Ref\square\alpha}$ and $i_{Ref\square\beta}$ are given by:

$$\begin{aligned} i_{Ref\square\alpha} &= \frac{pll_\alpha \cdot p_{Reg}}{pll_\alpha^2 + pll_\beta^2} = pll_\alpha \cdot p_{Reg} \quad \square \\ i_{Ref\square\beta} &= \frac{pll_\beta \cdot p_{Reg}}{pll_\alpha^2 + pll_\beta^2} = pll_\beta \cdot p_{Reg} \quad . \end{aligned} \tag{3}$$

Indeed, since the control signals pll_α and pll_β are sinusoids with unitary amplitude and pll_α leads $\square 0\square$ pll_β, it can be assumed that the sum of their square values is equal to one.

Based on the Clarke Transformation [13] [14] and assuming a "fictitious" three-phase three-wire system, the control signal i_{Ref} is given by:

$$\begin{bmatrix} i_{Ref} \\ 0 \\ 0 \end{bmatrix} = \sqrt{\frac{2}{3}} \cdot \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} i_{Ref\square\alpha} \\ i_{Ref\square\beta} \end{bmatrix} \quad . \tag{4}$$

As it can be observed in (4), i_{Ref} is only associated with $i_{Ref\square\alpha}$. Combining (3) and (4) the reference signal i_{Ref} can be determined in a very simple way as described as follows:

$$i_{Ref} = \sqrt{\frac{2}{3}} \cdot \square pll_\alpha \cdot p_{Reg} \square \quad . \tag{5}$$

Based on the aforementioned e□planation, it can be noted that the computational effort to determine i_{Ref} is directly related with the synchronizing circuit and with the PI-Controller. In sequence, the control algorithm that determines the reference voltage v_{Ref} is described.

□. □olt□ge-Reference Algorithm

As illustrated in Fig. 3, this algorithm presents as inputs the signals derived from the source current (i_S) in αβ coordinates ($i_{S\alpha}$, $i_{S\beta}$), the control signal obtained from the system voltage($v_{S\alpha}$), plus the signals generated by the synchronizing circuit (pll_α, pll_β). In this algorithm there is also a control block that determines control voltages with the objective to damp resonance phenomena, denominated as "Damping

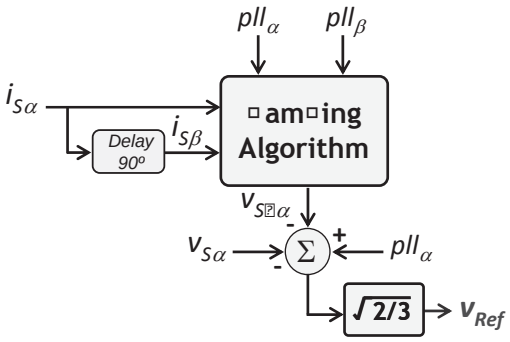

Fig. 3. Diagram blocks of the Voltage-Reference Algorithm

Algorithm" block. Indeed, as described in [6], instability problems due to the resonance phenomena, involving the passive filters and the system impedance, may occur. In order to enhance the overall system stability, an au□iliary algorithm can be added to the controller of the series converter. In sequence, it is described a mathematical methodology, based on the $p-q$ *Theory*, to determine the control signal $v_{S\square\alpha}$.

In a similar way of the presented one in (4) the control signals $i_{S\alpha}$ and $v_{S\alpha}$ are determined, respectively, from the source current (i_S) and system voltage (v_S) as described as follows:

$$\begin{aligned} i_{\square\alpha} &= \sqrt{\frac{3}{2}} \cdot i_{\square} \quad \square \\ v_{\square\alpha} &= \sqrt{\frac{3}{2}} \cdot v_{\square} \quad . \end{aligned} \tag{6}$$

The signal $i_{S\beta}$ is shifted by $\square 0\square$ from $i_{S\alpha}$. The control signals $i_{S\alpha}$ and $i_{S\beta}$, together with to the ones generated by the synchronizing circuit (pll_α, pll_β) are applied to calculate the real and imaginary powers as described as follows:

$$\begin{bmatrix} p \\ q \end{bmatrix} = \begin{bmatrix} pll_\alpha & pll_\beta \\ pll_\beta & -pll_\alpha \end{bmatrix} \cdot \begin{bmatrix} i_{\square\alpha} \\ i_{\square\beta} \end{bmatrix} \quad . \tag{7}$$

In sequence, the control signal $i_{S\square\alpha}$ is determined according to the following equation:

$$\begin{bmatrix} i_{\square h\alpha} \\ 0 \end{bmatrix} = \frac{1}{pll_\alpha^2 + pll_\beta^2} \cdot \begin{bmatrix} pll_\alpha & pll_\beta \\ pll_\beta & -pll_\alpha \end{bmatrix} \cdot \begin{bmatrix} \square \tilde{p} \\ \square \tilde{q} \end{bmatrix} \quad , \tag{□}$$

where, the powers $\square\tilde{p}$ and $\square\tilde{q}$ corresponds to the oscillating components of the real (p) and imaginary ($\square$) powers, and they can be obtained through high-pass filters. The direct product involving the control signal $i_{S\square\alpha}$ by a gain denominated as $\square_{\square}$ results in the harmonic controlled-voltage ($v_{S\square\alpha}$). The gain $\square_{\square}$ can be understood as a resistance only for the harmonic components. Further details involving the damping algorithm are described in [14].

Finally, the reference voltage (v_{Ref}) is determined as indicated in Fig. 3. □hen v_{Ref} is produced by the series converter, it is e□pected that power quality problems

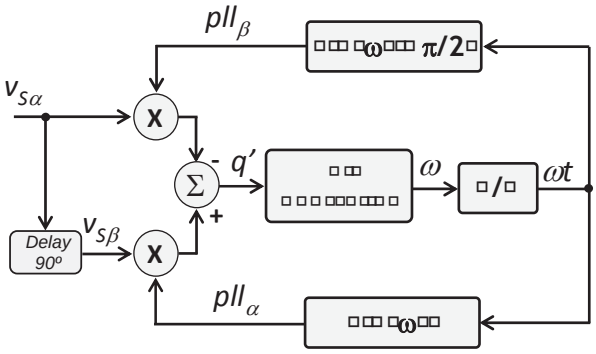

Fig. □ □ingle-□hase □hase-□ocke□-□oo□

obser□e□ at the s□stem □oltages can be com□ensate□□an□□ moreo□er□it is e□□ecte□that □roblems relate□ □ith resonance □henomena can be a□oi□e□ □n se□□ence are □resente□ the s□nchroni□ing circ□its aforementione□in section □.

C. *Single-Phase Phase-Locked-Loop (Single-Phase PLL)*

□his s□nchroni□ing circ□it is similar to the one im□lemente□ to three-□hase s□stems□ □ith some sim□lifications as intro□□ce□in □□□. □n Fig. □is ill□strate□the single-□hase □□□ in αβ coor□inates.

As in□icate□in Fig. □□the fee□back signals pll_α an□ pll_β are b□ilt □□ b□ the □□□ circ□it□□st □sing the time integral of o□t□□t ω of the □-□ontroller. □hese fee□back signals ha□e □nit□ am□lit□□e an□ pll_α lea□s □□□ pll_β. □he □□□ circ□it becomes stable onl□ if the a□erage com□onent of the □fictitio□s□imaginar□ □o□er reaches □ero □al□e □$\tilde{q}' = 0$ □an□ has minimi□e□ lo□-fre□□enc□ oscillating □ortions in its oscillating com□onent $\tilde{q}'$. □nce the circ□it is stabili□e□□the a□erage □al□e of q' is □ero an□□□ith this□the □hase angle of the f□n□amental fre□□enc□ is reache□. At this con□ition□the fee□back signal pll_α becomes in □hase □ith the f□n□amental com□onent of the control signal $v_{S\alpha}$. F□rther e□□lanations in□ol□ing this □□□ for three-□hase s□stems are □resente□ in □□□.

□ereafter□it follo□s some sim□lation res□lts relate□ □ith the single-□hase □□□. □nitiall□□in this case test□the in□□t signal corres□on□s to $v_{S\alpha} = 100 \cdot sin\,(\omega t + 45º)$. At $t = 2.0\ s$ □the □hase angle of the in□□t signal is mo□ifie□□s□ch that the mo□ifie□in□□t signal corres□on□s to $v_{S\alpha} = 100 \cdot sin\,(\omega t + 90º)$.

□n Fig. □is sho□n the □erformance of the single-□hase □□□ tracking the in□□t signal $v_{S\alpha} = 100 \cdot sin\,(\omega t + 45º)$. □he □□□ starts at $t = 0.1\ s$. After □ c□cles□the control signal pll_α tracks the in□□t signal $v_{S\alpha}$.

Fig. □ ill□strates the control signal pll_α tracking the in□□t signal $v_{S\alpha}$□at the transient □$t = 2.0\ s$□□hen the □hase angle of the in□□t signal □φ_{Ref}□is increase□ from □□□to □□□. As it can be seen in Fig. □□at $t = 2.07\ s$□the control signal pll_α tracks again the in□□t signal $v_{S\alpha}$.

□ase□ on these □reliminar□ sim□lation res□lts□it can be note□ the feasibilit□ of this s□nchroni□ing circ□it. □t can also be seen in literat□re □□□□□the □erformance of this □□□ □n□er □orse con□itions than the □resente□ones in this □a□er.

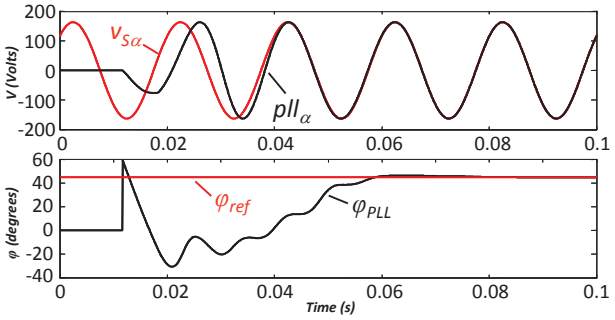

Fig. □ □erformance of the single-□hase □□□ to track the in□□t signal □$v_{S\alpha}$□.

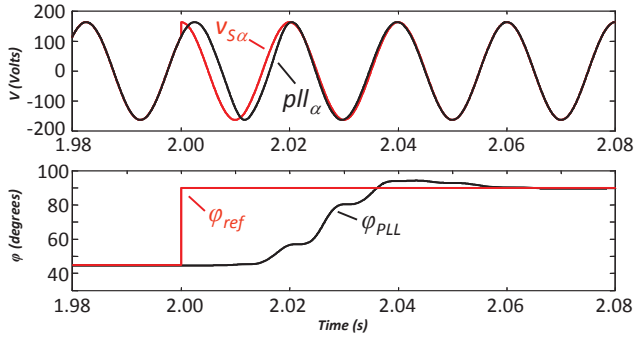

Fig. □ □erformance of the single-□hase □□□ to track the in□□t signal □$v_{S\alpha}$□□ □hen the □hase angle □φ_{ref}□is mo□ifie□from □□□to □□□.

D. *Single – Phase Enhanced PLL*

□n Fig.□□the □ro□ose□ algorithm is sho□n as a block □iagram of the □nhance□ □□□ □□□□□□□□. □riginall□□the □□□□ com□rises a control loo□ to □etermine the am□lit□□e□ an□another control loo□that e□tracts the fre□□enc□an□□hase angle of the in□□t signal. □herefore□□ifferent from the □□□□ the □-□□□ reall□ □etermines the f□n□amental com□onent of the in□□t signal□□hich one is com□rehen□e□b□its am□lit□□e□ fre□□enc□an□□hase angle.

□nfort□natel□□it is □esire□that the generate□signals b□the s□nchroni□ing circ□it □resent constant am□lit□□e. □h□s□the generate□signals □ro□□ce□b□the □□□□ □$Epll_\alpha$ □$Epll_\beta$□can not be □irectl□ □se□. □n Fig. □the single-□hase □□□□ is sho□n. □e□t□it follo□s a brief □escri□tion in□ol□ing the □□□□ str□ct□re □ith the a□□lie□mo□ification.

□he error signal e corres□on□s to the total □ist□rbance bet□een the in□□t signal $v_{S\alpha}$ an□ the generate□ one b□ the □□□□ □$Epll_\alpha$□. □he fee□back signals $cos\,(\omega t)$ an□ $sin\,(\omega t)$ are

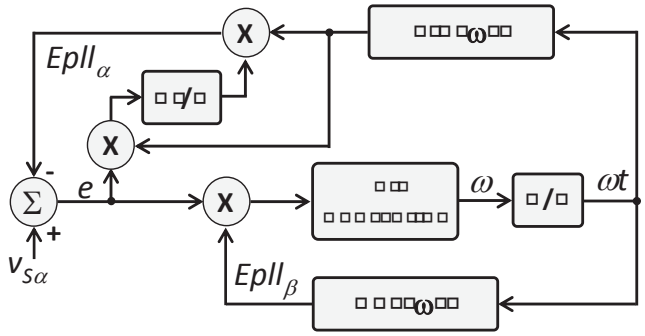

Fig. □ □ingle-□hase □nhance□ □□□ □□□□□□

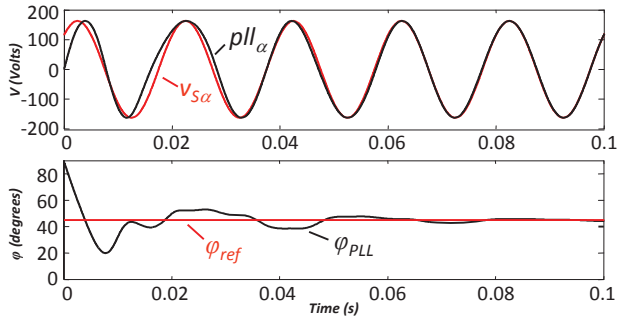

Fig. 8. Performance of the single-phase EPLL to track the input signal ($v_{s\alpha}$).

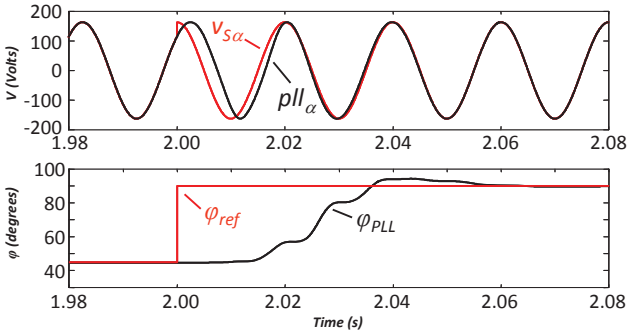

Fig. 9. Performance of the single-phase EPLL to track the input signal ($v_{s\alpha}$), when the phase angle (φ_{ref}) is modified from 45º to 90º.

b□ilt □□ □sing the time integral of o□t□□t ω of the □□-□ontroller. □he □□□□ circ□it becomes stable onl□ if the a□erage com□onent of the error signal □e□reaches □ero □al□e. □nce this circ□it is stabili□e□□the control signal $Epll_\alpha$ tracks the in□□t signal $v_{s\alpha}$ an□□as a conse□□ence□the □hase angle of the f□n□amental fre□□enc□ is reache□. F□rther e□□lanations in□ol□ing the □□□□ are □resente□ in □□□□□□□□. □n Fig. □ an□ Fig. □are □resente□ the sim□lation res□lts □ith the same test cases a□□lie□to the single-□hase □□□.

□V. □□ □□R□□ □□□A□R□□□ □□□

□he s□nchroni□ing circ□its □ere im□lemente□on the □e□as □nstr□ments □□ □3□□F□□□□F D□□ micro□rocessor. For memor□ re□□irements assessment□ □ariables si□e □as meas□re□. □n □able □□ the □ariables n□mber an□ si□e are sho□n an□ total memor□ s□ace □eman□e□ for each s□nchroni□ing circ□it is calc□late□.

□A□□□ □

□□□□□R□□□□□□ □□R□□□□ □ □□ □R□ R□□□□R□□ □□□□

Type	Memory Space	
	Single-Phase PLL	Enhanced PLL
double	(4 x 32) 128 bits	(6 x 32) 192 bits
long int	(14 x 32) 448 bits	(17 x 32) 672 bits
long int array	(640 x 32) 20480 bits	-
TOTAL	21096 bits	864 bits

The system voltage is sampled 640 times each grid period. These instantaneous values are stored in a 640 position array, which is used to create the 90° shifted signal used in the Single-Phase PLL. This causes the Single-Phase PLL

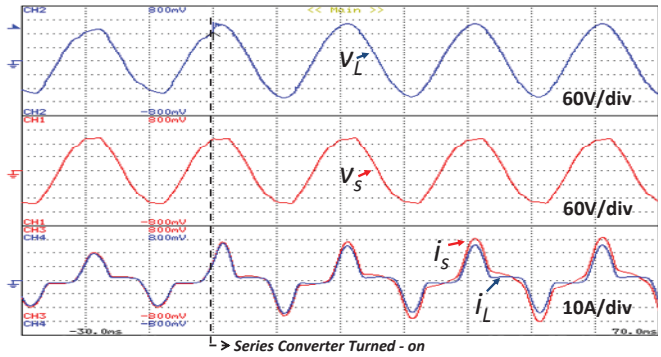

Fig. 10. Voltages and currents of the system when the Series Active Conditioner with single-phase PLL is turned on.

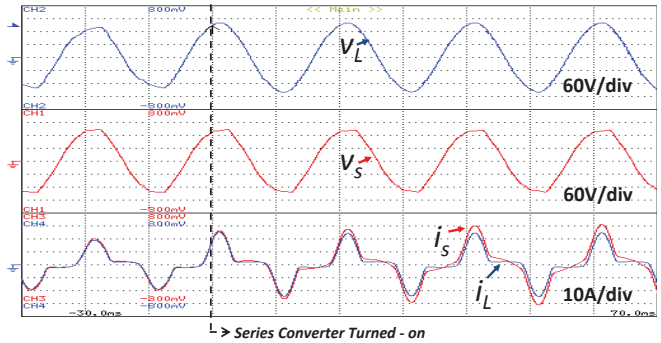

Fig. 11. Voltages and currents of the system when the Series Active Conditioner with EPLL is turned on.

memory requirements to be wider than the EPLL. Given the vast amount of memory available in the selected microprocessor, this matter has a small importance.

The processing speed of each synchronizing circuits was also measured. This was made by counting the system clock cycles of the synchronizing circuit routine. The all control system has a 31.25 µs available processing time, actuating 640 times by grid cycle. The DSP TMS320F2812F system clock frequency was set at 135MHz. The EPLL synchronizing circuit takes 2197 system clock cycles, which corresponds to 16.27 µs. It occupies 52% of the control system routine available time. The Three-Phase Adapted PLL takes 1511 system clock cycles, 11.19 µs, which corresponds to 35.8% of the available processing time.

To evaluate performance characteristics, the Series Active Conditioner was set to compensate the load voltage distortion. For each proposed algorithm, the load voltage (v_L) presents a 7.9% THD, and a RMS value of 102.2V before compensation. In Fig. 10 is shown the systems voltages and currents when the Conditioner starts with the Single-Phase PLL. v_L THD drops to 2.1%, and the RMS value rises to 114.3 V. In Fig. 11 is showed the same transient, being the EPLL the synchronizing circuit. v_L THD drops to 2.1% and RMS value is of 114.3 V. The two synchronizing circuits present the same behavior in this transient analysis. In both cases it can be seen that i_S rises, in order to regulate the DC link voltage.

Another transient was applied to the system. It consisted in closing contactor C_1 (see Fig. 1,) thus connecting the shunt

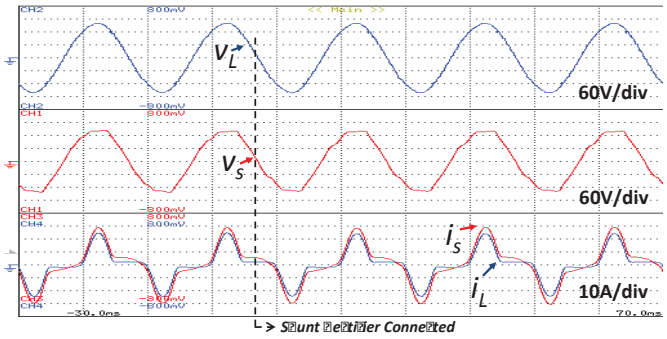

Fig. 12. Series Active Conditioner with Single-Phase PLL under the connection of the shunt rectifier. Dot line marks the connection of the rectifier.

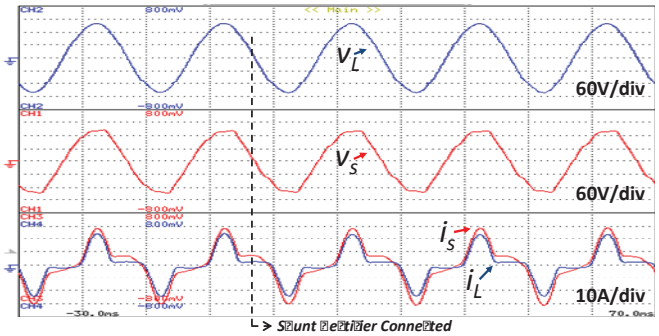

Fig. 13. Series Active Conditioner with Single-Phase PLL under the connection of the shunt rectifier. Dot line marks the connection of the rectifier.

rectifier to the system, with the series converter turned on. This action would degrade v_L THD to 8.8%, and the RMS value to 99.7V if there was no compensation. In Fig. 12 can be seen the system voltages and currents when the rectifier is connected with the Conditioner already compensating, with the Single-Phase PLL algorithm. It can be seen that v_S becomes more distorted, but v_L maintains a low THD. It is of 1.8% and the RMS voltage is at 115 V. The same values where obtained when the same transient was applied to the system with the Conditioner compensating using the EPLL algorithm. This can be seen in Fig. 13. Since the distortion in v_L increases, the series converter has to inject more power in order to compensate it. This forces the shunt power converter of the Conditioner to drain more power to regulate the DC link. Thus, an increased system current (i_S) is also observed. Also, the compensated v_L. THD is improved when compared with the first analysis. This is due to the increasing of v_{ref} that leads to a better modulation index of the series power converter.

V. CONCLUSIONS

A comparison between to synchronizing circuits for the control algorithm of a Series Active Converter is made in this paper.

The Single-Phase PLL presents higher memory requirements. But given the vast amount of memory available in the selected microprocessor, this matter has a relative importance. His synchronizing circuit, however, presents higher speed performance. In a real time processing control system, this is an important advantage, since it releases time for other processing routines. In this particular, the Single-Phase PLL can overtake the Enhanced PLL. Even though the EPLL uses less memory resources, its processing time is long. Thus, one can conclude that the Single-Phase PLL is more suited for real time processing systems such as the one presented in this paper.

Experimental results also showed that the compensated load voltage (v_L) delivered to the load is in accordance with international standards that regulate harmonic distortion and RMS value. These standards are CEI 61000 and ANSI/IEEE 519 -1992 for harmonics. For RMS value, the standard taken in account is ANSI/IEEE 519 - 1992, that describes power quality problems. This was seen on both synchronizing circuits.

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