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A Control Strategy for a Three-Phase Four-Wire Shunt Active Filter

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***Abstract*- This paper presents a control strategy for a three-phase four-wire shunt active filter. The shunt active filter is a custom-power device capable to compensate, in real time, harmonics, unbalances and power factor in an electrical installation. In this work the power circuit is based on a three-leg IGBT inverter, with the dc-link composed by two capacitors connected in split. Thus the neutral point is connected directly to the midpoint of the dc-link capacitors. Its control system is composed by an algorithm based on the active and non-active currents together with a synchronizing circuit, and a novel algorithm to keep the voltages of the dc-link capacitors balanced and regulated. Due to the applied power-inverter topology, it is imperative to keep these voltages of the dc-link capacitors balanced in order to avoid malfunctioning of the active filter. To validate the proposed control strategy, simulation and experimental results are presented.**

Keywords — Power Quality, Shunt Active Filter, Real-Time Control System, dc-link voltage regulation.

I. INTRODUCTION

The intensive use of power converters and non-linear loads has contributed for the deterioration of the power quality, and this factor affects critical processes, resulting in substantial economical losses. Therefore the development of equipments capable to mitigate problems that affect electrical installations is of great interest [1] [2]. Devices based on power electronics directed to improve power quality are denominated as "Custom-Power".

The shunt active filter is a custom-power device capable to compensate, in real time, harmonics, unbalances and power factor in an electrical installation. Since the shunt active filter deliver to the load these components, the currents at the electrical system become sinusoidal, balanced and in phase with the fundamental positive-sequence component of the system voltages.

This work describes a three-phase four-wire shunt active filter, where the neutral wire is connected directly to the midpoint of the dc-link capacitors. Thus the power inverter is composed by only six semiconductor devices (IGBTs).

A disadvantage of this topology is the fact that the size of the dc-link capacitors has to be over-dimensioned. However this drawback does not make impracticable to implement a shunt active filter with this topology. As described in [3], there are manufactures that develop shunt active filters with this topology, for power systems based on 400 V (line voltages) and currents up to 120 A.

The control system is composed by an algorithm to determine the reference currents that are injected by the shunt active filter and another one to keep the voltages of the dc-link capacitors regulated and balanced. The algorithm that determines the reference currents is based on the theory of the active and non-active currents [4] [5]. This algorithm is implemented together with a digital PLL (Phase Locked Loop) [6].

Due to the applied power inverter topology, with the neutral wire connected at the midpoint of the dc-link capacitors, it is necessary to design an algorithm that regulates and balances these dc-link voltages. This algorithm constitutes an original contribution of this work.

As mentioned in [7], a few papers have been published on voltage-balancing control for active filters. In [8] [9] were also proposed voltage-balancing algorithms for three-phase four-wire active filters based on three-leg inverters, with the neutral wire connected at the midpoint of the dc-link capacitors. As advantages of the proposed algorithm in this paper, in comparison with those introduced in [8] [9], are its very simple structure and its suitability for implementation with any switching technique.

A summary involving the major topics of this paper is described as follows. Aspects related to the system configuration of the shunt active filter are illustrated in Section II. A set of equations describing the control system based on the theory of the active and non-active currents for three-phase four-wire systems, including the algorithm to regulate the dc-link voltages, are presented in Section III. In Section IV are presented simulation and experimental results of the shunt active filter. Finally, conclusions and suggestions for further works are presented in Section V.

II. SYSTEM CONFIGURATION

As mentioned in section I and illustrated in Fig. 1, the shunt active filter is composed by a power-converter connected in parallel with the power grid (shunt converter). A 10 kVA step-down (Δ-Y) transformer (230 V//115 V) is used to connect the load and the shunt active filter with the power grid.

The implemented shunt converter is composed by three branches (6 IGBTs) from model Mitsubishi PM25RSB120 [10]. This power module is designed for power switching applications operating at frequencies up to 20 kHz. The IGBTs of this power module present as main features a collector-

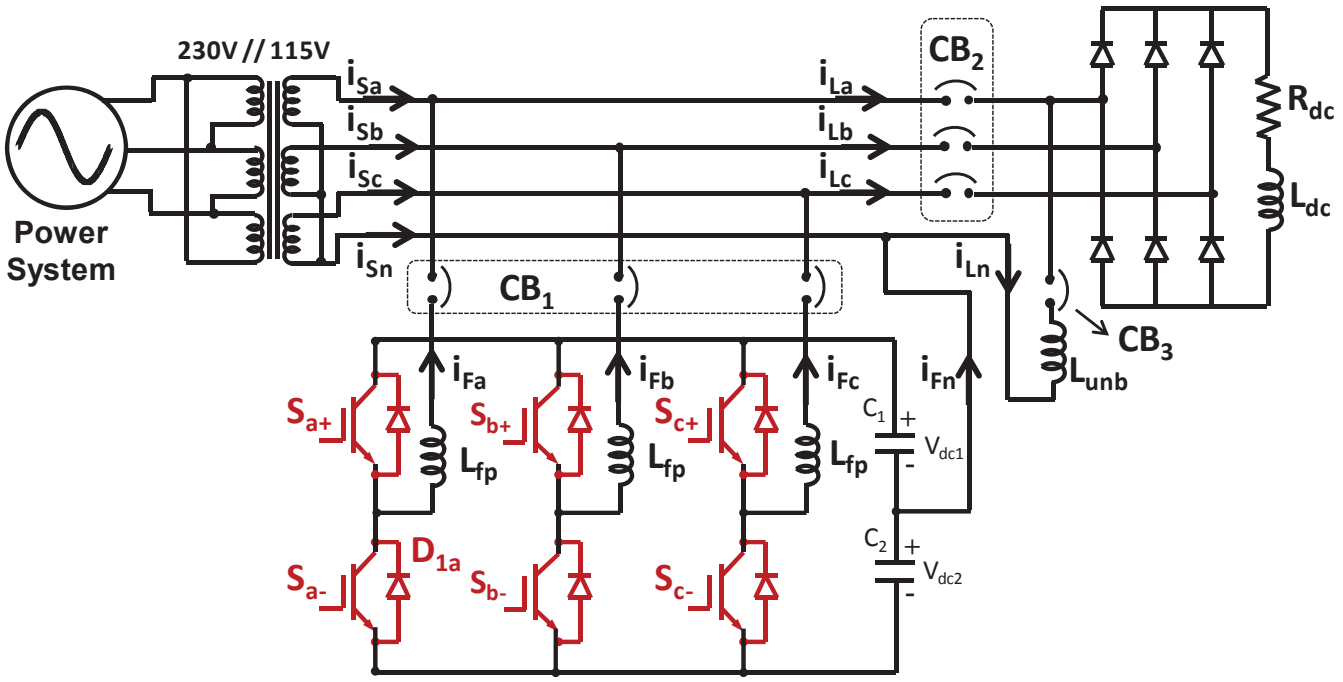

Fig. 1. Electrical diagram of the shunt active filter

emitter voltage of 1200 V, collector current of 25 A (with 50 A peak collector current), and collector dissipation of 132 W.

The dc-link is composed by two capacitors of 4700 µF connected in split. These capacitors are illustrated in Fig. 1 as C_1 and C_2, respectively. The shunt converter is connected to the power grid through iron-core inductances (represented in Fig. 1 as L_{fp}) of 5 mH.

The load is composed by a three-phase diode bridge rectifier, with a RL load in the dc-link, plus an inductance (L_{unb} in Fig. 1) connected between phase "a" to the neutral wire. The RL load of the dc-link is represented in Fig. 1 as R_{dc} (35 Ω) and L_{dc} (5 mH), respectively. The inductance L_{unb}, connected between phase "a" to the neutral wire, is equal to 62.5 mH.

According to Fig. 1, i_{La}, i_{Lb}, i_{Lc} represents the load currents, i_{Sa}, i_{Sb}, i_{Sc} the supply currents, v_{Sa}, v_{Sb}, v_{Sc} the system voltages, v_{dc1}, v_{dc2} the inverter dc-link voltages, and i_{Fa}, i_{Fb}, i_{Fc} the currents produced by the inverter.

Finally, circuit breakers (CB_1, CB_2, and CB_3) are employed to connect the shunt active filter and the load with the power grid. As observed in Fig. 1 the circuit breaker CB_1 connects the shunt conditioner, and the circuit breakers CB_2, CB_3 connect the load.

III. Control System

As introduced in section I the control system is constituted by control algorithms to determine the reference currents to be synthesized by the inverter, to control the dc-link voltage, plus a switching algorithm to command the IGBTs.

The conductance G determined in Fig. 2 corresponds to the active currents of the load. In other words, it comprises all current components that can only produce active power with the fundamental positive-sequence components of the system voltages v_{Sa}, v_{Sb}, v_{Sc}. A low-pass filter (pseudo moving average filter) is used to extract the average value of G, denominated as G_{bar}.

Since the control signals generated by a Digital PLL [6] (pll_a, pll_b, pll_c) are synchronized with the fundamental positive sequence of the system voltages, it is possible to assure that G_{bar} must correspond to the active portion of the fundamental positive-sequence component of the load current.

The control signal $G_{control}$ is the sum of G_{bar} and G_{loss}, which, together with the control signals pll_a, pll_b, pll_c, are used to determine the active component of the load currents (i_{wa}, i_{wb}, i_{wc}) as illustrated in equation (1).

$$\begin{cases} i_{wa} = G_{control\_a} \cdot pll_a \\ i_{wb} = G_{control\_b} \cdot pll_b \\ i_{wc} = G_{control\_c} \cdot pll_c \end{cases} \quad (1)$$

These control signals are pure sinusoidal waves in phase with pll_a, pll_b, pll_c, and include the magnitude of the positive-sequence load current (proportional to G_{bar}), plus the active current (proportional to G_{loss}) that is necessary to compensate

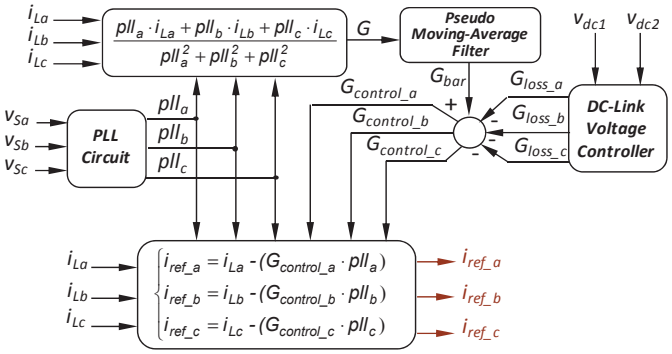

Fig. 2. Control algorithm to determine the reference currents

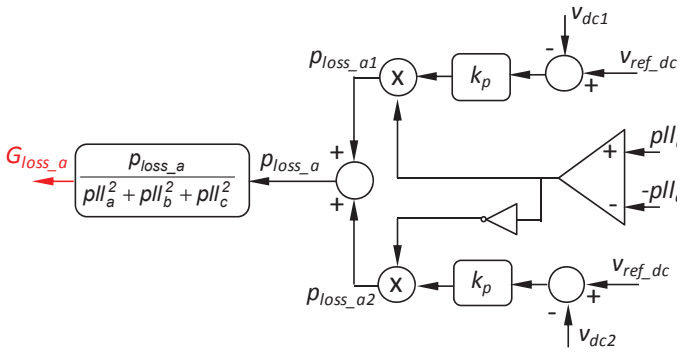

Fig. 3. DC-link voltage algorithm used to generate the signal G_{loss_a}

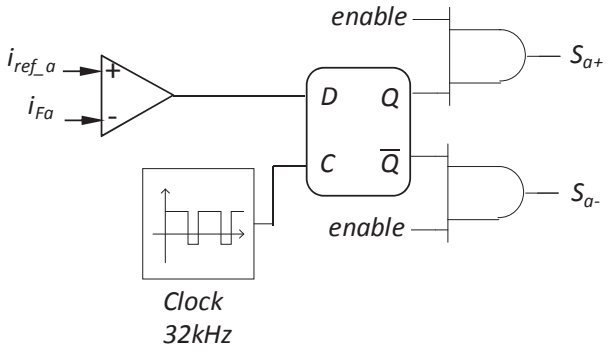

Fig. 4. Periodic-sampling switching technique

for losses in the shunt active filter.

The dc-link voltage algorithm is used to generate a control signal G_{loss}, as shown in Fig. 3. Each one of the reference currents presents their own control signal as illustrated in equation (2). The signals G_{loss_a}, G_{loss_b}, G_{loss_c} force the shunt active filter to draw additional active current from the network, to compensate losses of the shunt active filter. Additionally, it corrects dc voltage variations caused by abnormal operation and transient compensation errors.

$$\begin{cases} G_{control\_a} = G_{bar} - G_{loss\_a} \\ G_{control\_b} = G_{bar} - G_{loss\_b} \\ G_{control\_c} = G_{bar} - G_{loss\_c} \end{cases} \quad (2)$$

The fact that each one of the reference currents present their own control signal ($G_{control}$) makes this control algorithm different from those introduced in [3] [4]. Such aspect was necessary since the voltage-balancing algorithm generates the output signals (G_{loss_a}, G_{loss_b}, G_{loss_c}) as showed in Fig. 3 and in equation (2).

For example, taking Fig. 3 as basis, when the control signal pll_a is positive, the control signal G_{loss_a} carries information related to the capacitor C_1. On the other hand when pll_a is negative, the control signal G_{loss_a} carries information related to the capacitor C_2. The same principle is applied to obtain the control signals G_{loss_b}, G_{loss_c}.

Still observing Fig. 3, when the electrical system is disturbed (by a connection of an unbalanced load, for example) the signals illustrated in Fig. 3 (p_{loss_a1}, p_{loss_a2}) present different magnitudes. As a consequence, the signal G_{loss_a} presents different magnitude at positive-and negative half-cycles, and the reference current i_{Ref_a} contains a dc-component that forces an exchange of energy directed to balance the dc-link voltages.

The applied switching technique is denominated periodic sampling [11]. It is a well known technique, with reasonable results, and it is very simple to be digitally implemented. In Fig. 4 is illustrated its block diagram.

Basically, when the error involving the reference current (i_{ref_a}) and the inverter current (i_{Fa}) is positive, means that i_{Fa} have to be increased. Thus the upper IGBT (S_{a+}) is switched from OFF to the ON state. In the same way when the error involving the reference current (i_{ref_a}) and the inverter current (i_{Fa}) is negative, means that i_{Fa} have to be decreased. Thus the lower IGBT (S_{a-}) is switched from ON to the OFF state. Since the sampling period is fixed in 32 kHz, the switching frequency presents a maximum value of 16 kHz.

With a maximum switching frequency of 16 kHz, the power inverter presents an average switching-frequency equal to 10 kHz, approximately. This characteristic makes the power inverter capable to generate currents up to 15th harmonic.

Unfortunately, to force the power inverter operate with a maximum switching frequency over than 16 kHz, would result in an increased power losses of the inverter and more computational effort of the micro controller. Such aspects would make the active filter impracticable to be implemented.

IV. Simulation and Experimental Results

With the objective to analyze the performance of the shunt active filter, in this topic are illustrated simulation and experimental results.

The simulated system, implemented in the electromagnetic transient program PSCAD®/EMTDC™ 4.2, presents a simulation time of 1.5 s, with a fixed time step of 5 µs.

The system line voltages present a RMS value of about 115 V, including 5 % of 5th harmonic (negative-sequence). These conditions, together with the harmonic content of the load currents, that also contributes to increase the voltage distortion, result in a source voltage THD equal to 6.5 %.

The load currents i_{La}, i_{Lb}, i_{Lc} and the neutral current i_{Ln} are illustrated in Fig. 5. Initially only the diode bridge rectifier is connected to the system. At 0.25 s CB_3 is closed and the unbalanced load is also connected, which results in a neutral current as it can be observed in Fig. 5.

The system currents i_{Sa}, i_{Sb}, i_{Sc} are illustrated in Fig. 6 and in Fig. 7. In Fig. 6 it can be observed the system currents when the shunt active filter turns on with the load constituted by the diode bridge rectifier only.

When the shunt active filter is turned on, the amplitude of the system currents is increased since the dc-link capacitors present their values lower than the reference voltage of 200 V. The amplitude of the system currents decreases just as the error between the dc-link voltages and the reference voltage also decreases.

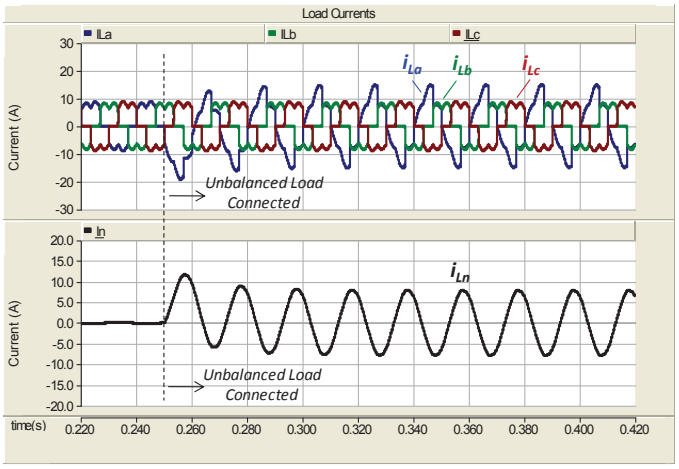

Fig. 5. Load currents when the unbalanced load is connected

Fig. 7 illustrates the system currents when the unbalanced load is connected to the system. When the unbalanced load is connected, a small unbalance is observed at the system currents. However this unbalance is minimized after 100 ms approximately.

In Fig. 8 and Fig. 9 are shown the dc-link voltages. In Fig. 8 is presented the time period in which the shunt active filter is turned on (150 ms) and the unbalanced load is connected to the system (250 ms). When the active filter starts the dc-link voltages have their amplitudes increased from 150 V to 200 V

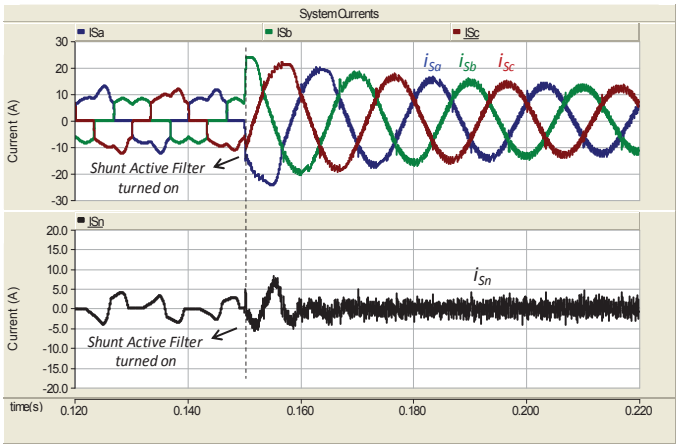

Fig. 6. System currents when the shunt active filter is turned on

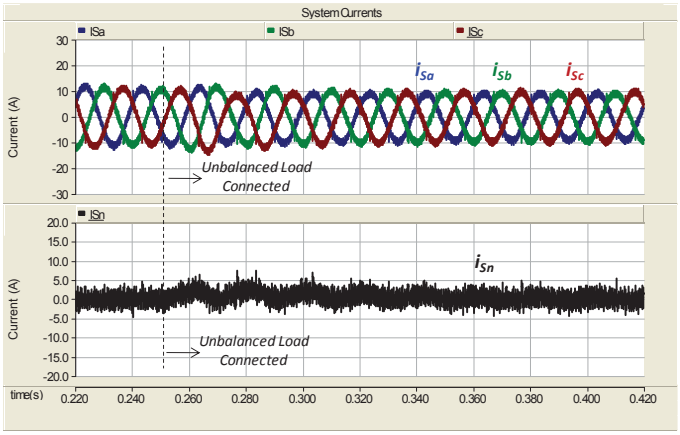

Fig. 7. System currents when the unbalanced load is connected

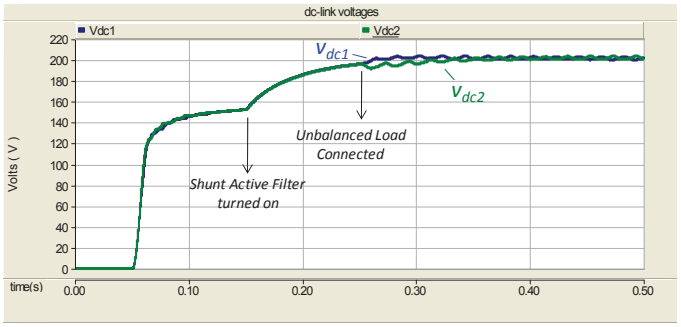

Fig. 8. DC-link voltages when the shunt active filter is turned on and the unbalanced load is connected

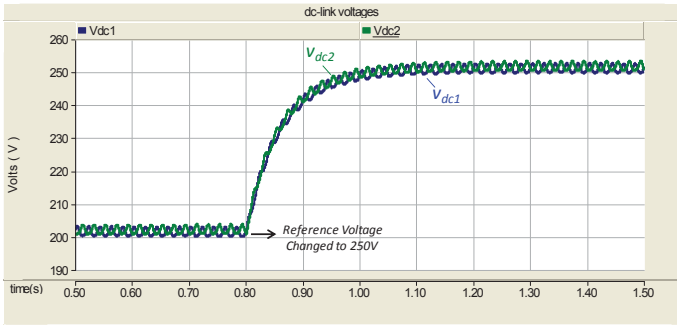

Fig. 9. DC-link voltages when the reference value is changed from 200 V to 250 V

in 100 ms approximately. When the unbalanced load is connected it can be seen the dc-link voltages with an unbalance plus an oscillating component. After 150 ms this unbalanced is minimized, with a small steady-state error (close to 2 V).

A new transient is observed at 800 ms (Fig. 9) when the dc-link voltages have their reference value increased from 200 V to 250 V. After 300 ms the dc-link voltages reaches the new reference value. A small steady-state error, close to 2 V, still remains. This error is expected since the dc-link voltage controller (illustrated in Fig. 3) does not have PI controllers.

In Table I are illustrated the Total Harmonic Distortion (THD) and the RMS values of the load and system currents, with the shunt active filter operating under steady-state condition. The neutral current (i_{Sn}) presents its RMS reduced from 5.67 A to 1.3 A (a reduction of 77% approximately). Since the algorithm to regulate the dc-link voltages does not have PI controllers, it is not possible to reach zero error, in steady state condition. Such effect results in a loss of capacity of the shunt active filter to compensate the total neutral current consumed by the load.

Next are illustrated the experimental results from a laboratorial prototype of the implemented shunt active filter.

TABLE I
THD AND RMS VALUES OF THE LOAD- AND SYSTEM CURRENTS
SIMULATION RESULTS

Phase "a"	i_{La}	THD = 19%	RMS = 9.4 A
	i_{Sa}	THD = 6.8%	RMS = 6.42 A
Phase "b"	i_{Lb}	THD = 32%	RMS = 6.5 A
	i_{Sb}	THD = 6.1%	RMS = 6.4 A
Phase "c"	i_{Lc}	THD = 28.7%	RMS = 6.5 A
	i_{Sc}	THD = 5.3%	RMS = 6.9 A

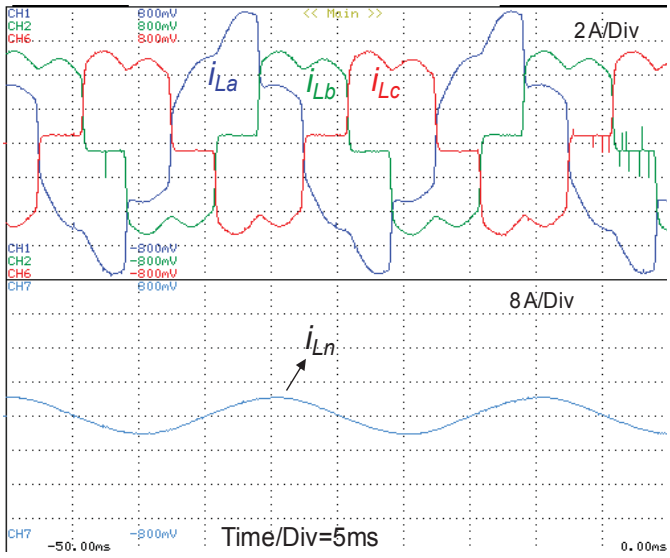

Fig. 10. Load Currents with the unbalanced load connected

In Fig. 10 are shown the load currents i_{La}, i_{Lb}, i_{Lc} and the neutral current i_{Ln}. A test case implemented experimentally is different of those observed in the simulation results. In this case the unbalanced load is connected before the shunt active filter is turned on.

The system currents i_{Sa}, i_{Sb}, i_{Sc} and the neutral current i_{Sn} are illustrated in Fig. 11 and in Fig. 12. In Fig. 11 it can be observed the system currents when the shunt active filter is turned on with the load constituted by the diode bridge rectifier together with the unbalancing inductance. This test conditions is harder than the one set for the simulation test (Fig. 6 and Fig. 7).

Once the shunt active filter turns on the harmonic and unbalanced components in the system currents are minimized. As already noted in the simulation results, the amplitude of the system currents is increased as the shunt active filter consumes an average active power to charge the dc-link capacitors up to the reference value of 200 V. After 120 ms, the amplitude of the system currents stop increasing as the dc-link voltages reaches the reference voltage of 200 V.

In Fig. 12 are presented the system currents with the shunt active filter operating under steady-state condition. A small unbalance is observed with the neutral current presenting an RMS value of 1.5 A, approximately.

In Fig. 13 and Fig. 14 are shown the dc-link voltages. Fig. 13 shows the transient when the shunt active filter is turned on. When the active filter starts the dc-link voltages have their amplitudes increased from 150 V to 200 V in 120 ms approximately. It can be seen in the dc-link voltages an unbalance plus an oscillating component due to the presence of an unbalanced load.

In Fig. 14 is presented the dc-link voltages with the shunt active filter operating under steady-state condition. A small unbalance (close to 3 V) is observed since the algorithm to regulate the dc-link voltages does not have PI controllers.

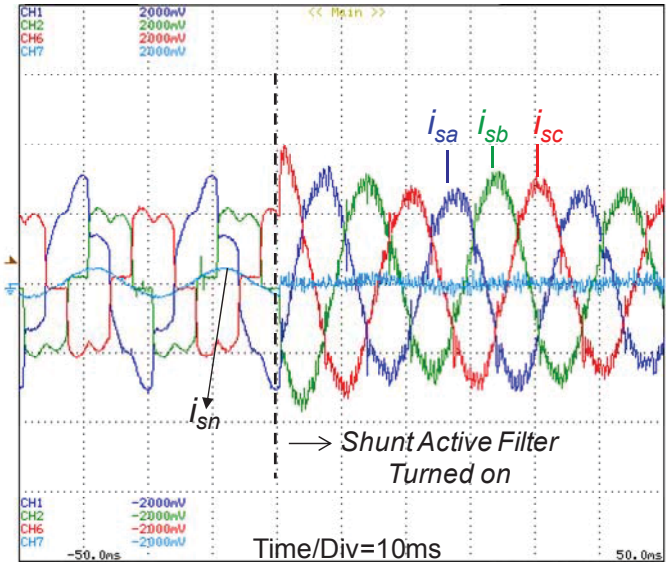

Fig. 11. Experimental results of the system currents when the shunt active filter is turned on

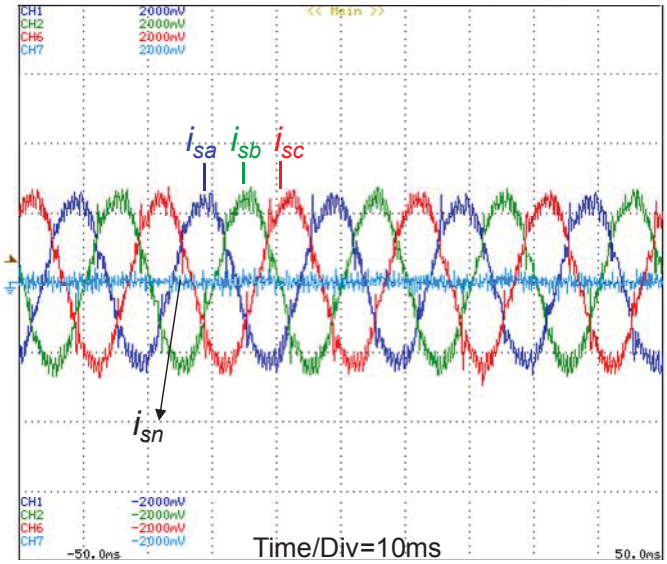

Fig. 12. Experimental results of the system currents with the shunt active filter operating under steady-state condition

Finally, in Table II are illustrated the Total Harmonic Distortion (THD) and the RMS values of the load- and system currents, based on the experimental results of the shunt active filter operating under steady-state condition. The neutral current (i_{Sn}) presents its RMS reduced from 5.01 A to 1.5 A (a reduction of 71% approximately).

As observed in simulation results, the shunt active filter could not compensate the total neutral current consumed by the load. Such aspect results from the fact that the algorithm to regulate the dc-link voltages does not have PI controllers.

V. Conclusions and Further Work Suggestions

A control system for a three-phase four-wire shunt active filter, with a split-capacitor inverter topology, is proposed in this work. Simulation and experimental results have validated

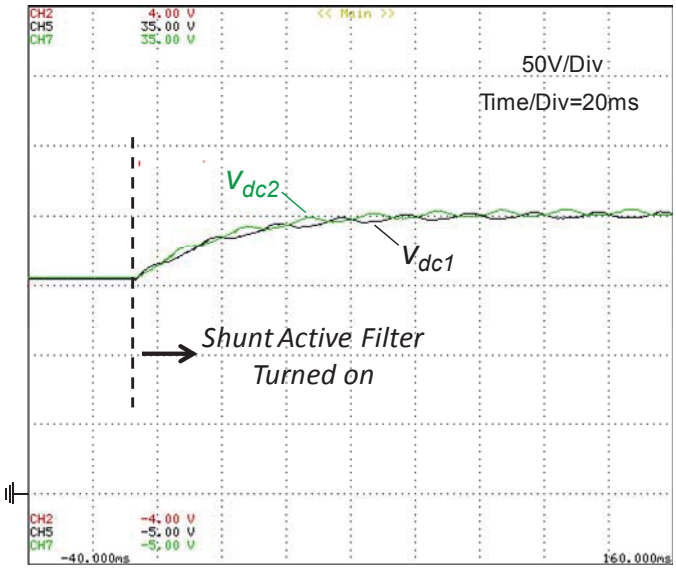

Fig. 13. Experimental results of the dc-link voltages when in which the shunt active filter is turned on

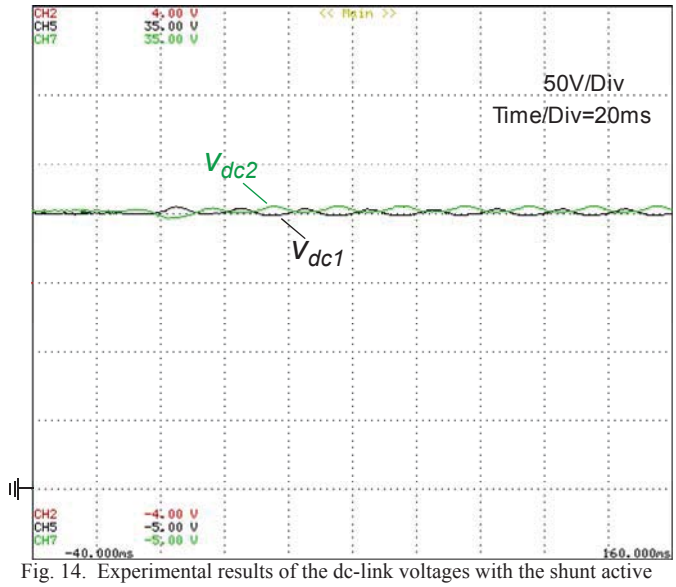

Fig. 14. Experimental results of the dc-link voltages with the shunt active filter operating under steady-state condition.

the algorithms to determine the reference currents and to regulate the dc-link voltages.

The obtained simulation and experimental results shows a good performance of this active filter, with the control strategies introduced in this work. However further tests under different conditions are needed, in order to more deeply investigate the behavior of the shunt active filter with the introduced control strategies. These test cases should include a system with a higher power-level, unbalanced or distorted voltages, and more transient situations (more loads to be connect to the power system), and other aspects.

The proposed algorithm to regulate the dc-link voltages presents a good performance since the observed unbalance, in simulation and experimental results, is very small (close to 1% in comparison with the reference voltages). The time period to reach a steady-state condition depends, directly, on the size of the capacitors and on the applied proportional gain.

A negative aspect is concerned with the fact that the neutral current could not be totally compensated. This problem can be overcome when the proportional controller is replaced by a PI controller.

TABLE II
THD AND RMS VALUES OF THE LOAD- AND SYSTEM CURRENTS
EXPERIMENTAL RESULTS

Phase "a"	i_{La}	THD = 22.5%	RMS = 7.9 A
	i_{Sa}	THD = 8.8%	RMS = 6.1 A
Phase "b"	i_{Lb}	THD = 28.6 %	RMS = 5.5 A
	i_{Sb}	THD = 6.3%	RMS = 6.5 A
Phase "c"	i_{Lc}	THD = 28.7%	RMS = 5.6 A
	i_{Sc}	THD = 7.3%	RMS = 6.4 A

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