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System-Level Measurement-Based Design Optimization by Space Mapping Technology

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***Abstract*—Space mapping arose from the need to implement fast and accurate design optimization of microwave structures using full-wave EM simulators. Space mapping optimization later proved effective in disciplines well beyond RF and microwave engineering. The underlying coarse and fine models of the optimized structures have been implemented using a variety of EDA tools. More recently, measurement-based physical platforms have also been employed as "fine models." Most space-mapping-based optimization cases have been demonstrated at the device-, component-, or circuit-level. However, the application of space mapping to high-fidelity system-level design optimization is just emerging. Optimizing highly accurate systems based on physical measurements is particularly challenging, since they are typically subject to statistical fluctuations and varying operating or environmental conditions. Here, we illustrate emerging demonstrations of space mapping system-level measurement-based design optimization in the area of signal integrity for high-speed computer platforms. Other measurement-based space mapping cases are also considered. Unresolved challenges are highlighted and potential general solutions are ventured.**

***Keywords*—Bayesian, Broyden, design automation, Kriging, machine learning, optimization, post-fabrication tuning, post-silicon validation, space mapping, surrogate modeling.**

I. Introduction

Space mapping (SM) is a well-established numerical approach specialized for the efficient modeling and design optimization of computationally expensive models [1], [2], also referred to as fine models. Although it started in the microwave engineering arena [3], SM optimization has found applications in a plethora of diverse disciplines [4]. Optimized fine models by space mapping have been implemented using a variety of commercially available EDA systems and internal CAD tools [4]. The great majority of design optimization cases solved by space mapping methods have been implemented at the device-, component-, or circuit-level [5].

In a recently observed trend [5], space mapping is now being extended to the design optimization of non-numerical "fine models" consisting of high-fidelity measurement-based physical platforms with adjustable design or tuning parameters. This is of great industrial relevance when each physical measurement, typically implemented at a system level, is either too long or too expensive, or both, such that applying classical optimization approaches are prohibitive given the large number of measurements implied.

A number of inherent challenges are typically associated with the problem of optimizing highly accurate systems based on complex and time-consuming physical measurements. In contrast to numerical fine models whose nominal responses are consistently reproduced each time the model is evaluated, measurement-based "fine model" responses are typically subject to statistical fluctuations caused by both measurement instrumentation variability and manufacturing variability. Additionally, measurement-based "fine model responses" can be significantly affected by operating conditions (biasing voltages, loading conditions, maximum data rates, etc.) as well as by environmental conditions (temperature, humidity, etc.)

Another challenge for optimizing highly accurate systems based on physical measurements is the typical lack for computationally efficient physics-based coarse models, such as circuit-level equivalents, macromodels, etc. This deficiency generally leads to the need to employ machine learning techniques to develop suitable coarse model surrogates to make space mapping feasible.

Emerging and preliminary demonstrations of space mapping as applied to system-level measurement-based design optimization are briefly described in this paper. These examples have been implemented in the area of signal integrity for high-speed computer servers, using actual industrial validation platforms. Additional measurement-based SM optimization cases on waveguide filters are briefly described. Based on these initial demonstrations, we attempt to make a general characterization of this problematic situation, emphasizing associated unresolved challenges as well as some potential general solutions yet to be explored and developed.

II. Post-Silicon Electrical Validation of High-Speed Computer Platforms

Post-silicon electrical validation (EV) of modern computer platforms focuses on testing electrical and EM performance of microprocessor circuitry in a system environment. This includes validating high-speed input/output (HSIO) links, phase-locked loops (PLLs), analog/mixed-signal circuitry, clock networks, and power delivery networks (PDN), among others. The largest portion of post-silicon EV is devoted to validating HSIO links [6].

Given the large die-to-die process variations in nanometric technologies, along with the typical variation in operating conditions, board impedance, channel loss, and different add-in cards, the performance of HSIO links can exhibit large fluctuations. Additionally, undesired EM effects such as jitter, inter-symbol interference (ISI), crosstalk, and others, can create

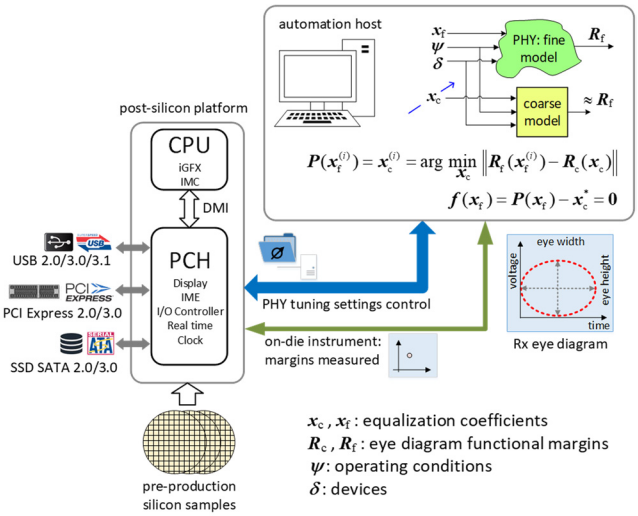

Fig. 1. Optimizing equalization coefficients of high-speed input/output links in a computer platform to maximize eye diagram functional margins under varying operating conditions (e.g. voltage, temperature) and devices (e.g. silicon skew, external devices). From [5].

multiple signal integrity problems in HSIO links, limiting the maximum data rates. This is relevant for modern industrial HSIO interfaces, such as Peripheral Component Interconnect Express (PCIe), Serial Advanced Technology Attachment (SATA), Universal Serial Bus (USB), and Ethernet.

Several tuning coefficients, embedded in the HSIO links, can be digitally adjusted to compensate for undesired effects and reduce various fluctuations. The so called "physical layer (PHY) tuning process" of HSIO links in post-silicon EV of high-performance computer servers consists of finding the "optimal" configuration of PHY tuning coefficients; it is the most time-consuming processes in industrial post-silicon validation [7]. Interestingly, this challenge can be addressed from a CAD-EDA perspective [8].

The above system-level measurement-based design optimization challenge is addressed by space mapping technology in [9], [10]. In that work, the optimal equalization (EQ) coefficients of a high-performance computer platform are efficiently obtained by adapting the Broyden-based input SM approach [11] to maximize the receiver eye diagram functional margins.

The block diagram in Fig. 1 illustrates the approach followed in [9]. The "fine" model is an Intel server post-silicon industrial validation platform shown in Fig. 2 [10]. The fine model response $\boldsymbol{R}_f$ contains the measured eye width margin e_w and eye height margin e_h. $\boldsymbol{R}_f$ depends on the PHY tuning settings $\boldsymbol{x}$ (SATA Gen 3 receiver equalization coefficients), the operating conditions $\boldsymbol{\psi}$ (voltage and temperature), and the devices $\boldsymbol{\delta}$ (silicon skew and external devices), i.e., $\boldsymbol{R}_f = \boldsymbol{R}_f(\boldsymbol{x},\boldsymbol{\psi},\boldsymbol{\delta})$. The coarse model response $\boldsymbol{R}_c$ approximates the same functional margins. Since no analytical, empirical, circuit, or CAD-tool approximation is available for this "fine model," the coarse model is developed following a Kriging surrogate modeling technique [12] from only 50 measurements using a Sobol [13] low-discrepancy [14] design of experiments (DoE) approach. However, other metamodeling approaches have been

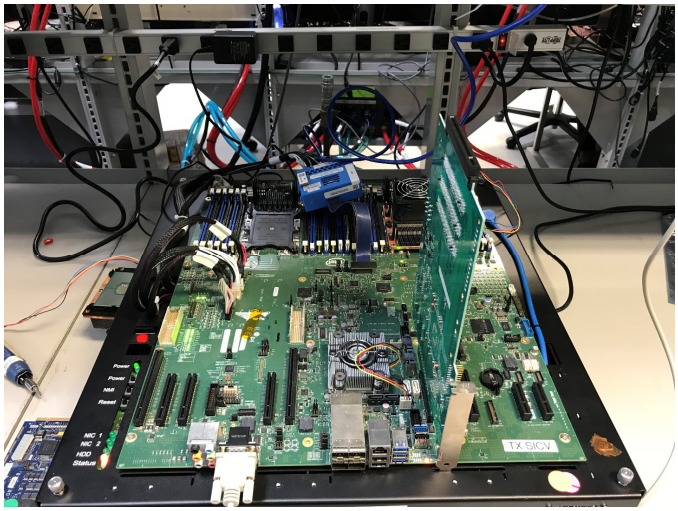

Fig. 2. Intel's post-silicon validation platform used in Fig. 1. From [10].

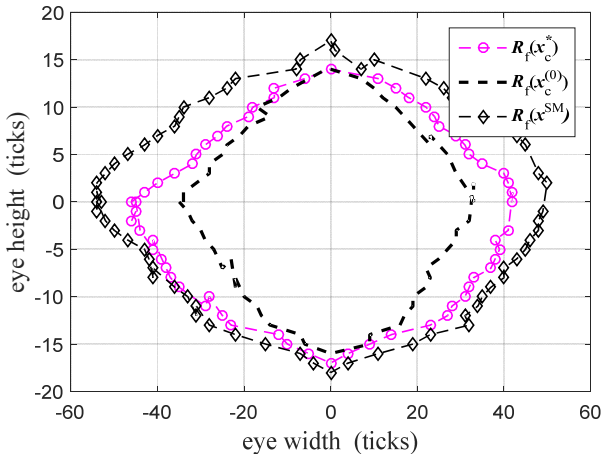

Fig. 3. Eye diagram functional margins of the high-performance computer platform used in Fig 2, evaluated at the initial equalization (EQ) settings, $\boldsymbol{x}_c^{(0)}$, at the optimal coarse model EQ settings, $\boldsymbol{x}_c^*$, and at the SM solution found, $\boldsymbol{x}^{SM}$. From [9].

used for developing coarse models for these kinds of physical platforms [15].

A space-mapped solution, $\boldsymbol{x}^{SM}$, is obtained in just 6 iterations (or fine model evaluations) of the Broyden-based input SM [9]. As seen in Fig. 3, the solution found makes an improvement of 85% on the fine model eye diagram margins area as compared to that one with the initial settings ($\boldsymbol{x}_c^{(0)}$, obtained from engineers' empirical knowledge), and a 33% improvement as compared to that one with the optimal coarse model solution ($\boldsymbol{x}_c^*$). The traditional industrial PHY tuning process, based on exhaustive enumeration practices, requires days for a complete empirical "optimization," while the proposed SM method can be completed in a few hours.

III. Other Measurement-Based Space Mapping Optimization Cases

Complex waveguide filters and multiplexers have been optimized by considering that each manufactured and measured prototype corresponds to a "fine model evaluation," while the coarse model is implemented in a full-wave EM simulator. That

is the case in [16]-[18], where SM is used to correct the typical manufacturing deviations in waveguide components, avoiding tuning elements and the problematic tuning process [19].

Accelerating the filter tuning process is possible by incorporating a computer-controlled robot to automatically adjust the tuning elements. Several tuning methods for waveguide filters with robotic tuner based on different variations of input SM are proposed in [20], where each "fine model response" is a VNA measurement for a given set of tuning parameter values, while the coarse model is implemented as a full-wave EM model with varying fidelity levels.

An alternative approach for surrogate-based post-fabricated filter tuning is in [21], where the surrogate model consists of a convex combination of an implicit space mapped equivalent distributed circuit and a first-order Taylor approximation. Optimal tuning parameter values are efficiently obtained in [21] for waveguide filters (turns in screws) and microstrip filters (DC voltages in varactors).

IV. Main Challenges and Potential Developments

The complexity, uncertainty, and variability of measured responses increases as we move from the component-, to circuit-, to system-levels. It makes sense using SM technology as long as the coarse model is much faster or cheaper than the "fine model," On the other hand, it is well-known that the parameter extraction (PE) subprocess can make SM to diverge or oscillate when non-unique solutions exists for PE [22], [23]. In the study case presented in Section II, it is explicit that the "fine model response" is not fully deterministic and depends on other variables ($\boldsymbol{\psi}$ and $\boldsymbol{\delta}$) besides the design parameters ($\boldsymbol{x}$). This was not an obstacle for SM to work, and PE was successfully implemented. This particular behavior needs more research; however, it might have been caused by the fact that the coarse model is a Kriging surrogate obtained from the same physical platform, capturing a similar stochastic relationship with $\boldsymbol{\psi}$ and $\boldsymbol{\delta}$ as that one of the fine model. This might be an indication that Bayesian metamodeling would be a suitable approach to develop inexpensive coarse models of system-level measurement-based "fine models," given its adequacy to deal with stochastic or noise-corrupted responses [24].

V. Conclusion

In this paper we briefly described emerging applications of space mapping for measurement-driven design optimization, emphasizing system-level applications in the area of electrical validation for high-speed computer platforms. We identified general associated challenges as well as potential solutions.

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