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Adaptable On-Board Computer for Nanosatellites

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Adaptable On-Board Computer for Nanosatellites

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***Abstract*— Nowadays, nanosatellite missions require a development process for the on-board computer (OBC). This process can be optimized using a unique hardware design for different applications. This paper presents the design, implementation and test of a reconfigurable OBC for nanosatellite applications. Reconfigurability is based on ZYNQ architecture that allows an iterative hardware/software co-design approach. The implementation showed an acceptable compatibility with different applications which lead to a successful integration with a custom payload subsystem. These integrated subsystems along with projects from several universities will perform a test flight on August 2022 in the mission FY22 Fort Sumner Campaign sponsored by NASA. In addition, this work can be seen as an open platform to swiftly develop further subsystem implementations.**

Keywords*— *On-Board Computer (OBC), nanosatellite, CubeSat, ZYNQ, Field Programable Gate Array (FPGA), codesign.

I. INTRODUCTION

Over the last years, nanosatellites have proven to be a turning point for aerospace technology. Contrary to traditional satellite systems, nanosatellites have a faster development cycle and a lower cost [1]. Nanosatellite market projections as reported by [2] have reinforced the interest of the private and academic sectors to enhance their own technologies. As a result, the development of aerospace projects by universities has provided an opportunity to test and validate suborbital designs. Nonetheless, the actual design paradigm for the electronics industry and its application in the aerospace sector focuses on generating devices with short useful life cycles coupled with high environmental costs [3].

Currently, several proposals [4], [5] suggest the use of reconfigurable technology to reduce costs during the project's design phase. Additionally, this approach reduces manufacturing pollution significantly by having products that last longer before becoming obsolete. Also, national universities address the use of field programmable gate arrays (FPGAs) on special environments. The Western Institute of Technology and Higher Education (ITESO) is one of the universities that are driving this change by proposing the ITESO Satellite (ITESAT) project. ITESAT is intended to be a nanosatellite that follows the sustainable development paradigm. There are five phases that compose this project: (1) on board computer (OBC), (2) attitude determination and control system (ADCS), (3) telemetry, (4) thermic control, and (5) payload.

In this work, a hardware (HW)/software (SW) codesign approach is used to develop an OBC for a CubeSat type nanosatellite using a ZYNQ System on a Chip as the basis of operation. After the first conceptual design is performed, the OBC is implemented as a printed circuit board (PCB) for it to be interfaced with a basic payload subsystem. Then, a codesign iteration is executed to test its adaptation capabilities.

This paper is organized as follows: Section II, the proposed system is described. Section III, describes the results of the reconfiguration tests. Section IV, presents the conclusions and future work.

II. PLATFORM DESIGN

Initially, the design flow defines the precepts that will guide the design, action that allows the definition of a base framework in which the codesign procedure can take place. "Fig. 1" shows a brief description of the followed design flow based and adapted on the proposal by [6].

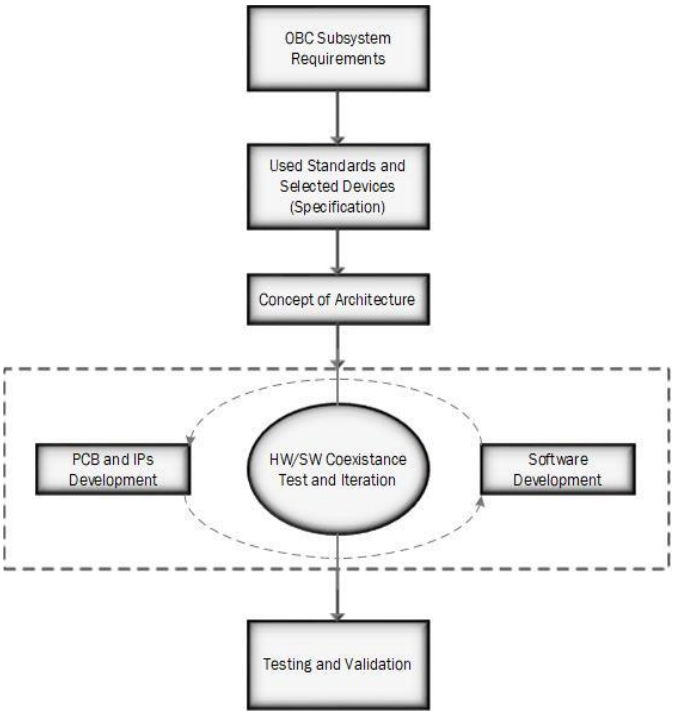


Fig. 1. OBC's design flow.

A. *Subsystem requirements*

The following listed requirements are used to define the OBC's base features and guide the design development.
REQ_1: The OBC shall be able to communicate with at least five other subsystems.
REQ_2: The OBC shall be able to implement new logic devices without adding external components.
REQ_3: The OBC must be connector compatible with other subsystems.
REQ_4: The OBC must be dimensionally compatible with other subsystems.
REQ_5 The OBC must be able to store up to 16 Bytes of information.
REQ_6 The OBC must be able to communicate through UART.
REQ_7 The OBC must be able to communicate through SPI.
REQ_8 The OBC must be able to communicate through I2C.
REQ_9 The OBC must be able to communicate through CAN.
REQ_10 The OBC must be capable of re-routing its pins internally (No external hardware addition).
REQ_11 The OBC shall not surpass X a in consumption.
REQ_12 The OBC shall be power supplied with 5v.
REQ_13 The OBC's operative temperature range must be ….
REQ_14 The OBC must be capable of surviving XXX vibration test.
REQ_15 The OBC must be able to be reconfigured to implement a new application and mission without changing its PCB hardware.

B. *Platform selection and standards*

The PC/104 specification is an electrical and mechanical standard for PCB design and is used primarily by the CubeSat industry/community. The PC/104 boards are meant to be stacked on top of each other, forming a rigid structure. The 104 pin headers provide an electrical connection between the individual boards, creating one electrical system [7] shown in "Fig. 2".

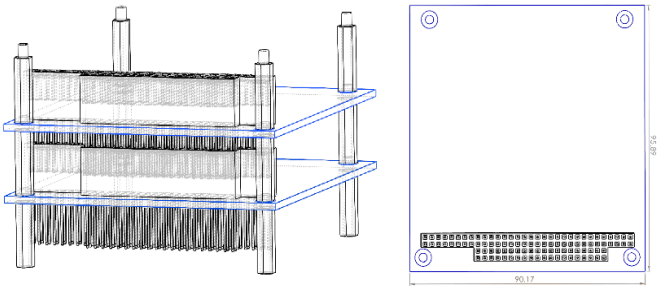


Fig. 2. OBC's PCB mechanical outline.

One of the key advantages of the PC/104 standard is flexibility to adapt board templates [8]. The template used is a PC/104 16-bit, designed in collaboration with the following universities: ITESO, National Autonomous University of Mexico (UNAM) and National Polytechnic Institute of Mexico (IPN), and it has the characteristic of incorporating reconfigurable logic inputs.

The OBC in CubeSat is the subsystem which acts as a bridge that connects the other subsystems with each other. It supervises many of the tasks that are performed by the different subsystems of the satellite, including housekeeping and monitoring to ensure the appropriate status of those subsystems. The hardware and software design of the OBC mainly depends on the mission of the CubeSat [9].

The proposed OBC architecture is based on commercial electronic components (COTS), which are often used for aerospace prototypes, therefore their design cost is lower, and validation tests are accelerated. In [10] an OBC computer was designed, and it details how COTS hardware supports satellite activities and shows how they can be used for short-term missions.

a) *Electrical configuration:* OBC requires a 5v input voltage to power XME0724 module, and a voltage of 3.3v to power banks of programmable logic (bank 34, bank 35), which are connected to the PC/104 connector and are taken from an external power supply.

b) *SoC selection:* In order to complete hardware and software specifications, a core board unit XME0724 was selected, which is a low-cost programmable system-on-chip (PSoC) designed by Microphase®, mainly used in industry for prototyping development. The characteristics and specifications of the PSoC are described below in TABLE I.

TABLE I. XME0724-10I SPECIFICATIONS

Characteristics	Specifications
FPGA Model	XC72010-1CLG4001
Logic Cells	28 k
Dddr3 ram	512mb
QSPI	256 Mbit
eMMC	8GB
I/O	IO PS 94 PL
Operating temperature	-40° C to 85° C

C. *Concept of architecture*

The implementation of the XME0724 module and the architecture ZYNQ distribution is shown in "Fig. 3". The processing system (PS) incorporates external storage in an SD memory, and it also has two pairs of CAN buses (CAN0 and CA12) and an UART (UART0). Programmable logic (PL) includes a JTAG interface, an I2C bus and twenty GPIOs wired directly to a PC-104 connector.

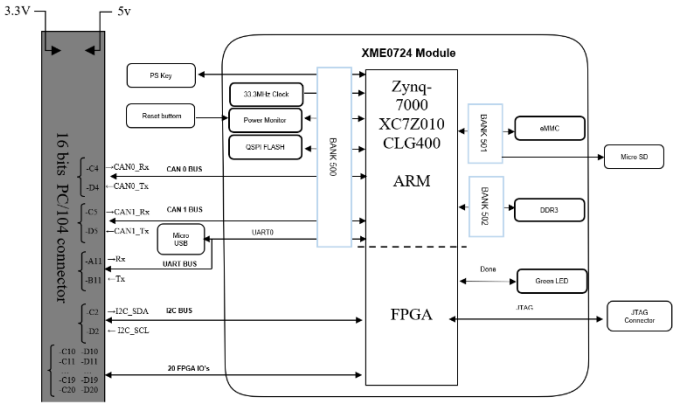


Fig. 3. OBC block diagram.

The other non-trivial function that every OBC on a satellite should perform is the management of payload (science) data [9]. The payload of this project contains the sensors described in TABLE II.

TABLE II. PAYLOAD SENSORS

Item	Description / Communication protocol
IMU	BNO055 9-DOF / I2C
GPS	GPS Neo-6 / UART
AQS	SGP40 / I2C
RTC	DS1307 / I2C
Pressure sensor	MS5803-14BA / I2C

Payload sensors were integrated in another designed PCB using PC104 standard, communication busses were wired to PC104 connector and it is the physical interface to OBC.

D. *Codesign implementation*

Developing software in a HW/SW codesign differs from the classical application-specific integrated circuit (A-SIC) approach, as the reconfigurable internal hardware needs to be implemented before the software logic development starts. In order to develop the intended codesign, the Vivado Suite Design provided by Xilinx was used. Once the hardware configuration was set and the FPGA was programmed, the software development started.

The program periodically monitors the air quality and pressure sensors, the real time clock (RTC) and the inertial measurement unit (IMU). Sensor readings are obtained once at a time (by polling) over I2C communication. Once the four sensors are read, the program saves the data of the current readings in memory. In case the memory is full, the oldest data begins to be overwritten. After the data is saved, the loop starts all over again and will continue until the device is powered off, as shown in "Fig. 4".

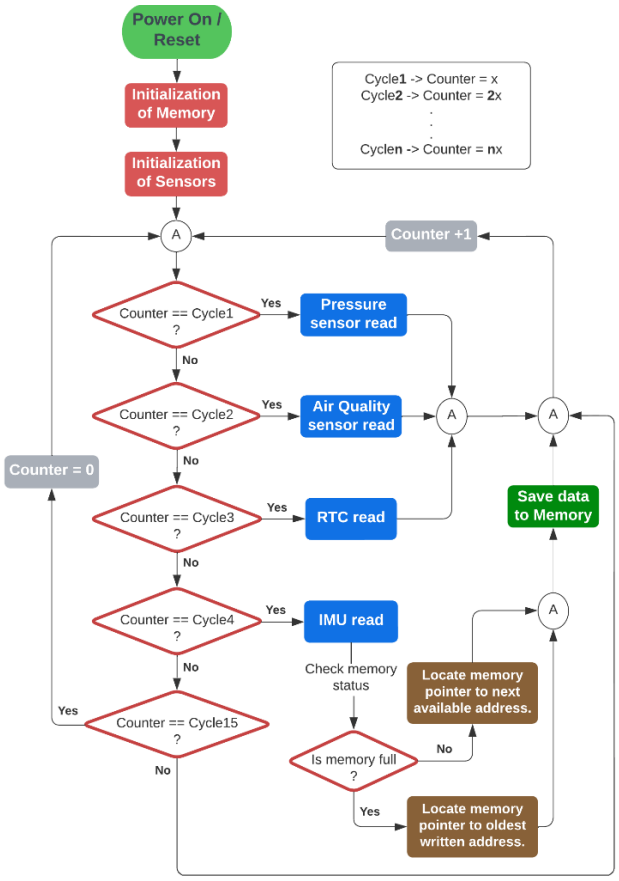


Fig. 4. Software implementation flow diagram.

At the end of the mission, data can be collected from the memory to obtain all the sensed data. That information contains the value of the absolute pressure (in millibars) and the temperature (in Celsius degrees), including CO2 (ppm) readings and total volatile organic compounds (TVOC) [ppb], the time since the last power-on from RTC, and lastly, the orientation of the device represented in Euler vector.

III. Integration and Testing Results

The hardware reconfiguration test validates that the I2C driver can be mapped to different pins over the extended multiplexed inputs/outputs (EMIOs). This is implemented in Case 1 shown in ”Fig. 5”, which should handle I2C communication properly. Afterwards, the pin package configuration of the “constraints.xdc” file should be modified to obtain Case 2 (also shown in “Fig. 5”). After every change of pin package configuration, the design must be rebuilt and the software reflashed to have the new changes in the ZYNQ. Both configurations worked properly using different pins.

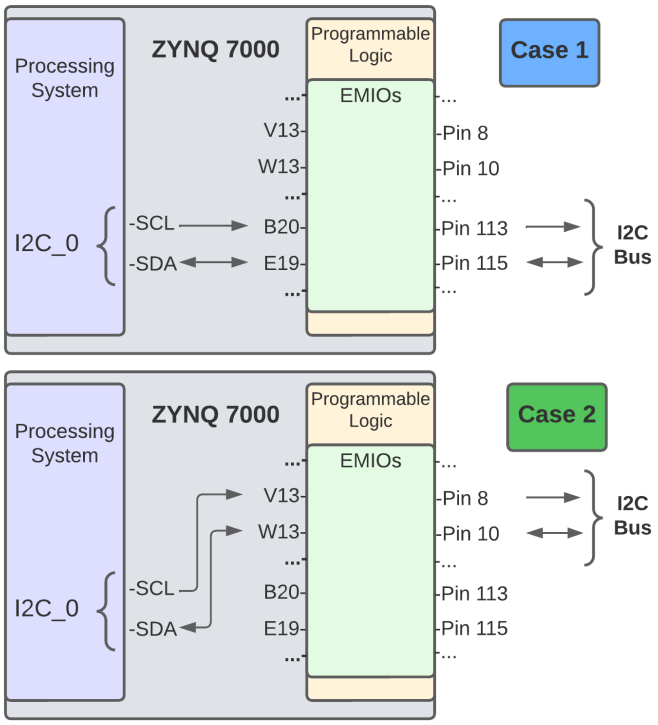


Fig. 5. EMIOs rerouting.

The developed OBC and its payload were assembled using plug-and-play scheme as it is represented in in “Fig. 6”. Aluminum spacers were placed to configure a rigid structure in M3 through hole.

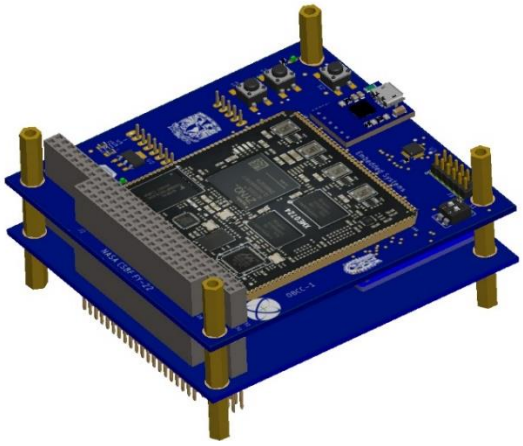
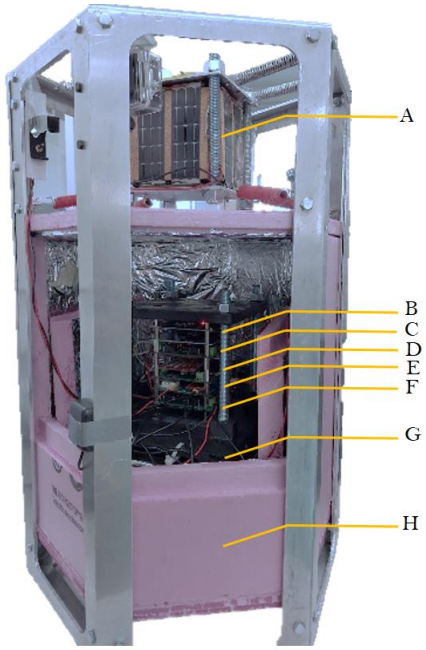


Fig. 6. Computer-aided design of the OBCC -1.

The assembled system was sent to UNAM’s laboratory to assembly in Experimental Module for Iterative Design of Satellite Subsystem version 3 (EMIDSS 3) there is a scientific/technological platform to evaluate aerospace prototyping. It has a PC/104 module adapted to add external units. “Fig. 7” shows the assigned position for the OBCC-1 and Payload-1.



A	Cubesat Submodule
B	OBCC-1
C	Payload-1
D	Principal OBC
E	Payload-2
F	LVPS module
G	Battery bank
H	Thermal protection

Fig. 7. EMIDSS distribution.

Vibration Test. A vibration test was performed on EMIDSS in the Aerospace Test Integration Laboratory from IPN including the sinusoidal and random vibration test:

a. Random vibration
   This test confirmed that EMIDSS integration structure was free of defects. No functional failures of the integrated system OBCC-1 /Payload-1 were detected.

b. Sine vibration (SV)
   This test confirmed that EMIDSS integration structure is able to resist a low-frequency launch environment (normally between 5 and 100 Hz).

After performing these tests, we can conclude that the OBCC-1/Payload-1 is capable to withstand the vibration conditions from a real launch scenario.

IV. Conclusion

The OBC hardware design prototype based on a reconfigurable device allows different hardware configurations reusing the hardware design. The electronic board described can host a wide range of applications for future suborbital missions with a positive impact on the environment, and a short development time. One of the applications for this prototype is to be a complementary OBC for the upcoming mission of the EMIDSS-3 satellite. This mission is scheduled to fly on a stratospheric balloon sponsored by NASA in August 2022.

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