ScienceDirect

Sensors and Actuators A 145–146 (2008) 75–80

ELSEVIER

A PHYSICAL

www.elsevier.com/locate/sna

On-chip array of thermoelectric Peltier microcoolers

L.M. Goncalves [a,*], J.G. Rocha [a], C. Couto [a], P. Alpuim [b], J.H. Correia [a]

[a] *University of Minho, Department of Industrial Electronics, Campus de Azurem, 4800-058 Guimaraes, Portugal*
[b] *University of Minho, Department of Physics, Campus de Azurem, 4800-058 Guimaraes, Portugal*

Received 30 June 2007; received in revised form 24 September 2007; accepted 18 October 2007
Available online 30 October 2007

Abstract

This article reports on the theoretical modelling, the finite element modelling (FEM) simulation, the fabrication process and preliminary results of the first on-chip thermoelectric microcooler array (64 pixels arranged in an 8 × 8 array), with each pixel independently controlled. This microcooler array uses co-evaporated V–VI compounds of Bi_2Te_3 and Sb_2Te_3 as thermoelectric layers, and can be fabricated using planar thin-film technology, lithography and wet etching, on top of a silicon wafer where the CMOS electronic circuits were previously made.

Keywords: Thermoelectric; Peltier; Bi_2Te_3; Telluride; Microcooler; Energy harvesting

1. Introduction

Integration of efficient solid-state thermoelectric microdevices with microelectronics is desirable for local cooling and thermoelectric microgeneration, since they can be used to stabilize the temperature of devices, decrease noise levels and increase operation speed. An array of such devices can also be used for lab-on-chip applications or energy harvesting microsystems. Despite the range of exciting applications, only few approaches to manufacture thermoelectric devices with small dimensions were reported up to now [1–4].

Due to silicon fabrication compatibility, polycrystalline SiGe alloys and polycrystalline Si are commonly used in thermopile applications. Their use in microcoolers has been attempted [5] but the performance is very low compared with that of tellurium compounds, which have been used for many years in conventional large area Peltier devices. Tellurium compounds (Bi_2Te_3 and Sb_2Te_3) are well-established room temperature thermoelectric materials and are widely employed in conventional thermoelectric generators and coolers. Different deposition techniques were tried to obtain thin-films of these materials. Thermal co-evaporation, co-sputtering, electrochemical deposition, metal-organic chemical vapour deposition and flash evaporation are some examples. Thin-films of n-type Bi_2Te_3 and p-type Sb_2Te_3 were obtained by the authors by thermal co-evaporation [6,7], with thermoelectric figure of merit (ZT) 0.84 for n-type and 0.5 for p-type. Best n-type films have Seebeck coefficient of 220–250 $\mu V\,K^{-1}$, resistivity of 10–15 $\mu\Omega\,m$, thermal conductivity $\approx 1.3\,W m^{-1}\,K^{-1}$ [8], carrier concentration $\approx 6 \times 10^{19}\,cm^{-3}$, Hall mobility from 80 to 120 $cm^{-2}\,V^{-1}\,s^{-1}$ and EDX analysis revealed a stoichiometric composition. p-Type films have Seebeck coefficient of 160–200 $\mu V\,K^{-1}$, resistivity of 10–15 $\mu\Omega\,m$, thermal conductivity $\approx 1.7\,W\,m^{-1}\,K^{-1}$ [8], carrier concentration $\approx 4 \times 10^{19}\,cm^{-3}$, Hall mobility from 120 to 170 $cm^{-2}\,V^{-1}\,s^{-1}$ and are slightly Te-rich (67–73%, measured by EDX) [6,7]. These values are similar to the best found in literature for the bulk materials [9]. Figure of merit can be calculated according to the following equation:

$$ZT = \frac{\alpha^2}{\rho\lambda} T \tag{1}$$

where α is the Seebeck coefficient, ρ the electrical resistivity, λ the thermal conductivity and T the temperature [9]. It is demonstrated that 15 °C cooling is possible to achieve at room temperature using such thin-film materials in an array of microcoolers. Böttner et al. [1,4] uses dry etching to pattern thermoelectric devices in a two wafers process. Power factors of $3 \times 10^{-3}\,W\,K^{-2}\,m^{-1}$ and $4 \times 10^{-3}\,W\,K^{-2}\,m^{-1}$ were obtained, respectively, in n-type and p-type telluride compounds. Verti-

* Corresponding author. Tel.: +351 253510190; fax: +351 253510189.
E-mail address: lgoncalves@dei.uminho.pt (L.M. Goncalves).

0924-4247/$ – see front matter © 2007 Elsevier B.V. All rights reserved.
doi:10.1016/j.sna.2007.10.062

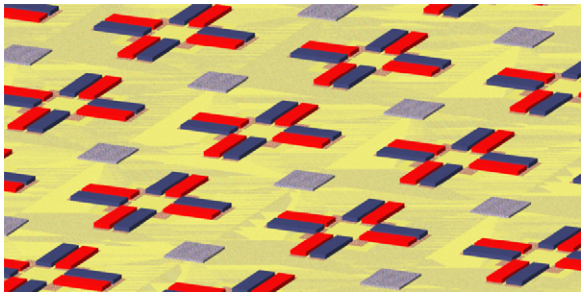

Fig. 1. Artwork showing part of the microcooler array.

cal columns of thermoelectric materials using lift-off on SU-8 photoresist, was achieved before by Silva et al. [2]. But thermoelectric properties of Bi_2Te_3 and Sb_2Te_3 films incorporated in the devices are worst than those obtained in bulk materials. A MEMS-like electrochemical process was also found in literature [3], but figure of merit obtained in materials deposited by this process is still very low. In the present work, high-figure-of-merit films are deposited by co-evaporation, and low cost wet etching techniques are used to pattern thermoelectric devices.

2. Design and simulation

The array of microcooler was designed to accommodate 64 pixels organized in 8×8 structure (Fig. 1). Each pixel can be independently controlled to heat or cool. Fig. 2 represents a single pixel cross-section. When a current flows from the n-type thermoelectric element (TE) to the metal cold pad and from this to the p-type TE, by Peltier effect, heat is absorbed in the metal–TE element junctions. The reverse applies to contact pads on electronics, where heating is generated by Peltier effect.

FEM simulation was used to calculate the expected temperature drop on each pixel. A temperature drop of 15 °C, bellow room temperature was obtained (Fig. 3). To obtain this cooling capacity, a membrane (200-nm thick) of silicon nitride supports four pairs of thermoelectric elements ($40\,\mu m \times 100\,\mu m \times 10\,\mu m$), powered with 14 mA current. Contact resistivity (between thermoelectric elements and metal pads) of $10^{-10}\,\Omega\,m^2$ was assumed on simulations [10,11]. Radiation and convection was considered on the cooled surface ($10\,W\,m^{-2}\,K^{-1}$). Thermoelectric properties of n-type and p-type elements were considered as achieved on previous experimental results [6,7]. Results obtained from FEM simulation on a single pixel microcooler agree with theoretical calculations [12].

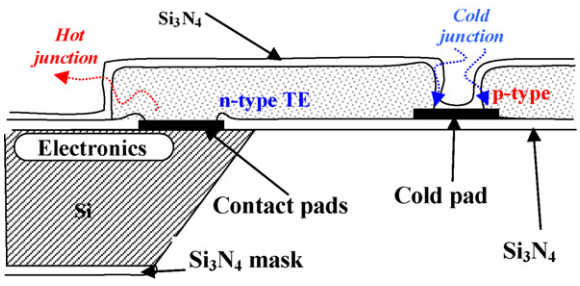

Fig. 2. Drawing of a pixel of the microcooler array (not on scale).

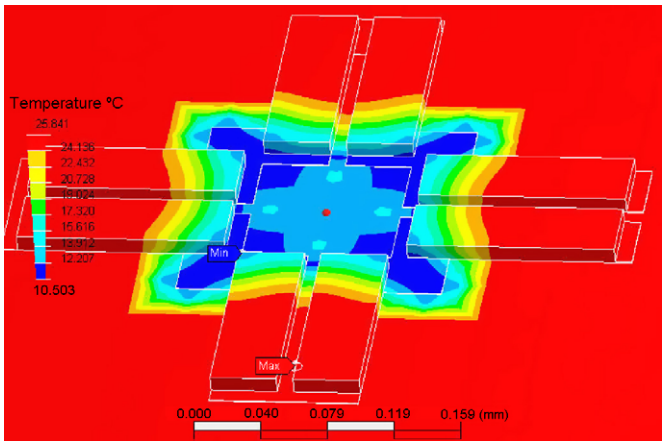

Fig. 3. Single pixel microcooler simulation shows the possibility to obtain 15 °C of cooling at the centre of the pixel.

All the cold junctions of the Peltier device are on the Si_3N_4 membrane. All the hot junctions of the Peltier device and the electronics are positioned on top of the silicon wafer (Fig. 2). The silicon wafer is used as thermal path to distribute all the heat generated by thermoelectric elements and electronics to an heatsink glued around the chip. Fig. 4 shows the overall expected heating of the backside of the chip due to the control electronics, Peltier effect and Joule heating. A power dissipation of 1 mW was considered for the electronics in each pixel and a current of 14 mA is supplied to each microcooler. A 500-μm thick silicon wafer was used, and the borders of the array were bounded to a fixed temperature of 25 °C (heatsink). A maximum temperature of 27.4 °C was obtained on the backside of silicon wafer.

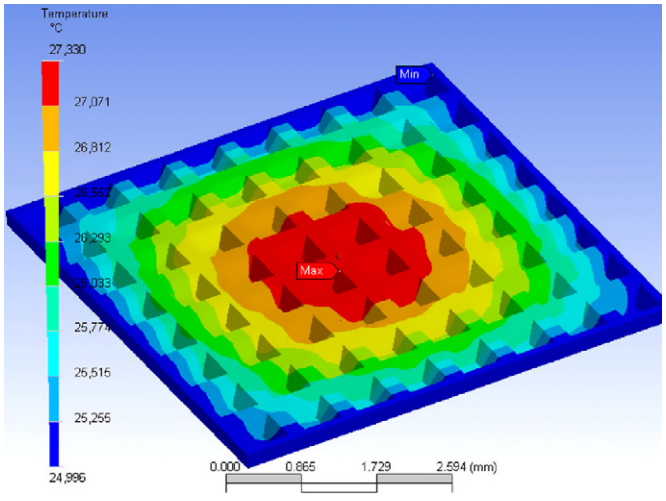

Fig. 4. Backside view of the simulated structure that supports the pixels showing that maximal heating is 2.3 °C above room temperature, with all pixels turned on to cool at full power.

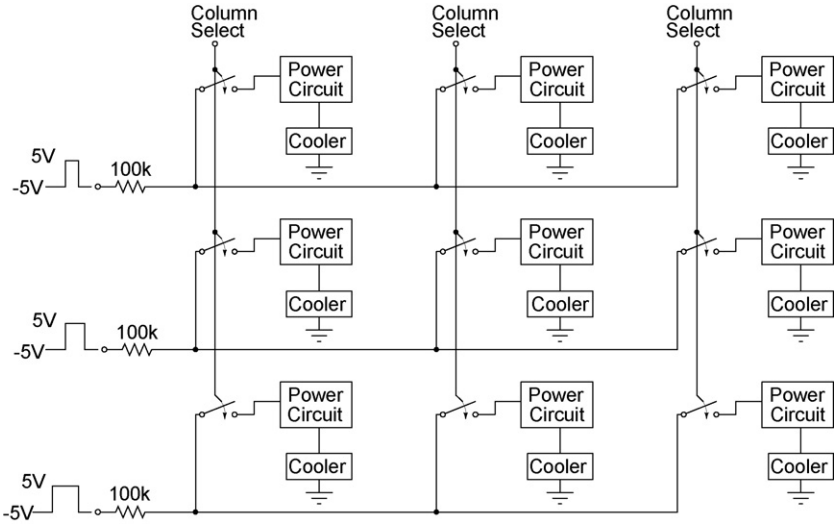

Fig. 5. Electronic circuit showing part of the 64 pixels of the device.

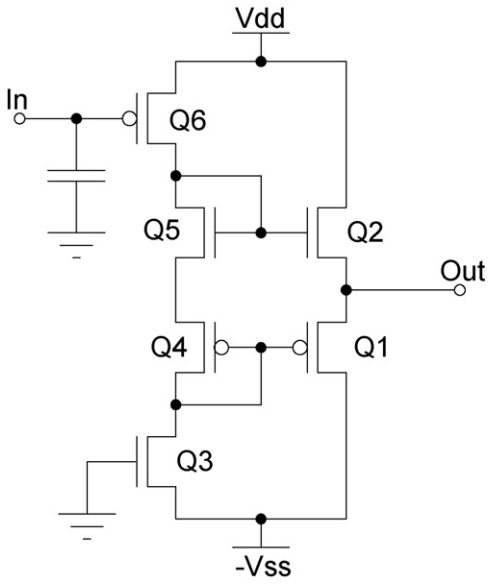

Fig. 6. Power circuit driving each pixel.

A CMOS microchip was designed, with the electronics to address and control each pixel of the array, memorizing the state of microcooler. Figs. 5 and 6 show the circuit repeated for 9 (of the 64) pixels. If the duty-cycle of the input signal is greater than 50%, the voltage across the capacitor becomes positive. By the other hand, if the duty-cycle is lesser than 50%, the voltage across the capacitor becomes negative. When the voltage across capacitor is positive, the voltage between the gate and the source of Q1 increases and the same of Q2 decreases. This causes an increase in Q1 current and a decrease in Q2 current. By the other hand, when the voltage across the capacitor is negative, the voltage between the gate and the source of Q1 decreases and the same of Q2 increases. This causes a decrease in Q1 current and an increase in Q2 current. Q5 and Q4 work as constant voltage sources biasing Q1 and Q2, once their currents are imposed by Q3. This solution allows controlling the power applied to each pixel. To minimize heating of Q1 or Q2, their dimensions and the power supply (Vdd and Vss) should be chosen in order to supply the maximum current to the microcoolers (14 mA), while keep Q1 or Q2 in the triode region. Working on saturation region will produce more heating on these transistors, rising the substrate temperature, if many pixels are turned on.

3. Fabrication steps

Fig. 7 presents the fabrication steps of the mircooler array. The backside of the wafer is covered with patterned Si_3N_4 layer which will act as a mask during etch on last step. The Si wafer (with electronics already fabricated) is also covered with a Si_3N_4 top layer where two vias are opened to access the contact metallic pads on top that will provide connection between electronics and thermoelectric elements. This Si_3N_4 layer will be used to fabricate the membrane where cool areas will be located. Metal pads to provide interconnection between TE elements are deposited and patterned. The p-type thermoelectric material is deposited by co-evaporation and patterned by photolithography on top of the wafer. An etchant with composition 10:6:26 HNO_3:HCl:H_2O (fuming 99.5% HNO_3 and 37% HCl) is used to etch Sb_2Te_3 p-type film without etching the metal contact pads [13] (etch rate below 0.1 nm/s was measured on contact pads). Bi_2Te_3 n-type film is deposited by co-evaporation and

Table 1
Thermoelectric properties of selected films at room temperature

Film	Te (%)	Bi or Sb (%)	Seebeck (μV/°C)	Resistivity (μΩ m)	Thermal conductivity (W m^{-1} K^{-1})	Figure of merit
Bi_2Te_3	62	38	−248	17.0	1.3	0.84
Sb_2Te_3	70	30	188	12.6	1.7	0.50

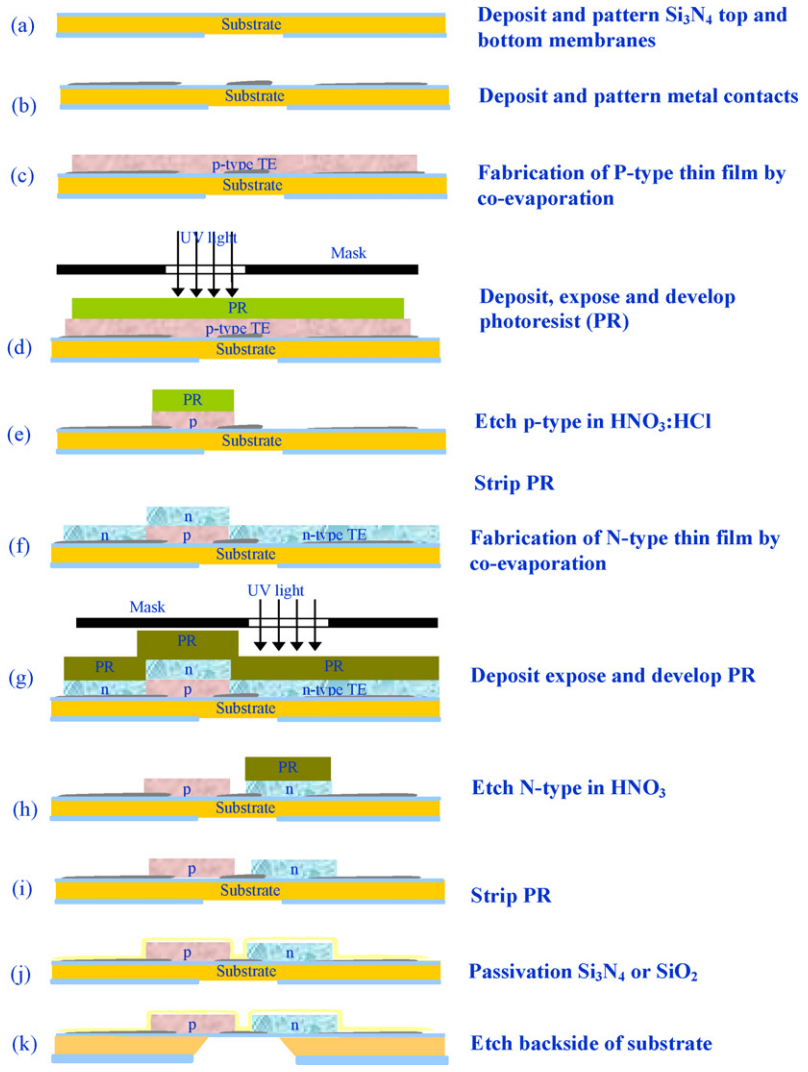

Fig. 7. Fabrication steps of the microcooler array.

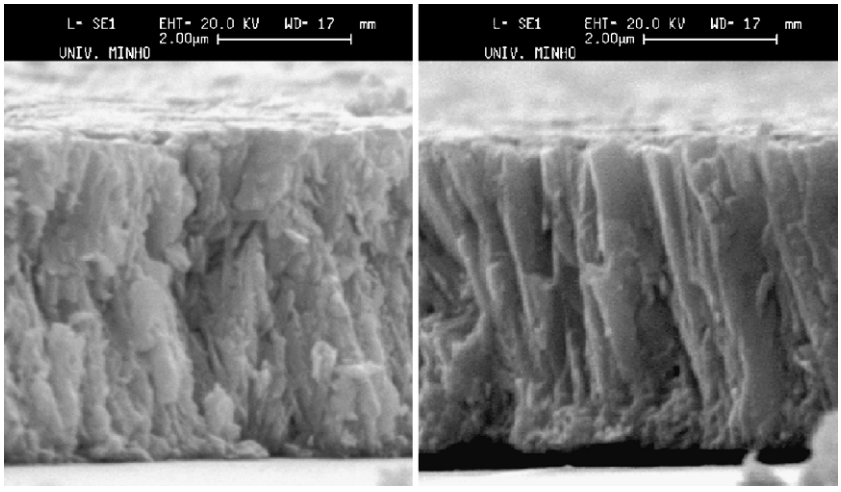

Fig. 8. SEM photo of Bi_2Te_3 (left) and Sb_2Te_3 (right) thin-films.

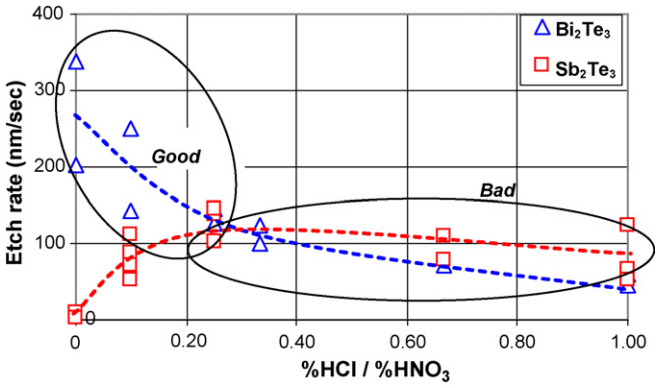

Fig. 9. Etch rate of Bi_2Te_3 and Sb_2Te_3 films in HNO_3:HCl solution (diluted 70% volume in water) as function of HNO_3/HCl content. Polyimide substrate was used.

patterned by photolithography. Table 1 presents thermoelectric properties and Fig. 8 shows a cross-section SEM photo of Bi_2Te_3 and Sb_2Te_3 films. HNO_3 (30% diluted in water) etches Bi_2Te_3 at etch rate of 250 nm/s and Sb_2Te_3 at etch rate of 5 nm/s, allowing selectivity of 50 times [13]. Fig. 9 plots the etch rate as function of etchant composition (pure HCl content divided by pure HNO_3 content), presenting the composition where best results are obtained. The etch rate observed on aluminium or chromium pads is also less than 0.1 nm/s. Etch rate measurements were all performed on Kapton polyimide substrate. Similar results are expected on top of Si_3N_4 substrate layer. Photoresist is removed and a passivation layer of Si_3N_4 is used to avoid degradation of the thermoelectric films in contact with atmospheric oxygen. The last step of fabrication is the etching of the back side of the Si wafer using KOH, to fabricate a membrane of Si_3N_4 on each pixel that supports the microcooler elements. This membrane achieves significant reduction of thermal conduction between the cold and the hot sides of the Peltier device. Electronic circuits in the wafer are confined to the regions between the microcoolers to prevent damage during the last KOH fabrication step.

4. Experimental results

An enlarged microcooler individual pixel was fabricated and tested on top of a polyimide substrate that emulates the Si_3N_4 membrane (Fig. 10). The fabrication of these enlarged microcooler pixel allowed a rapid demonstration prototype. The working principle of the microcooler and the quality of materials were demonstrated and evaluated. The performance of the microcooler was analyzed by use of a thermal image map generated with an infrared microscope. An image was obtained with a 4 mA current through the device and cold and hot sides are clearly identified (Fig. 11).

A temperature difference of 5 °C was measured between the hot and the cold sides, under vacuum. The distance from expected results is due to high contact resistances between metal pads and thermoelectric elements. A contact resistance of $10^{-6}\,\Omega\,m^2$ was measured, with a method [7] based on TLM (transmission line model) method. This value is expected to

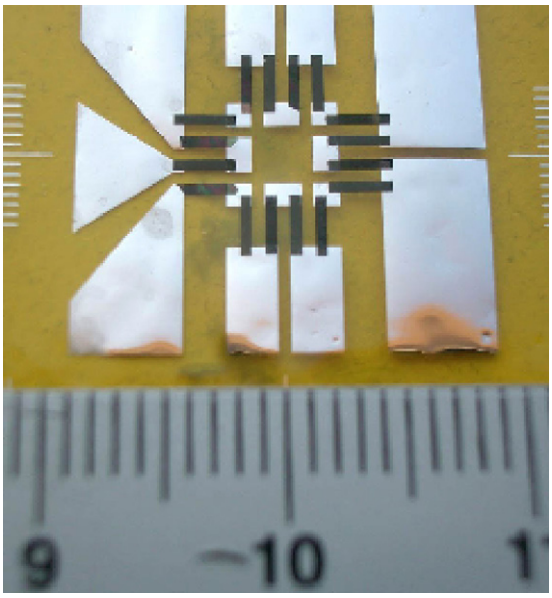

Fig. 10. Photo of a microcooler pixel, on top of a polyimide substrate.

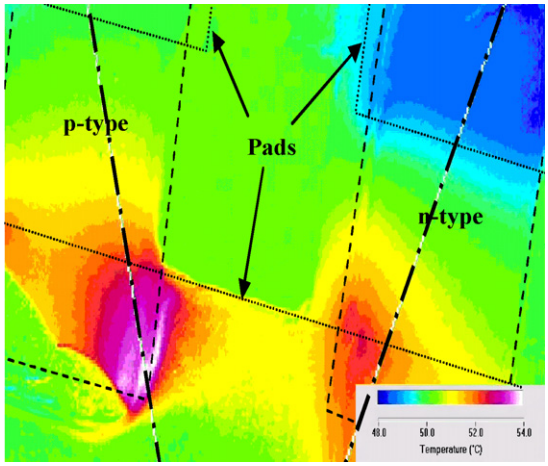

Fig. 11. Thermal image of n-type and p-type thermoelectric elements, powered with 4 mA current, under vacuum.

be reduced to less than $10^{-9}\,\Omega\,m^2$ using an interface layer in the fabrication process [2,11]. The high temperature achieved on the hot side of the device results from the low dissipation capability due to the low thermal conductivity of the substrate used in the prototype (polyimide) compared with the substrate used in simulation (silicon covered with silicon nitride). The low thermal conductivity in contact pads also contributes for this higher temperature on the hot side of the device.

5. Conclusions

An array of microcoolers, with 64 pixels, with each pixel controlled independently to cool or heat was designed and simulated, and the respective fabrication process was described. A temperature difference of ±15 °C could be achieved in each pixel. Thermoelectric thin-films with high figure of merit were

obtained by co-evaporation, suitable for fabrication of such microcoolers, and lithographic pattern techniques were applied on these films. Bi_2Te_3 and Sb_2Te_3 films were patterned with 3:7 HNO_3:H_2O and 10:6:26 HNO_3:HCl:H_2O (99.5% HNO_3 and 37% HCl), respectively, and selectivity of 50× was measured between these two processes.

A large area pixel of the microcooler was fabricated and its performance analyzed under microscopic infrared imaging. A temperature difference of 5 °C was obtained. Differences from expected performance are due to high electrical resistance and low thermal conductance obtained in the pad–thermoelectric material interface. Efforts are being made to reduce contact resistance and fabricate thermoelectric elements with lower dimensions.

Acknowledgements

This work was supported by ADI (MPYROM) and Portuguese Foundation for Science and Technology (SFRH/BD/18142/2004). First author also would like to thank Gao Min and D.M. Rowe infrared thermal imaging and F. Völklein for thermal conductivity measurements.

References

[1] H. Böttner, J. Nurnus, et al., New thermoelectric components using microsystem technologies, J. Microelectromech. Syst. 13 (2004) 414–420.
[2] L.W. da Silva, M. Kaviany, Fabrication and measured performance of a first-generation microthermoelectric cooler, J. Memsci 14 (5) (2005) 1110.
[3] G.J. Snyder, J.R. Lim, C.-K. Huang, J.P. Fleurial, Thermoelectric microdevice fabricated by a MEMS-like electrochemical process, Nat. Mater. Lett. 2 (2003) 528–531.
[4] H. Böttner, Micropelt miniaturized thermoelectric devices: small size, high cooling power densities, short response time, in: Proceedings of ICT, Clemson, SC, 2005.
[5] D.D.L. Wijngaards, S.H. Kong, M. Bartek, R.F. Wolffenbuttel, Design and fabrication of on-chip integrated polySiGe and polySi Peltier devices, Sens. Actuator A: Phys. 85 (2000) 316–323.
[6] L.M. Goncalves, C. Couto, J.H. Correia, P. Alpuim, G. Min, D.M. Rowe, Optimization of thermoelectric thin-films deposited by co-evaporation on plastic substrates, in: Proceedings of ECT'06, Cardiff, UK, 2006.
[7] L.M. Goncalves, C. Couto, J.H. Correia, P. Alpuim, G. Min, D.M. Rowe, Flexible thin-film planar Peltier microcooler, in: Proceedings of ICT'06, Vienna, Austria, 2006.
[8] F. Völklein, Characterization of the thermal properties of bulk and thin-film materials by using diagnostic microstructures, in: Proceedings of the Symposium on Microtechnology in Metrology and Metrology in Microsystems, Delft, The Netherlands, 2000.
[9] D.M. Rowe (Ed.), CRC Handbook of Thermoelectrics, CRC press, 1995.
[10] L.W. da Silva, M. Kaviany, Micro-thermoelectric cooler: interfacial effects on thermal and electrical transport, Int. J. Heat Mass Transfer 47 (2004) 2417–2435.
[11] U. Birkholz, R. Fettig, J. Rosenzweig, Fast semiconductor thermoelectric devices, Sens. Actuator 12 (2) (1987) 179–184.
[12] F. Völklein, G. Min, D.M. Rowe, Modelling of a microelectromechanical thermoelectric cooler, Sens. Actuator 75 (1999) 95–101.
[13] L.M. Goncalves, J.G. Rocha, C. Couto, P. Alpuim, G. Min, D.M. Rowe, J.H. Correia, Fabrication of flexible thermoelectric microcoolers using planar thin-film technologies, J. Micromech. Microeng. 17 (2007) S168–S173.

Biographies

Luís Goncalves graduated in 1993 and received his MSc degree in 1999, both in industrial electronics engineering from the University of Minho, Guimarães, Portugal. From 1993 to 2002 he researched on embedded systems and electronics, on Idite-Minho, an institute to interface between university and industry, Braga, Portugal. Since 2002, he has been a lecturer at Electronics Department, University of Minho. There, he started a new lab on thermoelectric thin-film deposition, characterization and patterning, in collaboration with Physics Department. He is currently working towards his PhD degree and is involved in the research on thermoelectric materials for on-chip cooling and energy harvesting. His professional interests are thermoelectrics, microfabrication technology and microsystems.

José Gerardo Vieira da Rocha received the BSc, MSc, and PhD degrees from the University of Minho, Guimaraes, Portugal, in 1995, 1999 and 2004, respectively, all in industrial electronics engineering. A significant part of his PhD work was done at Delft University of Technology, Delft, The Netherlands. Since 2004, he has been an assistant professor with the Department of Industrial Electronics, University of Minho, where he is involved in the research of radiation sensors.

Carlos Couto graduated in electrical engineering at University of Lourenco Marques, Mozambique, in 1972. He obtained the MSc degree in 1979 and PhD degree in 1981 at UMIST (University of Manchester Institute of Science and Technology), UK, both in power electronics. In 1976, he joined the University of Minho in Portugal, where since 1995, he has been full professor in the Department of Industrial Electronics. His research interests are microsystems, instrumentation and power electronics.

Pedro Alpuim received the PhD degree in materials science and engineering from Instituto Superior Técnico, Lisbon, Portugal, in 2003. His PhD thesis was on the deposition and clean-room fabrication of amorphous and nanocrystalline silicon thin-film transistors and other devices on plastic substrates. Since 2003 he has been with the University of Minho in Guimaraes, Portugal, where he is an assistant professor in the Physics Department. There, he obtained support from European partners and from his own university to start a new lab on semiconductor thin-film deposition and characterization using CVD and PVD deposition techniques. His current research interests include thin-film devices for energy applications such as solar cells and thermopiles, flexible electronics, and thin-film silicon-based optoelectronics for telecommunications.

José Higino Correia graduated in Physical Engineering from University of Coimbra, Portugal, in 1990. He obtained in 1999 a PhD degree at the Laboratory for Electronic Instrumentation, Delft University of Technology, working in the field of microsystems for optical spectral analysis. Presently, he is an associate professor in Department of Industrial Electronics, University of Minho, Portugal. His professional interests are in micromachining and microfabrication technology for mixed-mode systems; solid-state integrated sensors, microactuators and microsystems.