

A 2.4-GHz RF CMOS transceiver for wireless sensor applications

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A radio-frequency transceiver chip was designed in a UMC RF 0.18 μm CMOS process. The target RF frequency is 2.4 GHz ISM band. The specifications are a sensibility of -60 dBm and a power transmission of 0 dBm. The power supply of the transceiver is 1.8 V. Simulations show a power consumption of 10.7 mW. Innovative topics concerning efficient power management was taken into account during the design of the transceiver.

1.1 INTRODUCTION

This paper describes a radio frequency transceiver designed in UMC RF 0.18 μm CMOS process. This process has a poly and six metal layers, allowing the use of integrated spiral inductors (with a reasonable quality factor), high resistor value (a special layer is available) and a low-power supply of 1.8 V. This RF CMOS transceiver will be applied to implemented a wireless sensors network in a wireless electronic shirt for helping health professionals with rapid, accurate and sophisticated diagnostic concerning cardiopulmonary disease in order to evaluate the presence of breathing disorders in free-living patients. Without proper design, communication will increase network power consumption significantly because listening and emitting are power-intensive activities [1]. Thus, in order to optimise power consumption, it was included in the design of the RF transceiver, the use of control signals. With these control signals it is possible to enable and disable all the transceiver subsystems. These signals allows for example to switch off the receiver when a RF signal is being transmitted, to switch off the transmitter when a RF signal is being received, and to put the transceiver in sleeping mode when neither RF signals are being transmitted, nor being received.

1.2 TRANSCEIVER ARCHITECTURE

The transceiver has a low-noise amplifier (LNA) that provides a 50 Ω input impedance, using a tuned load to provide high selectivity. The amplified RF signal is downconverted to the baseband with an envelope detector. Internal oscillator is a phase-locked loop (PLL) working at 2.4 GHz, with a stable crystal oscillator reference of 20 MHz. An internal antenna-switch was included in the design. The whole transceiver structure is illustrated in Figure 1.

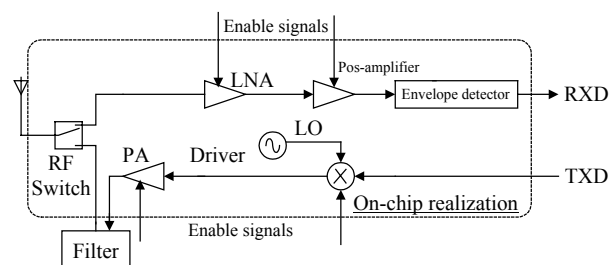


Figure 1: The block schematic of the transceiver.

1.3 ANTENNA SWITCH

An internal antenna-switch makes this transceiver a true complete system-on-a-chip. The antenna-switch connects the antenna to one of the receiver or transmitter path, that are connected to the RX and TX ports, respectively. The signal V_{CTL} selects the port to be connected to the antenna. The isolation between non-connected ports must be high. In order to have a power efficient transceiver without degrading its sensitivity, the losses in the switch must be low. The next table shows the simulation results for the antenna-switch. These results are much better, compared with reference values [2].

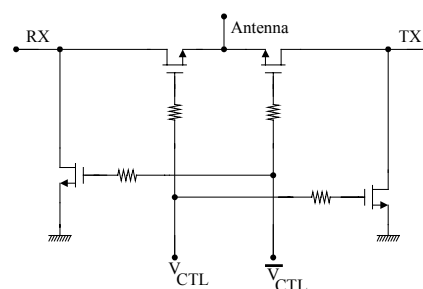


Figure 2: The antenna-switch [2].

Table 1: Simulated S parameters for the switch.

S parameters	V_{CTL} state
$S_{RX, Antenna} = -1.32$ dB	On
$S_{RX, Antenna} = -41.51$ dB	Off
$S_{Antenna, TX} = -41.50$ dB	On
$S_{Antenna, TX} = -1.32$ dB	Off
$S_{RX, TX} = -43.44$ dB	On
$S_{RX, TX} = -43.54$ dB	Off

1.4 RECEIVER

1.4.1 LOW-NOISE AMPLIFIER

The low-noise amplifier (LNA) is the first gain stage in the receiver path. The noise figure (NF) of the LNA is a measure of the degradation of the signal-to-noise ratio (SNR) at the output of the LNA, compared to that at the input. Another main performance parameter is its gain. The signal should be amplified as much as possible, with hardly lowering the SNR. This is achieved with the best noise figure.

As illustrated in Figure 3, the LNA is an inductively degenerated common source amplifier [3,4]. This makes the input impedance at 2.4 GHz equal to 50Ω , for matching with antenna switch. Cascoding transistor M_2 is used to increase the gain, to better isolate the output from the input and to reduce the effect of M_1 's C_{gs} . Transistor M_3 is used to bias the transistor M_1 , and its width is a small fraction of M_1 's width, to minimise the power overhead of the bias circuit.

This LNA is an improved version of the LNA presented in [5]. On this version, all of the inductors are internal (including the L_g inductor, where it was formerly external) and where it was taken in account the wire inductance, that connects the PADs of the die, to the external PCB. A source inductance $L_s=0.9$ nH, made with the wire from the PAD connected to the M_1 's sources to the PCB. It were used in the design, a gate inductance $L_g=20$ nH, an inductance $L_{sd}=10$ nH, and a drain inductance $L_d=3.2$ nH. The inductance L_{sd} improves the S_{11} , keeping the S_{21} in an acceptable level. Simulations show a gain of 17.24 dB, a return loss at the input of -17.20 dB and a noise figure $NF=1.68$ dB ($F=SNR_{in}/SNR_{out}=1.47$).

As cited before, the transceiver must have a power efficient management, thus in the idle or transmitting modes, the LNA is disabled by switching off the bias circuitry. The same principle applies to all subsystems of the transceiver, being no more cited on this paper.

1.4.2 ENVELOPE DETECTOR

Figure 4 shows the envelope detector schematic. Basically, the idea is that an increasing input amplitude implies a decrease in the transistor M_1 gate voltage (in order to keep branch current constant) what means a decrease in the gate voltage of the transistor M_2 (after filtering), thus decreasing the transistor M_2 current itself. When this current reach a point where cancels with the transistor M_3 mirror current, then the output capacitance starts to discharge and the output voltage goes to high. The minimum voltage amplitude at the input is 70 mV.

1.5 TRANSMITTER

1.5.1 PHASE-LOCKED LOOP

As depicted in Figure 5, the PLL has a reference generator circuit with a crystal based oscillator at

20 MHz, followed by a Phase-Frequency Difference Circuit (PFD) without dead zone, a current steering charge pump (CP), a third order passive filter. The passive section output is connected to the Voltage Controlled Oscillator (VCO), that generates the desired frequency of 2.4 GHz. Finally, in order to get the 2.4 GHz, this frequency must be divided by 120 and connected to the PFD again, closing the loop.

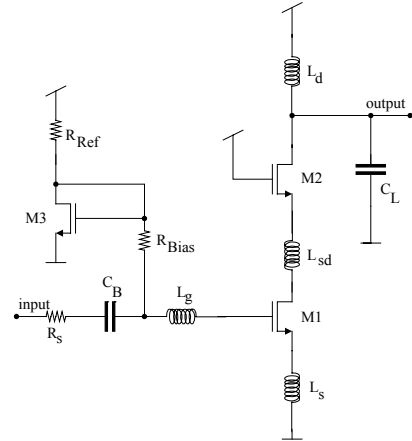


Figure 3: The LNA circuit [3,4].

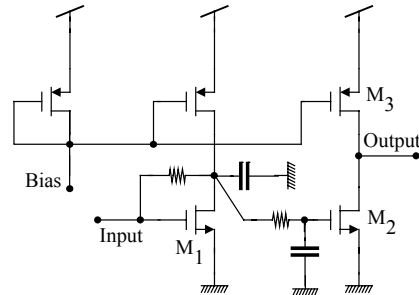


Figure 4. The envelope detector, and voltage V_{in} at the input and voltage V_{out} at the output.

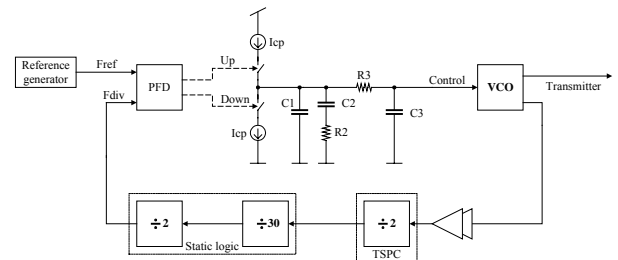


Figure 5: The PLL structure.

The charge pump is a current steering, with Up and Down currents $I_{Up}=173 \mu A$ and $I_{Down}=178 \mu A$, with a detector gain constant $K_{\phi}=175 \mu A/2\pi$ rad. This circuit avoids the conventional problem in charge pumps, that limits the opening and closing of current sources, in fact, in spite of being switched, the current is routing from the load, to a alternative path, and from that path to the load.

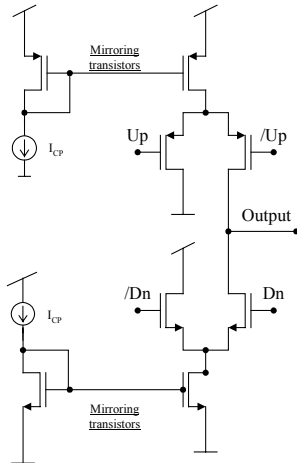


Figure 6: The currents steering charge-pump.

In order to saving on-chip area, it was used a current starved ring oscillator [6] to implement the VCO, rather than a tuned LC oscillator. This VCO has the advantage to control the full range [0, 1.8 V], providing a frequency range of [2.016, 2.757 GHz], with a tuning constant $K_{VCO}=876.6$ MHz/V, calculated in the linear working range. The structure of this VCO is shown in Figure 7.

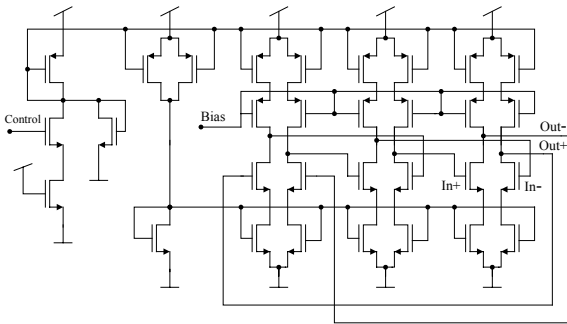


Figure 7: The voltage controlled oscillator [6].

The 2.4 GHz frequency is achieved with a 20 MHz reference, dividing it by 120. This is done with a cascade constituted by one half divider implemented with true single phase clock (TSPC) logic, one divider by 30, followed by a toggle flip-flop. TSPC logic works only when the input signals are rail-to-rail [7].

1.5.2 POWER AMPLIFIER

The function of the power amplifier is to provide a transmitted signal with an appropriated output power. The power amplifier has a cascade of five inverters, in order to drive the ASK output signal to the input of power amplifier. The Figure 9 shows the power amplifier, where it is possible to select between none or three different output powers. In that figure, the network L_1-C_1 eliminates the strong second harmonic of the carrier, while the network L_2-C_2 , is tuned to carrier frequency. The maximum simulated output power is 1.28 mW.

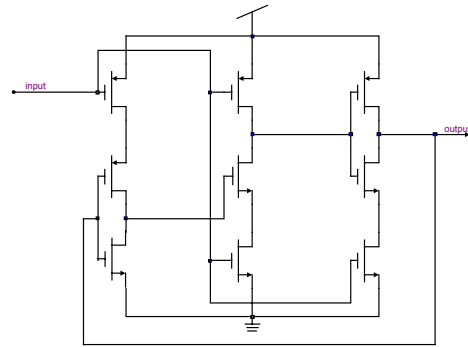


Figure 8: The TSPC frequency divider by 2.

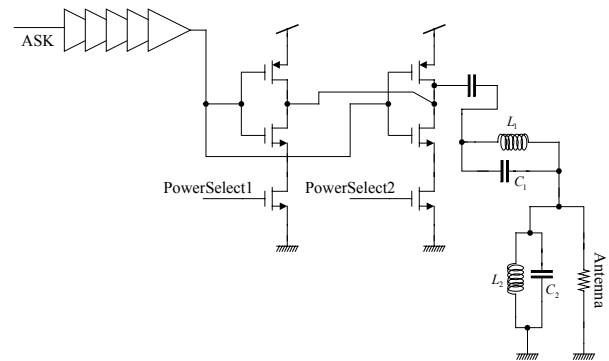


Figure 9: The power amplifier.

1.7 CONCLUSIONS

A low-power low-voltage radio-frequency transceiver at 2.4 GHz, working with a supply voltage of 1.8 V was presented in this paper. Simulations show a power consumption of 10.7 mW. Innovative techniques were included in the frequency divider, e.g., the use of TSPC logic. This logic can overcome the limitation of this technology to toggle in static logic, signals at frequencies above 2 GHz. The receiving mixer was designed, with a new switched transconductance technique. This RF CMOS transceiver will be applied in a wireless electronic shirt for helping health professionals with rapid, accurate and sophisticated diagnostic concerning cardiopulmonary disease in order to evaluate the presence of breathing disorders in free-living patients.

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