A Wireless RF CMOS Interface for a Soil Moisture Sensor

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Summary. *This paper describes a wireless RF CMOS interface for a soil moisture sensor. The mixed-signal interface is based on a 2^{nd}order switched capacitor, fully differential sigma-delta modulator with an effective resolution of 17-bit. The modulator bit stream output is applied to a counter as a first order decimation filter and encoded as a pulse width modulated signal. This signal is then transmitted by means of an amplitude shift keying modulation, through a power amplifier operating at $433.92\ MHz$ in class-E mode. The soil moisture sensor is based on Dual-Probe Heat-Pulse method and is implemented using an integrated temperature sensor and heater. After applying a heat-pulse, the temperature rise that is a function of soil moisture, generates a differential voltage that is amplified and applied to the mixed-signal interface input. The described interface can also be used with other kinds of environmental sensors in a wireless network for agricultural environments such as greenhouses. The CMOS mixed-signal interface has been implemented in a single-chip using a standard CMOS process (AMI $0.7\ \mu m$, n-well, 2 metals and 1 poly).*

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Category: 9 (System architecture, electronic interfaces, wireless interfaces)

1 Introduction

The control of physical and chemical variables in agriculture fields require the use of several sensors, as soil temperature and relative humidity, CO_2 concentration, solar radiation, soil moisture, among others.

An important goal in agricultural exploitations it is the need to minimize natural resources over-consumption, namely water supply in irrigation systems. Irrigation management systems should have information about soil moisture at the plant root level. With such information, only the necessary water could be provided in an efficient way.

Today a large number of sensors based on different methods are available for measuring soil moisture. However, they present a few drawbacks: as inaccuracy, high-cost and soil dependency.

Integrated microsensors, with on-chip interface circuitry, are currently replacing discrete sensors due to their inherent advantages, namely, low cost, high reliability and on-chip processing. To accomplish small, robust and inexpensive microsystems, it is desirable to integrate the soil moisture sensor with digital signal processing and wireless front-end. Therefore, this microsystem can be installed near plants roots for measuring real plant water needs.

2 System overview

The complete system is divided in two blocks, as depicted in Fig. 1: the sensing system and the mixed-signal interface.

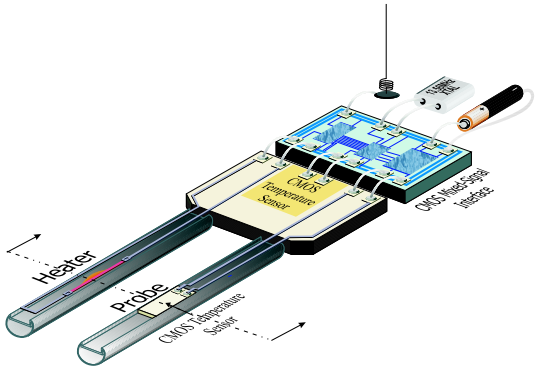

Fig. 1: System Overview.

The sensing system is based on a dual probe where in one rod is placed a heater and in the other rod a temperature sensor. A special package will allow its implementation near plants roots.

The implemented CMOS mixed-signal interface, outlined in Fig. 2, includes a 2^{nd}order switched-capacitor fully differential sigma-delta ($\Sigma\Delta$) modulator, a first-order decimation filter, a shift register and frame generator, a pulse width encoder, an amplitude-shift-keying (ASK) modulator and a RF switch. The $433.92\ MHz$ carrier is generated on-chip by means of a phase-locked loop (PLL).

3 Mixed-signal interface

The water in the soils must be measured with a resolution better than 1%. The sensing system, developed in a previous work, [1], has a differential output of about $0.825\mu\text{V}/m^3m^{-3}$ and signal bandwidth is typically a

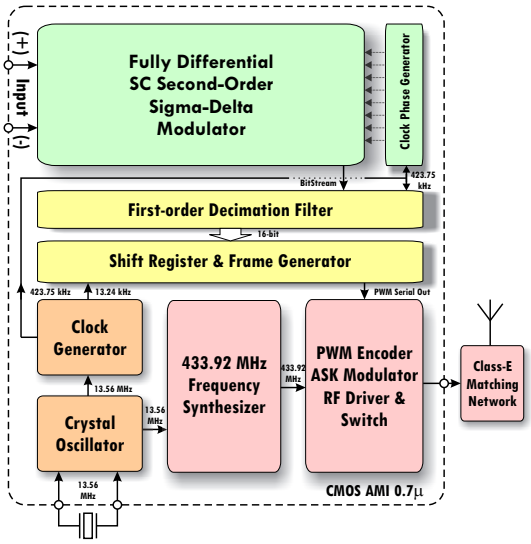

Fig. 2: Mixed-signal interface architecture.

few Hz.

3.1 Analog section

Previous studies have showed that a second-order $\Sigma\Delta$ modulator is a suitable architecture for converting this kind of signal to digital domain. The second-order architecture is preferred to the simpler first-order one because it is less sensitive to the correlation between the input and the quantization noise, which reduces the presence of pattern noise [2].

The 2^{nd}order $\Sigma\Delta$ modulator has been implemented using switched capacitor techniques. In addition to robustness of these techniques, the use of fully differential topology minimizes common mode interferences, switches charge injection and clock feedthrough. The two integrators are based on fully differential folded-cascode amplifiers biased by a constant-gm wide swing circuit. Also, for reducing the influence of the first-amplifier offset and low-frequency noise, a chopper scheme has been implemented. The modulator reference is external and set to $\pm 0.5V$. The complete $\Sigma\Delta$ modulator is shown in Fig. 3.

The dominant sources of error in the $\Sigma\Delta$ modulator are quantization and thermal noise. A clock frequency of $423.75kHz$ with an oversampling ratio (OSR) of 256 was chosen to make the quantization noise insignificant. This results in an input signal bandwidth of about $830Hz$ which is fairly above the requirement. Thermal noise is essentiality determined by the size of sampling capacitors which are in our case $6pF$.

The amplifiers used in the $\Sigma\Delta$ modulator are based in a fully-differential folded-cascode topology. A NMOS-input topology was preferred to a PMOS-input one because PMOS transistors generate more thermal noise (for the same dimensions and current). The higher flicker noise associated to the NMOS transistors will be reduced by the chopper action. Also, input transistors were chosen to be large enough to minimize systematic offset by employing matching techniques.

$\Sigma\Delta$ modulators show low sensitivity to the errors induced during internal quantization. In our case, having a single-bit (two-level) quantization, errors are limited to offset and hysteresis. For a 2^{nd}modulator the offset is attenuated by A_V^2, where A_V is the amplifier open-loop low-frequency gain. The hysteresis, as an indetermination of the output state for small input values, is also attenuated by the high DC-gain of the integrators. This low-demanding performance requirements leads to a simple solution based on a clocked comparator followed by a NOR SR flip-flop with minimum size transistors to reduce resolution time.

Special care has been taken in the layout of the $\Sigma\Delta$ modulator which was manually routed. All matched transistors and capacitors have been laid using common-centroid techniques. The switches used in the SC implementation are all transmission gates.

3.2 Digital section

The bitstream output is applied to a counter as a 1^{st}order decimation filter as seen in Fig. 4. The time-base circuit generates a signal to latch the counter data and afterwards a reset signal to clear the counter.

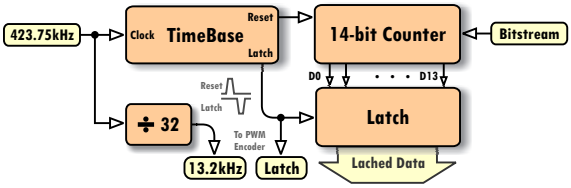

Fig. 4: First-order decimation filter.

For each counting, a sample is generated, stored and transmitted. Prior to transmission, data is encoded in pulse widths of 25 % and 75 % duty-cycle representing the logic levels '0' and '1' respectively. For error detection and receiver synchronization, data is assembled together with a $11-bit$ preamble and a $4-bit$ checksum. The assembled frame has a $29-bit$ length and takes about $4.39ms$ to be transmitted. The PWM encoder as well as the frame generator block diagram is shown in Fig. 5. The resulting frame is then transmitted by means of a amplitude shift keying modulation. The modulated signal is then applied to a class-E power amplifier that drives a small off-chip loop antenna to transmit the signal.

3.3 RF transmitter module

The RF transmitter module schematically represented in Fig. 6, includes a crystal-controlled frequency synthesizer, a PWM encoding circuit, an ASK modulator, a RF driver and a RF switch. With the convenient matching network, the transmitter operates in Class-E mode.

By using a simple modulation scheme such as ASK, where the carrier is switched on and off, carrier frequency generation circuit can be relaxed. In this way,

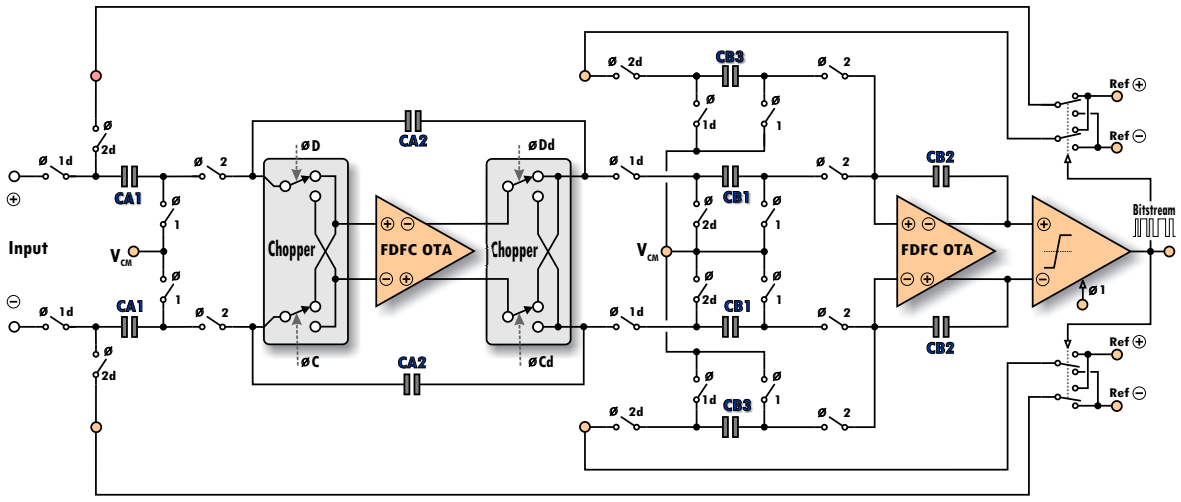

Fig. 3: Complete 2^{nd}order SC $\Sigma\Delta$ modulator.

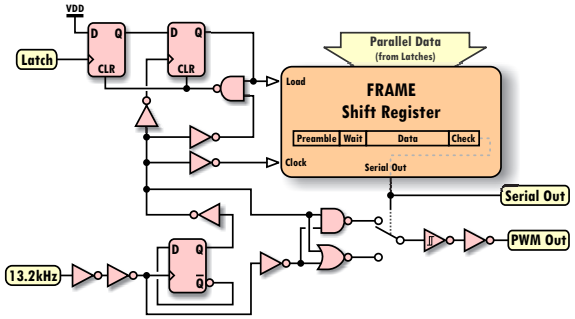

Fig. 5: Shit register and PWM encoder block diagram.

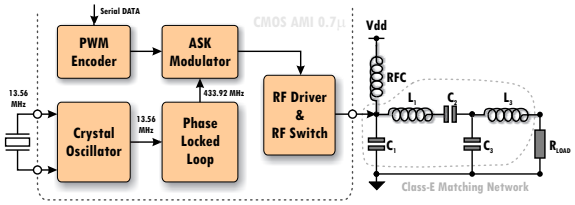

Fig. 6: Transmitter module diagram.

and to ensure carrier stability, the frequency synthesizer was implemented as a classical phase-locked loop (PLL) using a $13.56\ MHz$ crystal reference oscillator.

The PLL consists of a phase-frequency detector (PFD), charge pump (CP), 3^{rd} order passive loop filter, current-starved voltage-controlled oscillator (VCO), and a fixed divider, as shown in Fig. 7. The phase-frequency detector identifies phase and frequency differences between the reference and the divider signals. With the charge pump and loop filter these differences are converted into a control voltage to adjust the output frequency.

The phase-frequency detector generates two signals, Up and $Down$, that controls the charge pump to charge and discharge the loop filter equivalent capacitor C_{LF}. Special care has been taken to avoid overlapping between these signals that leads to a short circuit in the charge pump. Also, a delay was inserted in the path

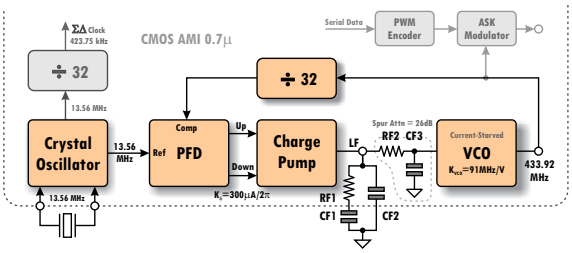

Fig. 7: Phase Locked Loop Block Diagram.

of reset signal to eliminate the dead-zone problem thus reducing the phase noise of the PLL.

In a conventional CMOS charge pump, the switches controlled by the Up and $Down$ signals are directly connected to the output node. When one of the switches are turned on, the charge on the LF equivalent capacitor, C_{LF}, will be shared with the switch parasitic capacitance. This induces glitches in the charge pump current which increases spurs in the PLL output signal, [3]. In the implemented charge pump, Up and $Down$ signals are used to switch on and off a current mirror with current matching, thus avoiding charge sharing in the CP output node. The charge pump current was designed to be 300μA.

The 3^{rd} order passive loop filter comprises an off-chip 2^{nd} order filter section(RF_1, CF_1 and CF_2), connected to the LF pin and an internal RC section (RF_2 and CF_3) providing an extra pole to assist the attenuation of the sidebands at multiples of the comparison frequency (spurs) that may appear. The resulting PLL is then a type-2 fourth-order loop which provides great noise supression in the PLL output spurious level.

The VCO is based in the current-starved configuration with five delay stages. To avoid the problem of locking on harmonics of the desired output frequency, the maximum output frequency has been limited. Output frequency range is between $330MHz$ and $500MHz$. The $433.92MHz$ carrier frequency is approximately the VCO center frequency and is obtained for an input voltage of about $2.3\ V$.

4 Results

Simulations from the extracted layout have shown that it can be expected an effective resolution of about $17bit$ ($DR = 103.36db$) for the $\Sigma\Delta$ modulator. The quantization noise power, P_Q, is $-112.28db$. Thermal noise contribution, P_{TH}, mainly due to the $6pF$ sampling capacitors, is $-115.57db$. Incomplete settling error in the first integrator is $P_{ST} = -108.87db$.

As a prototype, and for testing purposes, the output of the modulator (bitstream) is available outside for off-chip digital filtering and decimation. For this prototype it was chosen to process internally 14-bit samples for testing the digital section and the RF transmitter. In this case, conversion time is $38.8ms$ for a clock frequency of $423.75\ kHz$.

The PLL has a simulated lock time of about 6μs as shown in Fig. 8. Loop filter values were $RF_1 = 3.9k$, $CF_1 = 220pF$, $CF_2 = 12.2pF$, $RF_2 = 33k$ and $CF_3 = 1.5pF$.

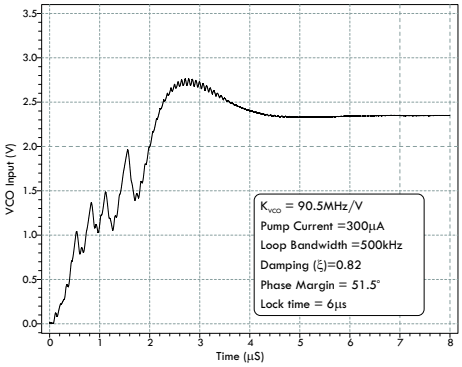

Fig. 8: PLL Simulated lock time.

Fig. 8 shows the simulated transfer function of the voltage-controlled oscillator. The VCO constant, K_{VCO}, is approximately $90.5MHz/V$.

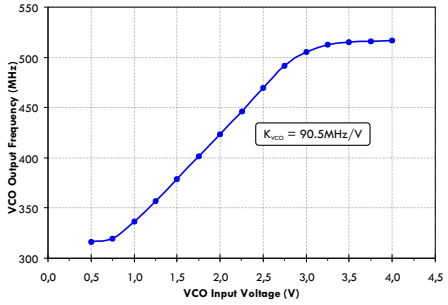

Fig. 9: VCO transfer function.

Fig. 10 shows a binary pattern '011' PWM encoded signal (A) and transmitted signal (B) in a 50Ω load.

In this first prototype, the typical class-E matching network is off-chip. Since component values are suited for integration, they will be on-chip in the next prototype. Fig. 11 shows the layout of the implemented mixed-signal interface. Die area is $3.79mm^2$.

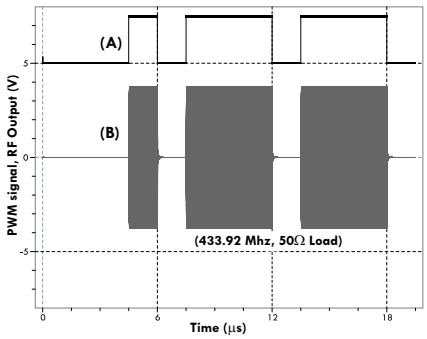

Fig. 10: PWM signal and RF output signal.

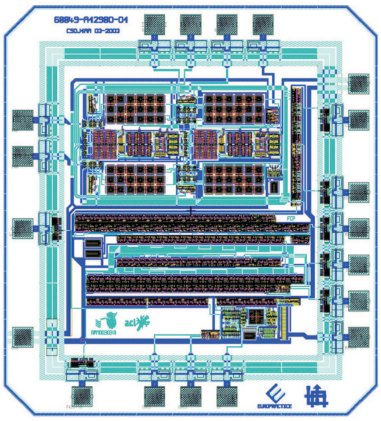

Fig. 11: Layout of the described mixed-signal interface.

5 Conclusions

In this paper a Wireless CMOS mixed-signal interface for a soil moisture sensor has been proposed. Chip layout has been submitted to fabrication through Europractice IC service. A set of experiments has to be done for testing the reliability and precision of results.

Some enhancements are now being carried out, such as a receiver, among others. With bidirectional communications capabilities, it will be possible to implement a wireless network of soil moisture sensors in a smart irrigation control system.

References

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