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A wireless RF CMOS mixed-signal interface for soil moisture measurements

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Abstract

This paper describes a wireless RF CMOS interface for soil moisture measurements. The interface basically comprises a Delta-Sigma ($\Delta\Sigma$) modulator for acquiring an external sensor signal, and a RF section where data is transmitted to a local processing unit. The $\Delta\Sigma$ modulator is a single-bit, second-order modulator and it is implemented using switched-capacitors techniques in a fully-differential topology. With a sampling frequency of 423.75 kHz and an oversampling ratio (OSR) of 256, the modulator achieves a dynamic range of 98.7 dB (16.1 bit). The output of the modulator is applied to a counter, as a first-order decimation filter, and the result is stored. Prior to transmission, data is encoded as a pulse width modulated signal and assembled in a frame containing preamble and checksum control fields. This frame is then transmitted through a power amplifier operating at 433.92 MHz in class-E mode. To evaluate the $\Delta\Sigma$ modulator performance, the bitstream was acquired and transferred to a personal computer to perform digital filtering and decimation using MATLAB. The soil moisture sensor is based on dual-probe heat-pulse (DPHP) method and is implemented by using an integrated temperature sensor and a heater. After applying a heat-pulse for a fixed period of time, the temperature rise, that is a function of soil moisture, generates a differential voltage that is amplified and applied to the mixed-signal interface input. The described interface can also be used with other kinds of environmental sensors in a wireless sensors network. The CMOS mixed-signal interface has been implemented in a single-chip using a standard CMOS 0.7 μm process (AMI C07M-A, *n*-well, 2 metals and 1 poly).

Keywords: Wireless; Delta-sigma; Soil moisture sensors; Sensor interfaces

1. Introduction

The control of physical and chemical variables in agriculture fields require the use of several sensors, such as soil temperature and relative humidity, CO_2 concentration, solar radiation, soil moisture, among others.

An important goal in agriculture is the need to optimize the use of natural resources, namely water supply in irrigation systems. Irrigation management systems should have information about soil moisture at the root level of plants. With such information, irrigation water could then be provided in a more efficient way.

Today a large number of sensors based on different methods are available for measuring soil moisture [1]. However, they present one or more of the following drawbacks: inaccuracy, high-cost and soil dependency.

Integrated microsensors, with on-chip interface circuitry, are currently replacing discrete sensors due to their inherent advantages, namely, low cost, high reliability and on-chip processing. To accomplish small, robust and inexpensive microsystems, it is desirable to integrate the soil moisture sensor with digital signal processing and wireless front-end. Therefore, this microsystem can be installed near plants roots and at several depths for measuring real plant water needs.

2. System overview

The complete system is divided in two blocks, as depicted in Fig. 1, the soil moisture sensor and the mixed-signal interface.

The soil moisture sensor, developed in a previous work [2], is based on the dual-probe heat-pulse (DPHP) method,

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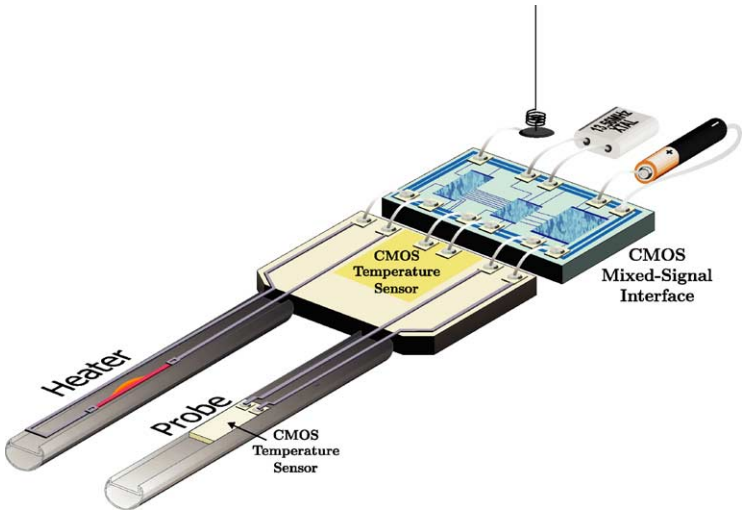

Fig. 1. System overview.

where a heater is placed in one rod and in the other one there is an integrated temperature sensor. A special package allows its implementation near plants roots. After applying a heat pulse for a fixed period of time, the maximum temperature rise, that is a function of the soil moisture, is measured in the opposite rod. The differential output of the temperature sensor is then amplified and applied to the mixed-signal interface.

The implemented CMOS mixed-signal interface, outlined in Fig. 2, basically comprises a second-order $\Delta\Sigma$ modulator, implemented using switched-capacitor techniques in a fully-differential topology, and a RF transmitter. The output of the modulator is applied to a counter as a first-order decimation filter and the result is latched. Prior to transmission, the latched data is assembled in a frame containing preamble and error-check control fields. Afterwards, data is encoded as a pulse-width modulated signal and transmitted by means of an amplitude-shift keying modulation through a power amplifier operating in class-E mode. The 433.92 MHz carrier is generated by the on-chip phase-locked loop (PLL).

3. Mixed-signal interface

The soil water content should be measured with a resolution better than 1%. The soil moisture sensor has a sensitivity of about $3.5\,\text{mV}\,^{\circ}\text{C}^{-1}$ or 6.825 mV per unit of volume change in water content for a heat strength of $400\,\text{J}\,\text{m}^{-1}$. Signal bandwidth is typically a few Hertz.

3.1. Analog section

Previous studies [3–5] have showed that a second-order $\Delta\Sigma$ modulator is a suitable architecture for converting low-frequency signals to the digital domain. The second-order architecture is preferred to the simpler first-order one because it is less sensitive to the correlation between the input and the quantization noise, which reduces the presence of pattern dependent noise for certain dc input signals [6]. Higher-order architectures may exhibit stability problems and normally are more area consuming designs. To achieve 16 bit performance in a single-bit, second-order

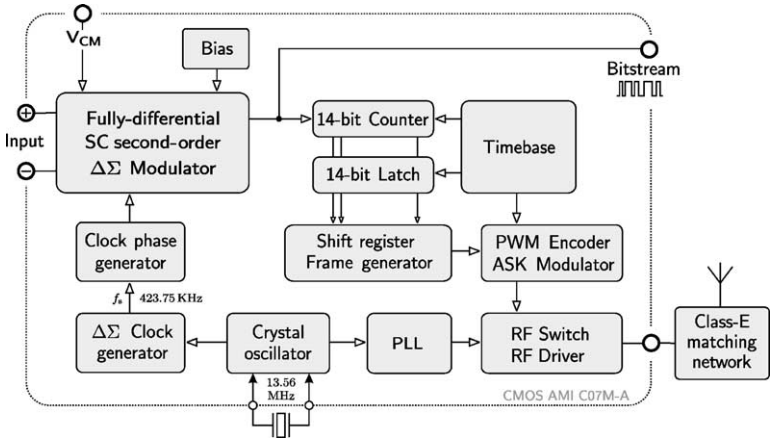

Fig. 2. Mixed-signal interface architecture.

architecture, the oversampling ratio (OSR) must equal at least 153, considering only quantization noise. To keep OSR a power of 2 and to accommodate other sources of noise, the OSR was chosen as 256. In order to ensure that the system will accommodate other sensors with eventually larger bandwidths, the modulator was dimensioned to have a 500 Hz bandwidth, which for this case results in a clock frequency of 256 kHz.

The second-order $\Delta\Sigma$ modulator has been implemented using switched-capacitor techniques. In addition to robustness of these techniques, the use of a fully-differential topology minimizes common-mode interference, switch charge injection and clock feedthrough. Additionally, the differential architecture doubles the dynamic range of the modulator. The two integrators are based on fully-differential folded-cascode amplifiers biased by a constant-g_m wide swing circuit. Also, for reducing the influence of the first-amplifier offset and low-frequency noise, a chopper scheme has been implemented. The modulator reference is external and set to 1.23 V (differential). The complete $\Delta\Sigma$ modulator is shown in Fig. 3.

The dominant sources of error in the $\Delta\Sigma$ modulator are quantization and thermal noise. A clock frequency of 423.75 kHz with an oversampling ratio of 256 was chosen to make the quantization noise insignificant. This results in an input signal bandwidth of about 830 Hz which is fair above the requirement. Thermal noise is essentially determined by the size of sampling capacitors, which are in this case 6 pF.

The amplifiers used in the $\Delta\Sigma$ modulator are based in a fully-differential folded-cascode topology. Since thermal noise is a major concern in the input stage, a NMOS-input topology was preferred to a PMOS-input one because PMOS transistors generate more thermal noise (for the same dimensions and current). Also, the higher transconductance of the NMOS devices improves dc gain, reducing harmonic (mainly second) distortion. The higher flicker noise associated to the NMOS transistors is reduced by the chopper action. Input transistors were chosen to be large enough ($W/L = 457\,\mu m/4.4\,\mu m$) to minimize systematic offset by employing matching techniques.

$\Delta\Sigma$ modulators exhibits low sensitivity to the errors induced during internal quantization. In our case, having a single-bit (two-level) quantization which is inherently linear, errors are limited to offset and hysteresis. For a second-order modulator, the offset is attenuated by A_V^2, where A_V is the amplifier open-loop, low-frequency gain. The hysteresis, an indeterminate output state for small input values, is also attenuated by the high dc-gain of the integrators. These performance requirements lead to a simple solution based on a clocked comparator followed by a NOR SR flip–flop with minimum size transistors to reduce resolution time, and thus, the loop delay.

Due to the existence in the same substrate of analog, digital an RF signals, the layout of the analog section of the prototype was one of the most critical phases. In order to optimize performance the layout was manually routed. The $\Delta\Sigma$ modulator layout is completely symmetrical, and all transistor and capacitors have been laid using common-centroid techniques. Due to the presence of RF signals, the analog section is also surrounded by a n-well isolation diffusion. Overlapping between analog and digital traces was also avoided.

3.2. Digital section

The output of the modulator is applied to a counter as a first-order decimation filter. A timebase circuit generates a latch signal every 2^{14} clock pulses corresponding to 38.6 ms time interval. After a clock cycle, a reset counting signal is issued to clear the counter value, as depicted in Fig. 4.

For each counting, a 14 bit sample is generated, stored and transmitted. Prior to transmission, data is encoded in

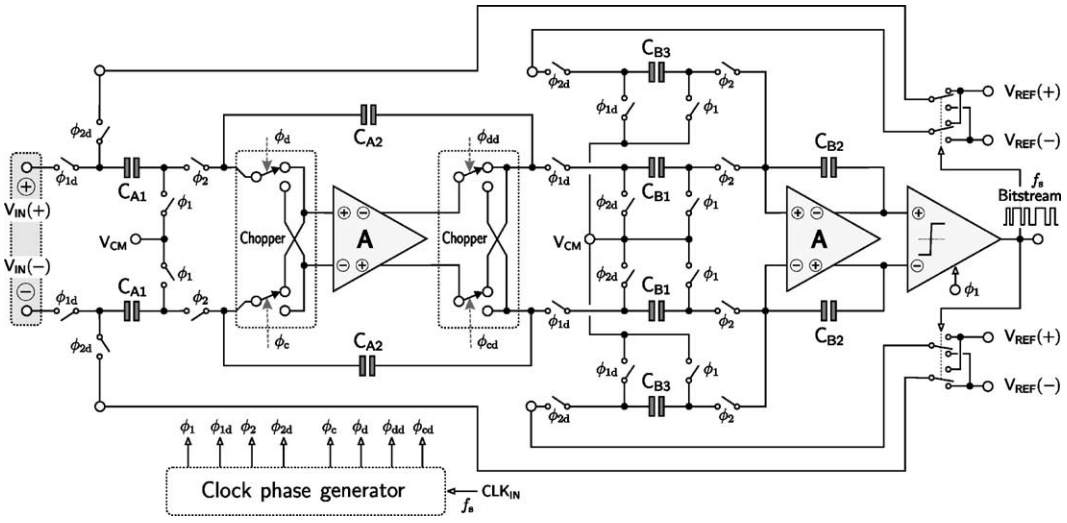

Fig. 3. Fully-differential implementation of the second-order $\Delta\Sigma$ modulator.

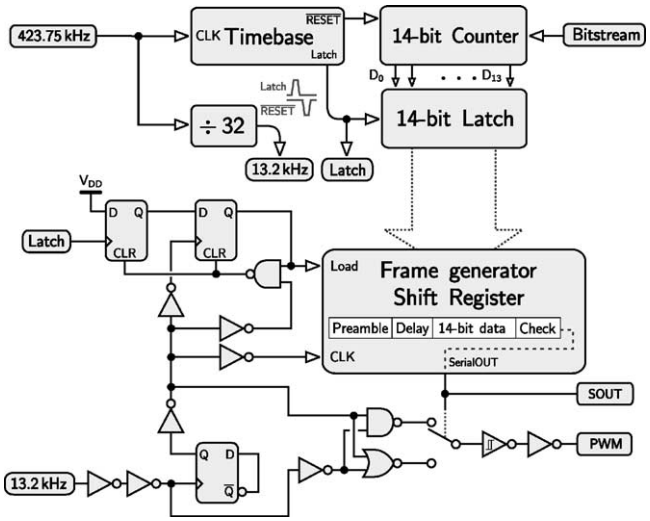

Fig. 4. Digital section of the interface.

pulse widths of 25 and 75% duty-cycle representing the logic levels 0 and 1, respectively. For error detection and receiver synchronization purposes, data is assembled together with a 12 bit preamble and a 4 bit checksum. The assembled frame has a 30 bit length and takes 4.53 ms to be transmitted with a bit-rate of about 6.6 kbps.

3.3. RF transmitter module

The RF transmitter module, schematically represented in Fig. 5, is composed of a crystal-controlled frequency synthesizer and a RF transmitter operating in class-E mode. The class-E power amplifier (PA) is a high-efficiency switching amplifier based on a NMOS transistor as switch RF switch, and a load network (L_{dc}, C_1, C_2, and L) that avoids the simultaneous imposition of substantial voltage and substantial current on the switch [7], yielding highly efficient operation.

FSK and PSK modulation schemes, being less prone to errors, and thus more robust, could be considered as the desired solution. However, due to ASK simplicity and the goal of ensuring compatibility with other modules in the system [8], ASK was the adopted scheme. Furthermore, ASK modulation requires less channel bandwidth than FSK. By using ASK, where the carrier is switched on and off, carrier frequency generation circuit can be relaxed. In this way, and to ensure carrier stability, the frequency synthesizer was implemented as a classical phase-locked loop (PLL) using a 13.56 MHz crystal reference oscillator. This commercially available crystal unit provide both the carrier signal (just by multiplying the original signal by 32 using the PLL) and the $\Delta\Sigma$ modulator clock signal (by dividing it by 32).

The PLL consists of a phase-frequency detector (PFD), a charge pump (CP), a third-order passive loop filter, a current-starved voltage-controlled oscillator (VCO) and a fixed divider, as shown in Fig. 6. The phase-frequency detector identifies phase and frequency differences between the reference and the divider signals. With the charge pump and loop filter these differences are converted into a control voltage to adjust the output frequency of the VCO.

The phase-frequency detector generates two signals, Up and Down, that controls the charge pump to charge and discharge the loop filter equivalent capacitance. Special care

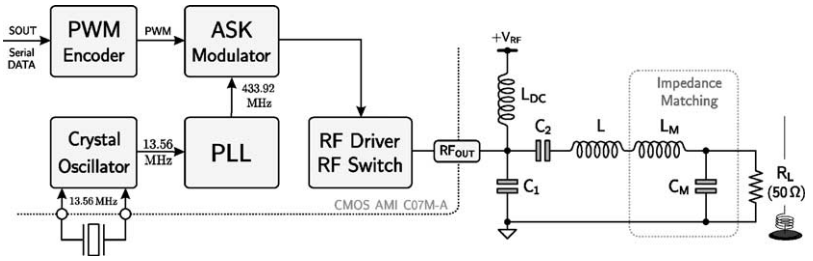

Fig. 5. Transmitter module diagram.

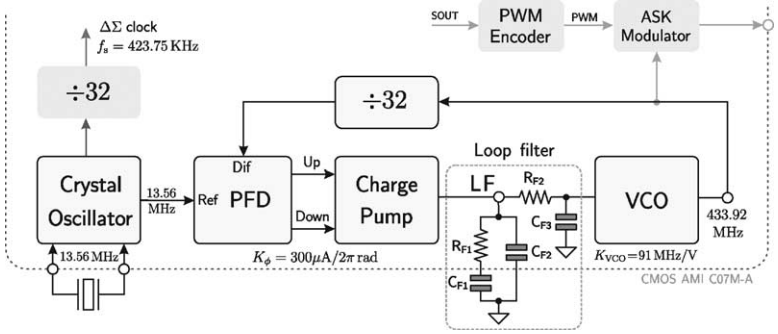

Fig. 6. Phase-locked loop block diagram.

has been taken to avoid overlapping between these signals that leads to a short circuit in the charge pump. Also, a delay was inserted in the path of reset signal to eliminate the dead-zone problem [9] thus reducing the phase noise of the PLL.

In a conventional CMOS charge pump, the switches controlled by the Up and Down signals are directly connected to the output node. When one of the switches is turned on, the total charge in the loop filter equivalent capacitance, will be shared with the switch parasitic capacitance. This induces glitches in the charge pump current which increases spurs in the PLL output signal [10]. In the implemented charge pump, Up and Down signals are used to switch on and off a current mirror with current matching, thus avoiding charge sharing in the CP output node. The charge pump current was designed to be 300 μA.

The third-order passive loop filter comprises an off-chip second-order filter section (R_{F1}, C_{F1} and C_{F2}), connected to the LF pin and an internal RC section (R_{F2} and C_{F3}) providing an extra pole to assist the attenuation of the sidebands at multiples of the comparison frequency (spurs) that may appear. The resulting PLL is commonly referred as type-2, fourth-order loop which provides great noise suppression in the PLL output spurious level [11].

The VCO is based in the current-starved configuration with five delay stages. To avoid the problem of locking on harmonics of the desired output frequency, the maximum output frequency has been limited. Output frequency range is between 330 and 500 MHz. The 433.92 MHz carrier frequency is approximately the VCO center frequency and is obtained for an input voltage of about 2.15 V, as seen in Fig. 7. The VCO constant, K_{VCO}, is approximately 91 MHz V^{-1}.

Fig. 8 shows the simulated VCO input voltage waveform. PLL loop bandwidth is 500 kHz, and the loop filter values used were $R_{F1} = 3.9\,k\Omega$, $C_{F1} = 220\,pF$, $C_{F2} = 12.2\,pF$, $R_{F2} = 33\,k\Omega$ and $C_{F3} = 1.5\,pF$. The PLL has a simulated lock time of about 6 μs. Fig. 9 shows a transient simulation of the RF output signal, in a 50 Ω load, with its driving signal.

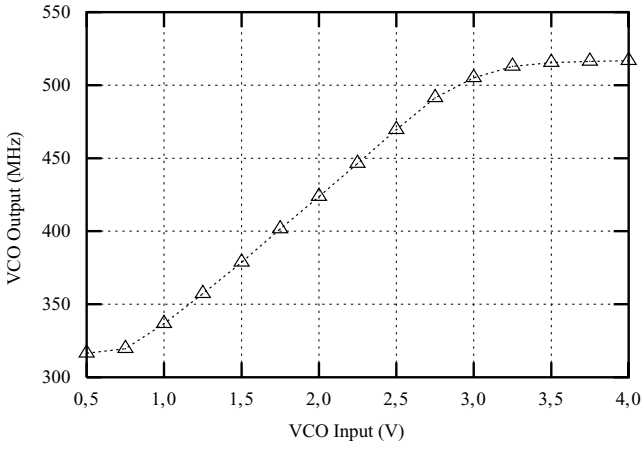

Fig. 7. Simulated VCO transfer function.

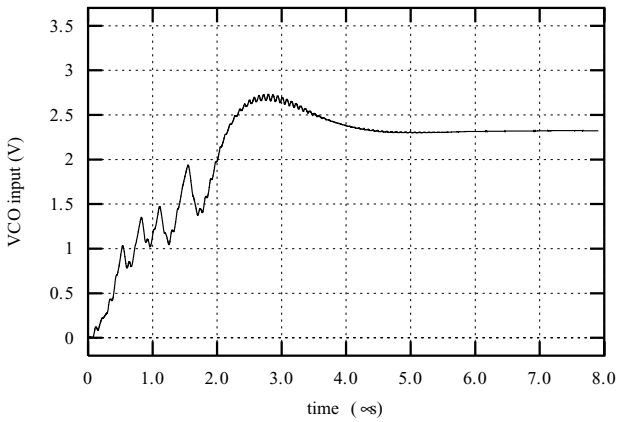

Fig. 8. VCO input voltage transient simulation.

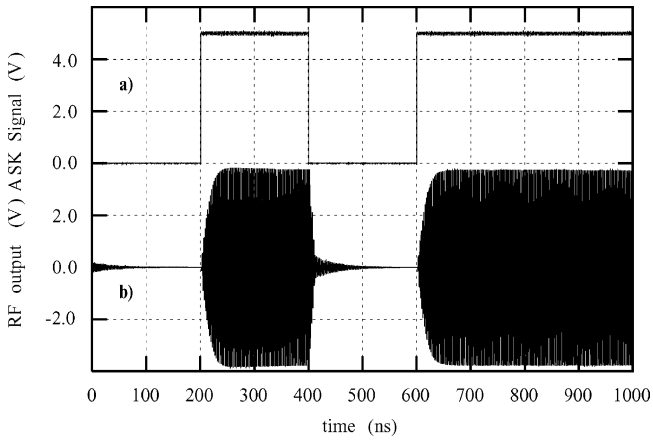

Fig. 9. (a) ASK driving signal and (b) PA RF output (50 Ω load).

4. Results

The mixed-signal interface has been fabricated in a standard CMOS 0.7 μm process from Europractice IC service (C07M-A, *n*-well, 2 metals and 1 poly). The ΔΣ modulator is seen in the upper half of the die photograph shown in Fig. 10. The switched-capacitor integrators have been laid-out symmetrically about the spine of the modulator, that in this case is the common-mode voltage trace. The total die area is 3.79 mm^2.

The interface was characterized by evaluating the ΔΣ modulator and the RF section performance. Since the modulator clock input and bitstream are accessible from the outside, the modulator can be independently tested. The same bitstream is applied to the digital section for frame generation and transmission. The RF transmitter was evaluated by transmitting 14 bit data that corresponds to the digital filtering of the bitstream.

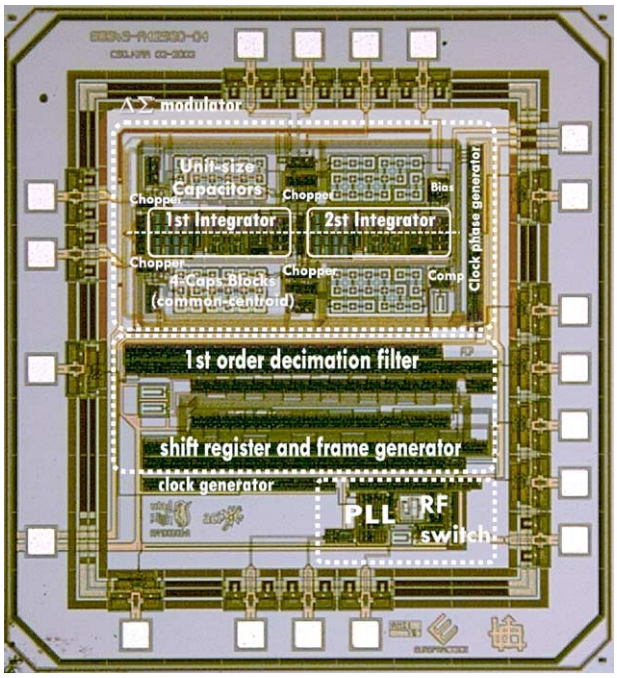

Fig. 10. Microphotograph of the implemented prototype.

4.1. ΔΣ modulator performance

The performance of the modulator was evaluated by driving its input with a precision sinusoidal signal source and acquiring its bitstream output to a personal computer for subsequent processing. The digital filtering and decimation were performed using MATLAB™.

Simulations taken from the extracted layout have shown a dynamic range (DR) of 103.36 dB (effective resolution of about 17 bit) for the ΔΣ modulator. However, other sources of error were not taken in consideration. The predicted quantization noise power, P_Q, is −112.28 dB below full-range input signal power. Thermal noise contribution, P_{TH}, mainly due to the 6 pF sampling capacitors, is −115.57 dB and incomplete settling error in the first integrator, P_{ST}, is −108.87 dB below full-range input signal power.

Fig. 11 shows the measured signal-to-(noise + distorsion) ratio (SNDR) as a function of the input sine wave amplitude. An input level of 0 dBV represents a sine wave whose peak-to-peak amplitude equals the spacing between the two levels of the D/A converter. The frequency of the input sine wave was 100 Hz and the modulator sampling rate was 423.75 kHz, with an OSR of 256. The dynamic range is 98.7 dB giving an effective resolution of 16.1 bit. The measured SNDR is 95.2 dB.

The baseband spectrum of the modulator for an input of −20 dBV at 200 Hz is shown in Fig. 12. As we can see, a tone of 50 Hz is present due to insufficient power line frequency rejection. This tone was injected through the acquisition board used to capture the bitstream. Distortion (mainly of second-order) is also present. It was verified that the level

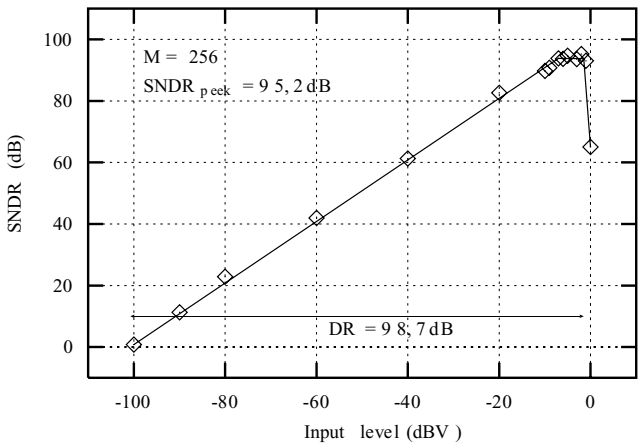

Fig. 11. Measured SNDR for a sine input of frequency 100 Hz and variable amplitude, with OSR = 256.

of such harmonic is very sensitive to the configuration of the measurement set-up, so probably it is not caused by the modulator itself. As expected, the flicker noise was attenuated by the chopper operation. The lobes in this low-frequency zone, that represents the offset of the modulator, are due to the limited resolution of the FFT.

Fig. 13 shows the output of the modulator when differential inputs are connected to the common-mode voltage, which corresponds to a zero differential input. Considering that the bitstream takes the values −1 and 1, the average value of the bitstream is zero, as depicted in Fig. 13(a). In the Fig. 13(b) is depicted the effect of the quantization error in the output of the modulator.

4.2. RF transmitter performance

For evaluation of the RF transmitter, the bitstream was applied to a 14 bit counter (as a first-order digital decimation filter) and afterwards, packed and transmitted through a RF power amplifier operating in class-E mode. In this

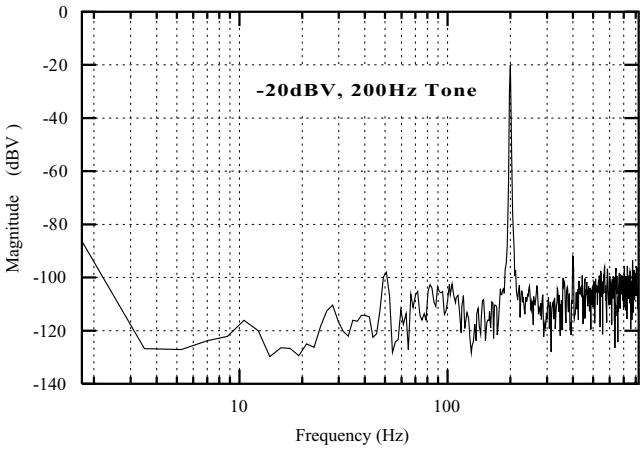

Fig. 12. Measured output spectrum for a sinusoidal input of amplitude −20 dBV and frequency 200 Hz.

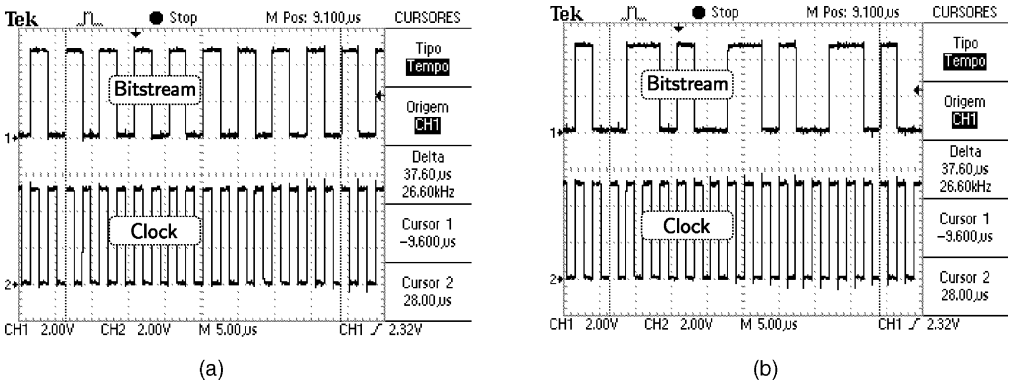

Fig. 13. Clock and bitstream output of the modulator: (a) ideal case for zero output; (b) with quantization noise.

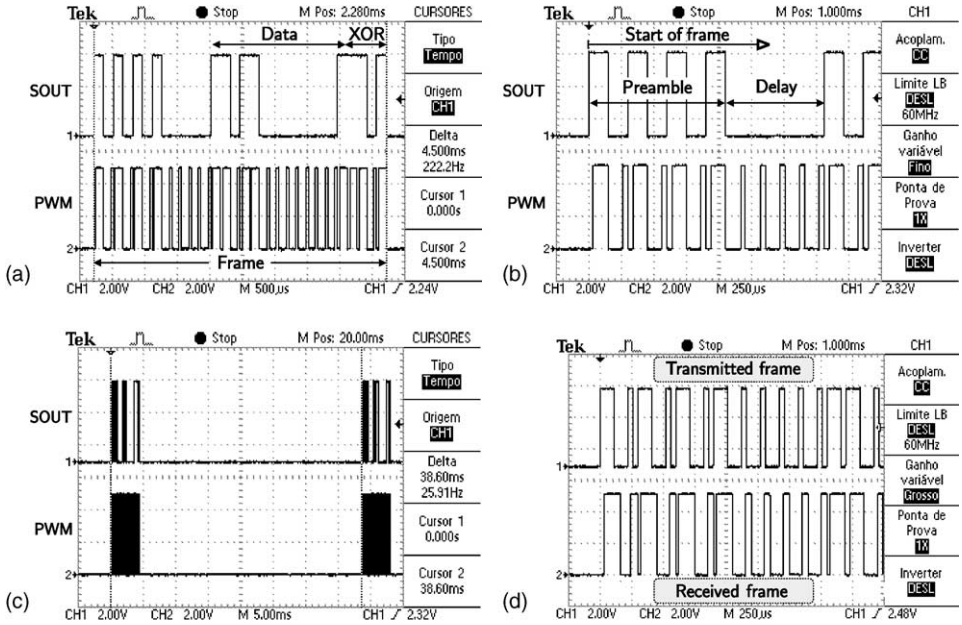

Fig. 14. Frame transmission waveforms: (a) complete frame; (b) detail of the beginning; (c) two consequent frames and, (d) transmitted and received frame.

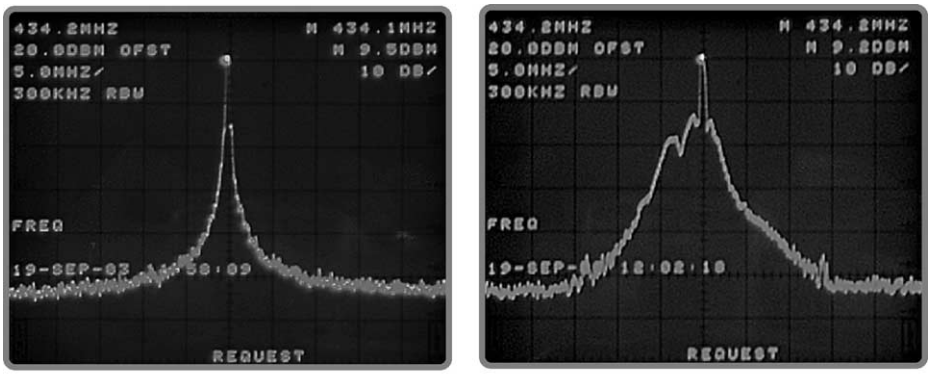

Fig. 15. Measured output spectrum of the RF transmitter (10 dB/div. vertical scale, 5 MHz/div. horizontal scale and 300 kHz resolution bandwidth): (a) only carrier; (b) carrier modulated by the PWM encoded signal.

Table 1
Summary of the measured mixed-signal interface performance

Parameter	Value
Area $(mm)^2$	1.86×2.04
Power supply (V)	5.0
Total power consumption (mW)	30.3
$\Delta\Sigma$ Modulator	
Oversampling ratio (OSR)	256
Sampling frequency, f_S (kHz)	423.7
Dynamic Range, DR (dB)	98.7
Reference (differential), V_{REF}, (V)	1.23
Effective resolution (ENOB) (bit)	16.1
SNR_{peek} (dB)	95.2
RF transmitter	
Output power (50 Ω load), (dBm)	11.5
Power conversion efficiency (%)	61
Range (m)[a]	>50

[a] With a commercial receiver unit (LM-RXAM2433 from LPRS, Ltd.).

case, the sample rate is approximately 25 samples per second (38.66 ms) for a clock frequency of 423.75 kHz. In this prototype, the power amplifier matching network is off-chip for tuning purpose Fig. 14 shows some waveforms related to frame transmission. Fig. 14(a) shows an entire frame before (SOUT) and after (PWM) encoding, while in Fig. 14(b) is shown the beginning of frame. Fig. 14(c) shows two consequent frames. After encoding, the PWM signal is applied to the ASK modulator and transmitted. Fig. 14(d) shows a transmitted frame (upper side) and the received frame (lower side) by a commercial receiver unit (LM-RXAM2433) from LPRS, Ltd.

The measured output spectrum of the transmitted signal is shown in Fig. 15. The power of the carrier was measured by connecting a cable directly to a Tektronic 2710 Spectrum Analyser. Cable attenuation of about 2.0 dB was determined using the spectrum analyser tracking generator. The measured carrier power of 9.5 dBm corresponds to transmitted power of approximately 11.5 dBm (14.1 mW). The center frequency is about 434.2 MHz, slightly different from the expected value due to a mistuning of the crystal oscillator.

Table 1 summarizes the measured performance of the mixed-signal interface.

5. Conclusions

In this paper a wireless CMOS mixed-signal interface for a soil moisture sensor has been presented. The experimental prototype has demonstrated that a second-order $\Delta\Sigma$ modulator is a suitable choice for acquiring low-frequency sensor data due to their simplicity, stability and robustness. The achieved performance may be expanded if a higher oversampling ratio is used to further suppress quantization noise and noise tones. Flicker noise at the input of the modulator has been reduced by the chopping action. However, thermal noise reduction is a more difficult task, and is a common problem in high-resolution CMOS A/D converters. Sampling frequency and oversampling ratio should be tailored to a specific sensing application to achieve the desired performance.

Some enhancements are now being carried out, such as a receiver, among others. With bidirectional communications capabilities, it will be possible to implement a wireless network of soil moisture sensors for smart irrigation control systems.

Acknowledgements

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Biographies

Raul Morais graduated in electrical engineering at University of Trás-os-Montes and Alto Douro (UTAD), Portugal in 1993. He obtained the MSc degree in Industrial Electronics in 1998 at University of Minho, Portugal. He is a PhD student at UTAD, Portugal. Since 1994, he has been a lecturer in the Engineering Department, UTAD, Portugal. He is a

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