SENSORS AND ACTUATORS A PHYSICAL

Single-chip CMOS optical microspectrometer

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Abstract

Numerous applications, e.g., systems for chemical analysis by optical absorption and emission line characterization, will benefit from the availability of low-cost single-chip spectrometers. A single-chip CMOS optical microspectrometer containing an array of 16 addressable Fabry–Perot etalons (each one with different resonance cavity length), photodetectors and circuits for read-out, multiplexing and driving a serial bus interface has been fabricated. The result is a chip that can operate using only four external connections (including V_{dd} and V_{ss}) covering the visible spectral range of the spectrum with FWHM = 18 nm. Frequency output and serial bus interface allow easy multi-sensor, multi-chip interfacing using a microcontroller or a personal computer. Power consumption is 1250 μW for a clock frequency of 1 MHz. © 2000 Elsevier Science S.A. All rights reserved.

Keywords: On-chip optical microspectrometer; Microinterferometer; Fabry–Perot etalon; Light-to-frequency converter; Internal/external bus interface

1. Introduction

Conventional benchtop spectrometers involve a complex system of lenses and moving parts (or a high-density photodetector array), and are thus bulky and expensive. By applying micromachining techniques one can produce a spectrometer with drastically reduced size and costs (in high-volume production). In addition, a number of these systems can be combined for improved spectral range and/or resolution. Moreover, an integrated optical device has a number of advantages over a conventional optical system, such as a simplified assembly, stable alignment, and compact size. The dimensional advantage of a miniaturized spectrometer is, in many applications, of higher importance than its reduced resolution.

Examination of products in a manufacturing line by means of laboratory analysis is time consuming, increases costs and sometimes stops production. Therefore, it has become important to perform on-line measurements in the process line in order to correct any process problems in real time. A small spectrometer has huge potential to serve the needs of future automated optical inspection systems.

Identification of the composition of gases and liquids, chemical analysis by optical absorption, emission-line characterization, colorimetry and biochemical analysis are some of the applications where a miniaturized spectrometer can be useful.

Previously developed microspectrometers, fabricated using bulk or surface micromachining, contain movable parts to perform wavelength tuning [1,2]. As a result, these are less reliable and suitable only for operation in a limited spectral band (mostly near-IR) [3,4]. Moreover, high-voltage electrostatic actuation is necessary for resonance cavity tuning. In this paper a fully integrated array-type single-chip microspectrometer with a light-to-frequency converter and a bus interface is presented.

2. Single-chip CMOS microspectrometer

2.1. Array-type microspectrometer

When a spectroscopic measurement is performed, each of the spectral components must be measured individually. Two basic approaches can be used:

(a) sequential measurement using scanning techniques.
(b) parallel measurement based on an array of detectors.

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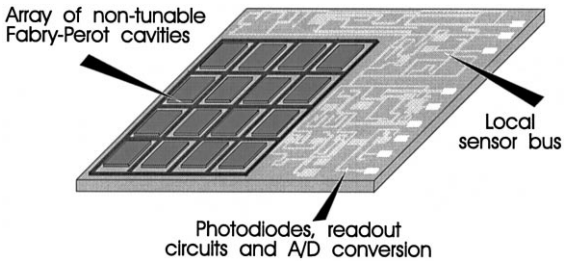

Fig. 1. A single-chip optical microsystem based on an array-type spectrometer of Fabry–Perot etalons integrated with photodiodes underneath the 16 etalons; read-out electronics, and the bus interface.

In the scanning-type spectrometer, measurement is performed in a time sequence. Two configurations are possible and both are used in practice. When the relative position of the input light beam is considered to be fixed, then, at a certain position of the wavelength-selecting element (WSE) relative to the detector, the first spectral component is measured. Subsequently, the relative position of the WSE with respect to the detector is slightly changed and the next spectral components are measured. Rotation of the WSE over a well-defined angle enables scanning and recording of the entire spectrum. Alternatively the photodetector can be moved to scan across all spectral components.

In the array-type approach, the measurement is performed in parallel. This means that a large array of detectors is required. Each of them measures one spectral component. The number of detectors or channels used can be a limiting factor for the resolving power. In contrast to the previous approach no mechanical scanning is required and, therefore, array-type systems are suitable for high-speed measurements. In practice, one WSE and an array of detectors is used in commercially available systems. As will be shown, combining an array of WSEs and detector is a very interesting option in a microspectrometer.

The single-chip CMOS microspectrometer uses fixed-cavity Fabry–Perot etalons with optical quality and long-term stability much higher than tunable devices [1,2]. An array of detectors is needed to cover a large optical spectral range with high resolution. Therefore, the single-chip microspectrometer contains an array of 16 addressable Fabry–Perot etalons with the respective photodetector underneath each of these (see Fig. 1).

2.2. Fabry–Perot etalon

CMOS postprocessing consists of depositing an $Al/SiO_2/Ag$ layer stack on top of each photodiode after the CMOS process has been completed (integrated-circuit fabrication). This stack functions as a tuned Fabry–Perot resonance cavity. Compatibility with a CMOS process is required, also the photodiode should be fabricated in a CMOS process. Fig. 2 shows the Fabry–Perot etalon structure plus the photodiode.

2.3. The photodiodes

Each Fabry–Perot etalon has an associated CMOS photodetector. The photodetectors have been realized in a conventional 1.6 μm n-well CMOS process. In an n-well CMOS process, three different types of photodiodes and one vertical phototransistor are available [5]. The three different photodiodes result from the n-well/p-substrate junction, the n-well/p-diffusion, and the p-substrate/n-diffusion junction. The device used for photodetection is the vertical pnp phototransistor (Fig. 2), with the deep junction formed by the p-epilayer and the n-well, and the shallow junction formed by the n-well and a p+ implanted layer that is normally used for the drain/source contacts (sp). Both junctions are connected in parallel and operate at reverse bias. The upper junction contributes little to the generated photocurrent, especially at long wavelengths. Because of its large capacitance per area, this junction is mainly used for photocurrent integration. The sensors are arranged in a 4×4 array of square photodiodes with an active area of $500 \times 500\ \mu m^2$ each. A typical dark current of 30 fA (12 pA/cm^2) was measured with both junctions reverse biased at 5 V in parallel.

Cross-talk reduction techniques are implemented (good isolation per each individual channel) so that the operating current comes only from the photocarriers generated in or near the depletion layer between the p-diffusion/n-well junction. The utilization of the three-layer photodiode is an effective approach to improve photodiode performance (high-sensitivity).

2.4. Read-out electronics

Low-noise read-out of photodiodes [6] has been implemented to cover a 10^5 dynamic range of light intensity level. The photocurrent-to-frequency circuits developed feature a dynamic range of sensitivity that is comparable to that of more complex analog circuits commercially available [7].

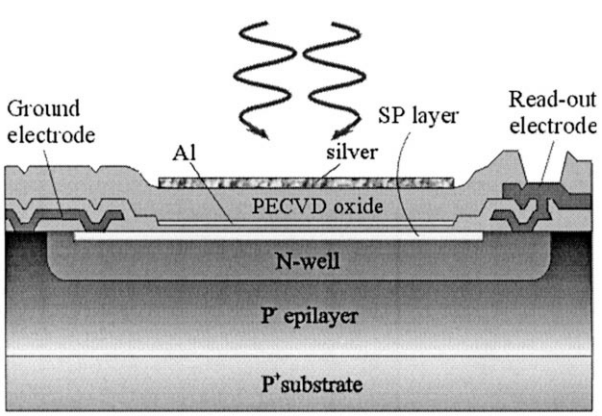

Fig. 2. A CMOS Fabry–Perot etalon with the photodiode underneath: a cross-section.

Fig. 3 shows the block diagram of the read-out circuit. Operation is based on a charge balancing technique, the voltage over the photodetector continuously varies from the reference level, V_{dd}, to the reference voltage, V_{ref}, of the comparator.

The capacitances of the lower and upper junction of the 500×500 mm^2 photodiode have been found from the measured CV curves: $C_{jl0} = 19.5$ pF and $C_{ju0} = 130$ pF, respectively. A CMOS bandgap reference [2,3] is used so $(V_{dd} - V_{th})$ equals 2.48 V. The output frequency equals two charge and discharge cycles, where each discharge equals one period of the clock (see Fig. 3). Since the clock frequency is much higher than the oscillator frequency, the relation between the photocurrent and the output frequency becomes:

$$f_0 = \frac{1}{2t_d + 2t_c} \approx \frac{1}{2t_d} \approx \frac{I_{ph}}{2\Delta Q}.$$

The sensitivity of the current-to-frequency conversion is linear and can be calculated as $S_{if} = f_0/I_{ph} = 1/(2\Delta Q)$. With ΔQ, the variation of the charge across the two junctions, depending on the junction capacitances of the photodiode. The total light-to-frequency conversion factor is given by the product of S_{if}, the spectral responsivity of the photodiode and the transmittance of the Fabry–Perot filter.

Only one photodiode can be connected to the comparator at a time using multiplexer S_1–S_N. At a voltage V_j lower than V_{ref}, the comparator output remains at a high logic level and, after synchronization with the clock, closes switch S_{ch}, which forces the photodiodes to be quickly charged during one clock period to V_{dd}. When this switch opens again, the photocurrent discharges the junction capacitance C_{jl} and C_{ju}, until the comparator detects $V_j < V_{ref}$, which causes the cycle to repeat. The flip-flop chain divides the signal by two, resulting in a symmetrical output signal that can be transferred to the bus via a buffer.

Basically, the photodiode read-out circuit can be considered a first-order (or relaxation) oscillator circuit and, since the circuit has only one pole (or frequency controlling element), it can be tuned over a very wide range [8]. The charge generated by the photoelectric effect directly modulates the charge in the integrating junction capacitance, thereby modulating the output frequency.

The charging switch S_{ch} is based on a complementary pair with equal-size PMOS and NMOS transistors to minimize capacitive charge injection at high oscillation frequencies. The currents in the multiplexer switches S_1–S_N are sufficiently low to allow a relatively high channel

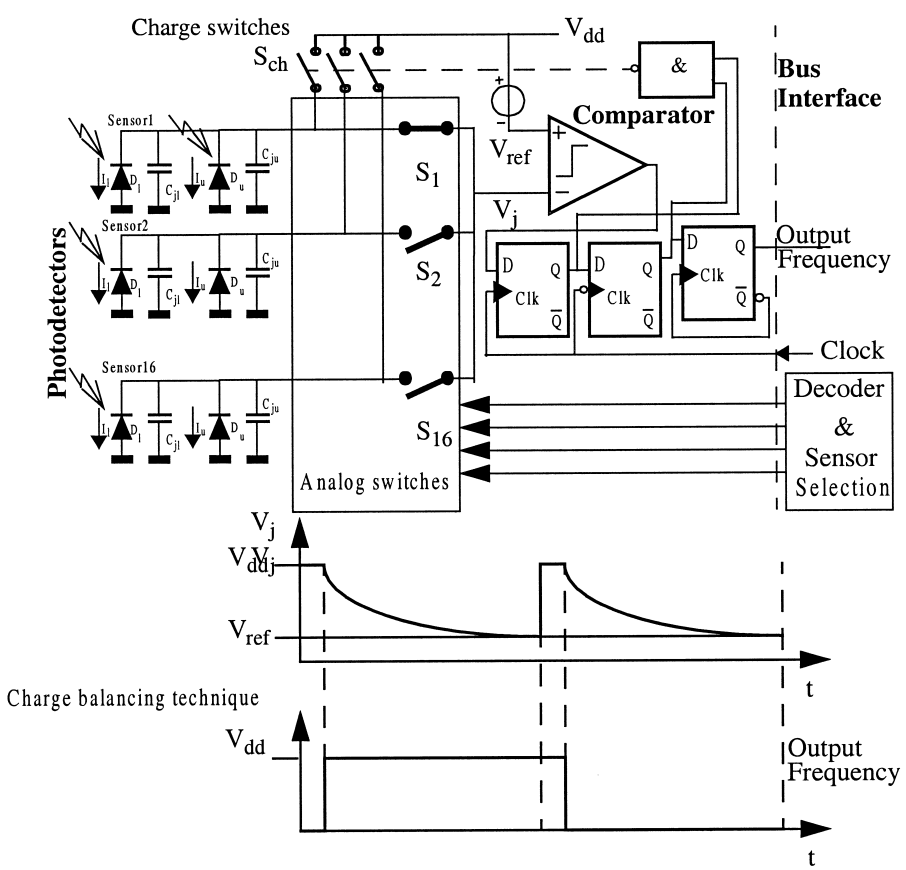

Fig. 3. Photodiode-read-out circuits.

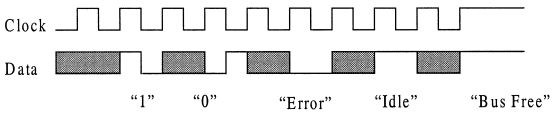

Fig. 4. Manchester encoding scheme.

''on'' resistance. The leakage current in the ''off'' state should be neglected compared to the dark current of the diode. The channel of these MOS transistors has a W/L of 2 μm/16 μm.

2.5. Bus interface

The upgraded version of the Integrated Smart Sensor (ISS) bus interface [9] is based on a single controller to coordinate the activity on the bus and is characterized by a maskable interrupt mechanism, calibration facilities, small size, and low power consumption, which makes it very suitable for integration with optical sensors.

Apart from simplicity, the improved ISS bus interface has two convenient features, which makes it very suitable for an optical microsystem. First, analog data can be transferred over the bus. Data generated by a sensor with limited signal-processing capability are usually analog, so this requirement is necessary, but is not present in the usual standard interfaces, which are designated to interconnect only digital subsystems. Secondly, the use of the Manchester encoding scheme for transmission of the data at the logical level adds further flexibility. In such a scheme, the clock is embedded into the data allowing four logical levels instead of two (see Fig. 4).

The physical structure consists of two wires, a data line and a clock line, both open drain driven. The data line allows half-duplex communication between the modules connected to the bus. In order to increase flexibility, we added a second data line to be used only for duplex transmission (e.g., for on-line sensor calibration or a testing procedure).

For use in embedded systems, particularly for instrumentation systems, sensor modules should also be able to signal announce to the controller when data is available, or more generally, when some particular event has happened. In the realized interface this flexibility is obtained by adding an interrupt request and a service request protocol.

An interrupt request message, if it is not disabled by the configuration used for that particular module, can be sent over the bus at any moment, even if the controller is in the middle of another conversation. A service request on the other hand, is allowed only if the bus is in the idle state. All messages excluding the request messages are initiated by the controller.

Fig. 5 shows the block diagram of the bus interface. A third bus line is used to put the frequency output after the light-to-frequency conversion on the bus (the simplest version of the bus interface uses only the clock line and data line). Also, the use of a different clock signal for the light-to-frequency conversion instead of the clock signal of the bus (SCL line) is allowed.

3. Device fabrication

The electronic circuits and photodetectors were realized in a conventional double-metal, single-polysilicon 1.6 μm n-well CMOS process. After completion of the standard CMOS process, but omitting the last silicon nitride deposition step for scratch protection (Fig. 6a), a postprocessing module was used to build the Fabry–Perot etalons on top of the photodetectors. These etalons consist of a thin-film stack (silver/PECVD oxide/aluminum). Fig. 6 presents a complete description of all CMOS postprocessing sequence steps.

The photodetector was formed in the n-well, located in the p-epilayer, by means of shallow boron implantation. Since the oxide layer on top of the photodiode is rather thick right after the CMOS process, this oxide layer was

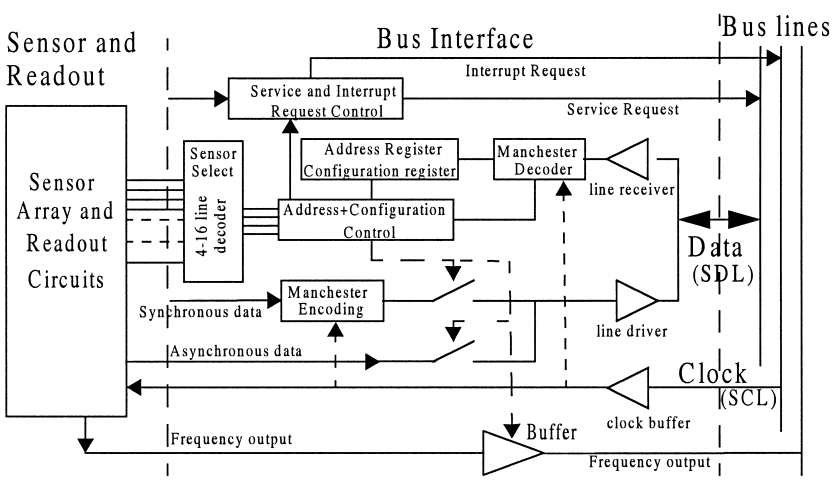

Fig. 5. Block diagram of the bus interface.

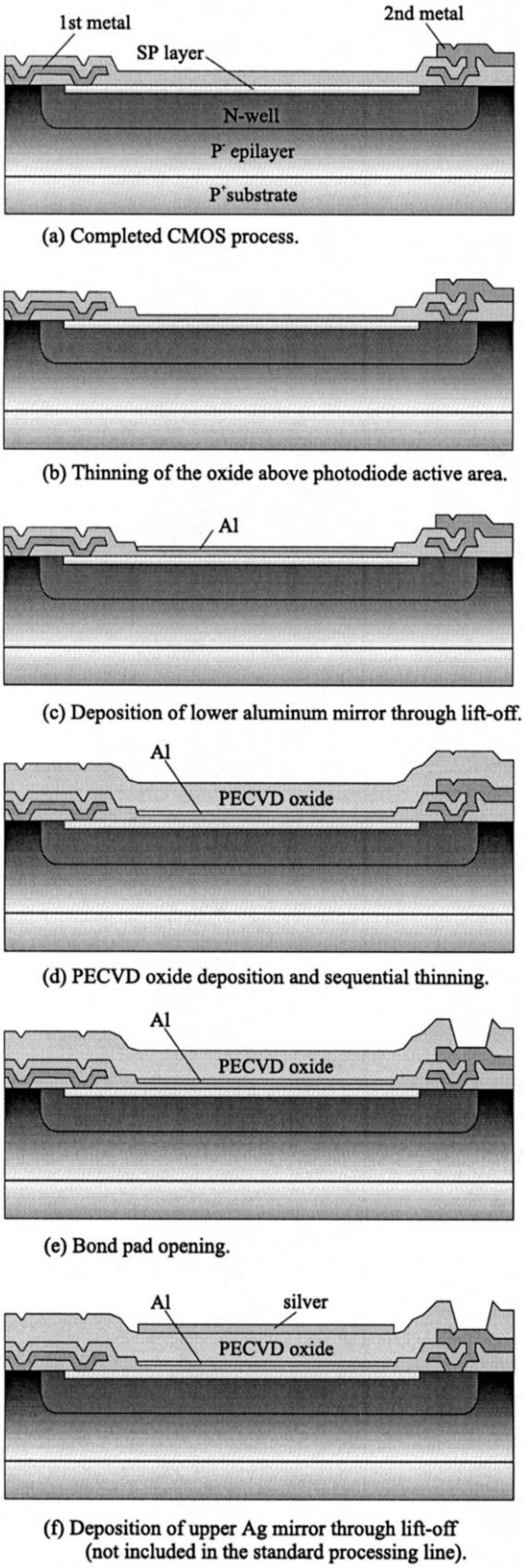

Fig. 6. CMOS postprocessing fabrication sequence.

thinned to 50 nm to minimize the effect of the oxide layer on the transmittance (Fig. 6b).

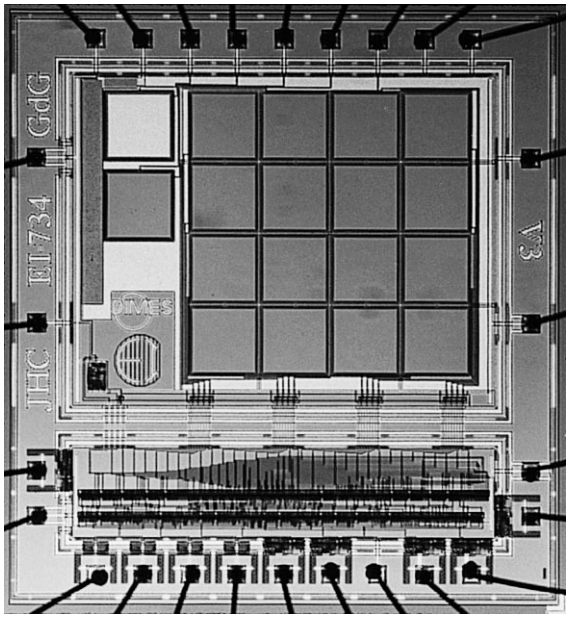

Fig. 7. A photograph of the single-chip CMOS optical microspectrometer.

The formation of the Fabry–Perot etalon starts with the deposition of a 20-nm Al layer after completion of the CMOS process (including metallization and thinning of the oxide above the photodiodes). The thin Al layer is evaporated and patterned using lift-off (Fig. 6c). Subsequently, a PECVD oxide layer is deposited with a thickness equal to the maximum cavity length (Fig. 6d). The thickness of the PECVD silicon dioxide layer, which is enclosed in between two semi-transparent metallic mirrors (Fig. 6f), determines the wavelength for tuning. In N subsequent plasma etching steps (for which different photoresist masks are used), the initially deposited PECVD oxide layer is thinned to form 2^N channels, each with a different resonance cavity length.

A photograph of the completed chip is shown in Fig. 7. The die measures 4.2×3.9 mm. The analog circuits can be seen in the upper part: a sensor array, analog switches, a test diode, a metal-covered diode (for dark-current compensation), a reference circuit, a reference capacitor, and a comparator. The lower part holds the bus interface, the

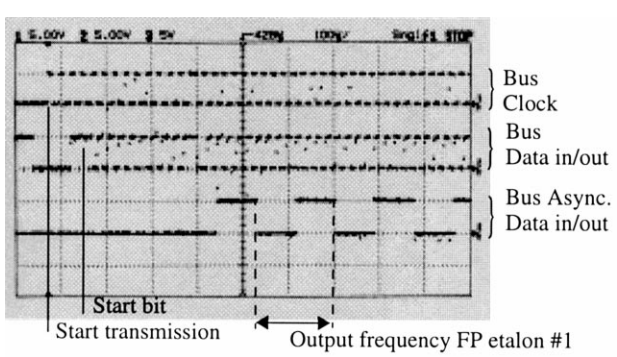

Fig. 8. Oscilloscope plot of the bus signals for a high light level.

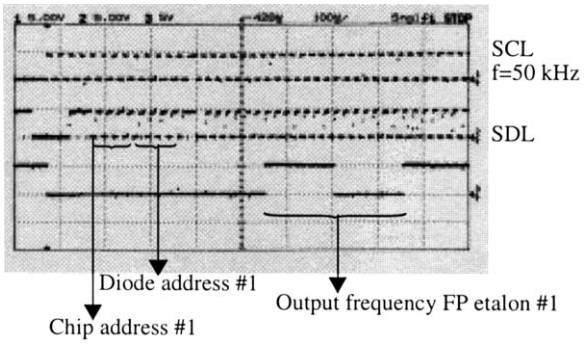

Fig. 9. Oscilloscope plot of the bus signals for a low light level.

multiplexer, and some other digital circuits. Only four external connections to the chip are strictly needed: V_{dd} (+5 V), ground, the clock input SCL, and the bidirectional dataline (SDL), since this line can also be used for transmission of the frequency output. The other pads are the chip address pins and pins for testing purposes. The two grounds (analog ground and digital ground) and the two supplies (analog supply and digital supply) are separated on the layout design to avoid digital interference.

4. Experimental results

Devices are addressed via an ISS bus interface by a conventional eight-bit microcontroller. A standard internal data-acquisition PC card can be also used for this purpose. The bus interface frames use eight bits for addressing. The four most significant bits are used for addressing the chip, so up to 16 chips can be addressed. The four least significant bits are used to select one of the 16 photodiodes. After selection, the corresponding sensor places its output frequency over the data asynchronous bus line. This sequence can be seen in the oscilloscope plots of Figs. 8 and 9. Three lines are shown: the clock line, the data line and the output frequency line.

Fig. 10 presents the spectral responsivity (A/W) between 400 and 800 nm for all 16 channels using on-chip photodiodes. The ratio between the base line and the peak maximum ranges from 4 to 7. The relatively high-intensity stray light, beam divergence, and the roughness of the surface are responsible for the background signal. Stray-light compensation methods must be used in order to compensate for the non-idealities of both the incident light beam and the Fabry–Perot etalon.

5. Conclusions

A single-chip CMOS optical microspectrometer containing an array of 16 addressable Fabry–Perot etalons (each with a different resonance cavity length), photodetectors and circuits for read-out, multiplexing, and driving a serial bus interface was fabricated. The result is a chip that can operate using only five external connections (including V_{dd} and V_{ss}) or in the simplest version with only four external connections (the data line will be also used for output frequency line) covering the visible spectral range. The array-type microspectrometer can be glued on an active silicon platform using Multi-Chip-Module (MCM) techniques [9]. This configuration allows more than one microspectrometer to be glued to the platform (up to 16, according to the four bits to address) to increase the spectral range. The advantage of the device presented is that it can easily be tuned during fabrication to cover different spectral bands, by adjusting the etching time of

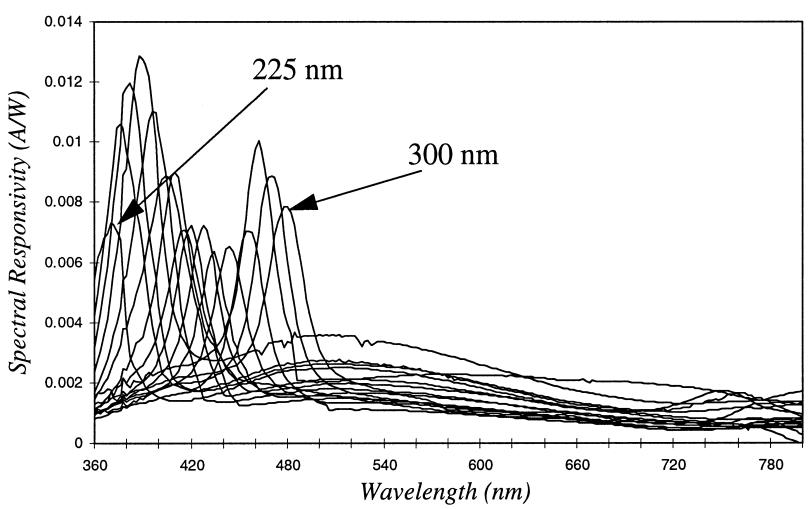

Fig. 10. Spectral responsivity of the 16-channel micro-spectrometer for a 45-nm Ag/SiO_2/20 nm Al layer stack. The SiO_2 layer thickness is used as a parameter and varies from 225 to 300 nm in 5 nm increments.

Table 1
Single-chip optical microspectrometer test results

	Condition	Test result
Operating voltage	5 V	
Power dissipation at 1 MHz	Clk = 1 MHz	1250 μW
Power dissipation at 100 kHz	Clk = 100 kHz	700 μW
Max. clock frequency	–	6 MHz
Dark frequency	25°C	0.05 Hz
Free spectral range	–	380–500 nm
FWHM	–	18 nm
Diode responsivity (no Fabry–Perot etalon)	$\lambda = 480$ nm	0.18 A/W
Sensivity (no Fabry–Perot etalon) [7] ref. TLS230 from Texas Instruments	$\lambda = 670$ nm	1.1 kHz/W m^{-2}
Sensivity with Fabry–Perot etalon [7] ref. TLS230 from Texas Instruments	$\lambda = 670$ nm	511 Hz/W m^{-2}

the oxide only, without affecting the device layout. Power consumption is 1250 μW for a clock frequency of 1 MHz (see Table 1).

Acknowledgements

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Biographies

José Higino Correia graduated in Physical Engineering from University of Coimbra, Portugal in 1990. Since May 1999, he has been an Assistant Professor at Dept. of Industrial Electronics, University of Minho, Portugal. In this University, he obtained the PAPCC (equivalent to MSc degree) in Electronics and Instrumentation in 1994 and he obtained in 1999 his PhD degree in the field of microsystems for optical spectral analysis at Delft University of Technology, the Netherlands.

Ger de Graaf was born in Delft, the Netherlands, on August 1, 1955. He is a staff member of the Department of Electrical Engineering of the Delft University of Technology since 1976. He received his BSEE degree in electrical and control engineering from the Technische Hogeschool in Rotterdam in 1983. Currently, he is working on electronic circuits for silicon sensors. Since 1992, he also has a consultancy company specializing in electronic design and computer-controlled measurement systems.

Seong Ho Kong joined in February 1997 the Electronic Instrumentation Laboratory at the Electrical Engineering Department of Delft University of Technology as a PhD. student, where he performs research on uncooled infrared detector array based on integrated thermopiles. He was born in Youngcheon, South Korea in 1967. He received his BSc degree in Electronic Engineering from Kyungpook National University, Korea in 1993 and his MSc degree in Mechatronics and Precision Engineering from Tohoku University, Japan in 1996 with his thesis work concerning fabrication of reactive ion etching systems for deep silicon etching.

Marian Bartek received his MSc degree (cum laude) in Electrical Engineering in 1988 from the Electrical Engineering Department of the Slovak Technical University, Bratislava, Slovakia. His master's thesis dealt with liquid phase epitaxy of InGaAsP quaternary layers for optoelectronic applications. After completion of his military service in October 1989, he continued this research at the Electrical Engineering Department of the Slovak Technical University as a research assistant. In August 1991, he joined the Electronic Instrumentation Laboratory, Department of Electrical Engineering at the Delft University of Technology, the Netherlands, where he, in 1995, obtained his PhD degree for research on selective epitaxial growth for smart silicon sensor applications. Currently, he is a research fellow at the same laboratory and his work deals with technological aspects of integrated silicon sensor systems.

Reinoud F. Wolffenbuttel received his MSc degree in 1984 and his PhD degree in 1988, both from the Delft University of Technology. His thesis work dealt with the application of silicon to colour sensing. Between 1986 and 1993, he was an assistant professor and since 1993, an associate professor at the Laboratory of Electronic Instrumentation of the Delft University of Technology and is involved in instrumentation and measurement in general and on-chip functional integration of microelectronic circuits and silicon sensor, fabrication compatibility issues and micromachining in silicon and microsystems in particular. In 1992/1993, he was a visiting scientist at the University of Michigan, Ann Arbor, MI, USA, and was involved in the research on low-temperature wafer-to-wafer bonding.