An Integrated Folded-Patch Antenna for Wireless Microsystems

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Abstract

A fully integrated, folded-patch antenna for operation at 5.62 GHz and application in wireless sensor networks has been realized and characterized. Overall dimensions of 4x4x1 mm^3, measured bandwidth of 100 MHz and an efficiency of 32% were achieved. The antenna fabrication is based on wafer-level packaging techniques and consists of two adhesively bonded glass substrates with through-substrate electrical vias and 3-D metallization. The measured electrical characteristics of the antenna prototype fit well with the simulations.

INTRODUCTION

Wireless sensor networks are an emerging technology becoming increasingly popular in military and civilian applications such as surveillance, monitoring, disaster recovery, home automation, health care and many others. In a wireless sensor network, a large population of sensor nodes is scattered in the monitored area to acquire, process and transfer data to the required destination. The individual nodes in these networks should have small form factor, light weight, long service with a limited energy source, and be inexpensive so they can be deployed in large numbers. To be effective and to have the ability to adapt itself to complex environments, each sensor node has to be autonomous. Obviously, these requirements are difficult to meet simultaneously.

This new technology brings not only numerous opportunities but also many technological challenges [1]. Recent technological advances have led to wireless network demonstrators that are capable of observing the physical world, processing the data, making decisions based on the observations and performing appropriate actions [2]. However, from the cost point of view, a full integration of all devices belonging to the sensor node is highly desirable. Also, medical applications form a strong driving force towards a full integration.

Solutions for an on-chip integrated circuitry, from baseband to antenna input/output, are already available. However, the antenna, as the key element in achieving a fully integrated solution, notwithstanding all the development efforts, still remains to be an open challenge. Full integration requires the availability of very-small antennas that can be fitted into a single chip. One approach being used in medical applications is a small coil acting as an antenna to transmit the data [3]. Despite all the success, they suffer from range drawback. The reading device has to be placed very close to the implanted sensor in order to reliably acquire the monitored data. Better solution would be to use an antenna design that allows for data transmission in a range of 1-10 m. This would allow real time health condition monitoring without movement restrictions of e.g. an astronaut working in the space shuttle using the local area network already available [4]. Many people could instantly benefit from this spatial technology at their home comfort.

Widespread of distributed sensing systems will emerge faster with the availability of cheap and easy-to-use 'on-chip' or 'in-package' solutions, equipped with short-range wireless communication capabilities. The state-of-the-art wireless sensor network nodes typically use an external antenna, which is a limiting factor of the device size.

In this work, wafer-level packaging (WLP) techniques, like adhesive wafer bonding and through-wafer electrical via formation, are applied to overcome the open challenge of a fully integrated solution, where a chip-size antenna is integrated in a cost effective way. The use of a folded shorted-patch antenna (FSPA) allows significant size reduction compared to simple patch antennas. The FSPA is designed to operate inside the 5-6 GHz ISM short-range wireless communication band, where smaller antennas can be developed and radiating signal is confined to small areas [5]. The antenna is formed with a stack of glass wafers adhesively bonded and interconnected with trough wafer vias [6].

ANTENNA INTEGRATION

Figure 1 shows the proposed antenna integration concept. A shorted folded-patch antenna is integrated using glass substrates on top of a silicon wafer containing the active circuitry.

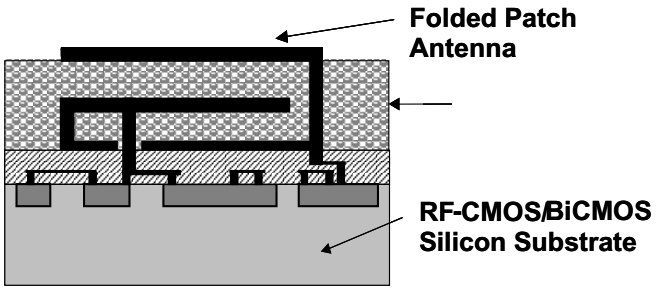

Figure 1. Concept of an integrated chip-size antenna using wafer-level packaging techniques.

Several small and planar antenna types have been proposed for wireless communications but none of them was designed to fulfill all the restrictions and requirements set by on-chip integration. Those restrictions include the properties of available substrate materials and the way they can be processed. Many of the previously proposed solutions to integrate antennas on-chip have been based on the design of planar antennas using silicon as a substrate. Since the low-ohmic silicon substrate suffers from high losses, high-resistivity silicon or bulk micromachining have to be used in order to increase the antenna efficiency. An optional solution to decrease the antenna losses is to use a combination of a low-loss material with silicon. The new material can be used as an antenna substrate and at the same time as a carrier for high-quality passives. The silicon will be used to implement the necessary circuitry.

Such combination of substrates can be achieved with the use of wafer-level packaging (WLP) techniques, like adhesive wafer bonding and through-wafer electrical via formation, which allows combination of silicon together with different silicon-compatible substrates. The typical silicon-compatible substrates (e.g. glass, BCB, polyimide, SU-8) have lower dielectric constant compared to silicon. In this way, the use of such materials reduces the losses at the expense of a size increase of the integrated antenna. However, the use of an advanced antenna design may be used to overcome this drawback, providing a small and effective radiator. In this work, we investigate the use of a folded structure based on multiple-stacked glass substrates.

ANTENNA MODELING

A cross-section of the proposed antenna structure is shown in Figure 2. The antenna consists of three horizontal metal sheets that are electrically connected by two metal walls. All this is embedded in a glass substrate having certain electrical permittivity and dielectric losses. These two parameters together with the antenna geometry and actual dimensions will determine its radiation characteristics and overall performance. For good performance, the metallization layers should have very low resistivity and the substrate should have the lowest losses possible. Noted should be the angled wall, which is desirable from the fabrication point-of-view due to lithographic difficulties to pattern layers on vertical walls.

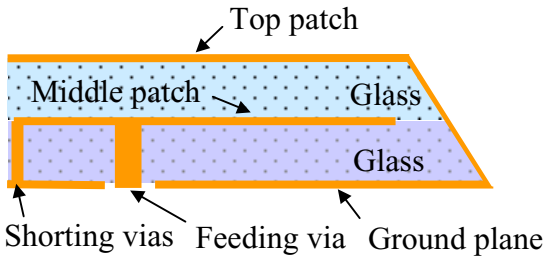

Figure 2. Folded shorted-patch antenna cross-section.

ANTENNA FABRICATION

The folded-patch antenna fabrication sequence is schematically shown in Figure 3. Two AF-45, 100 mm diameter and 500 µm thick glass wafers are used as the starting material.

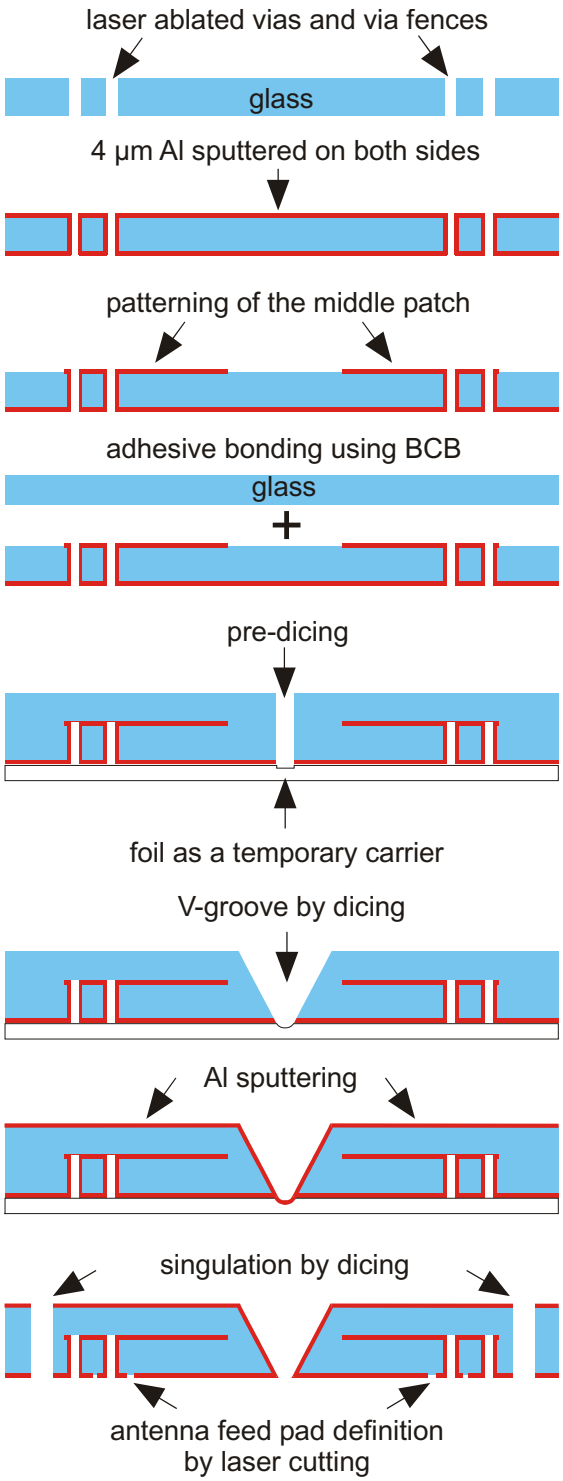

Figure 3. Schematic fabrication sequence used for antenna fabrication.

Firstly, 200 µm diameter through-wafer vias were formed in the bottom glass substrate. A laser system at Philips CFT with a 30:1 reduction mask was used for ablation of the feeding and shorting vias. Because the selected glass substrate material exhibits sufficient light absorption in the UV region only, a 193 nm excimer laser was required. The initial tests with 248 nm laser were not successful due to formation of cracks. The vias were then metallized by sputtering of 4 µm Al layers from both sides of the wafer. Due to the low aspect ratio of the vias (2.5:1) and the fact that the sidewalls are not perfectly vertical, it was possible to form a continuous conductive layer within the vias. The middle antenna patch was then patterned using electroplated photoresist and plasma etching (see Figure 4).

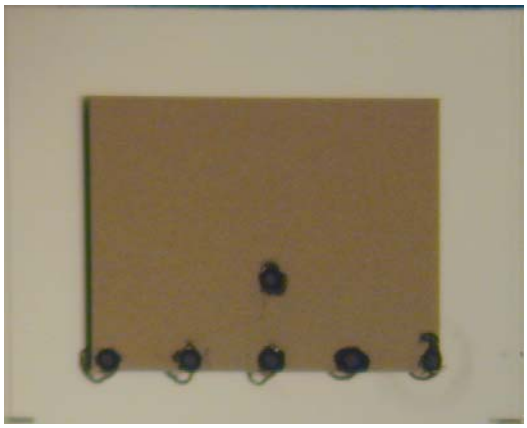

Figure 4. Photograph showing detail of the bottom glass substrate with the 200 µm diameter ablated vias and the patterned middle Al antenna patch.

Then, the second glass wafer was adhesively bonded using ~5-7 µm thick BCB layer as the adhesive. This wafer stack was attached to a temporary carrier (foil or Si wafer) to allow formation of the slanted antenna sidewall by V-blade dicing. The sidewall shaping was performed in two steps. First, a vertical trench through the wafer stack was formed using a 400 µm wide dicing blade. In the second step, a V-shaped dicing blade (60 deg. angle) was applied to shape the antenna sidewalls. The accuracy of this step is critical for antenna electrical properties and care has to be taken to achieve alignment with the middle antenna patch. The achievable accuracy of blade positioning is close to 2 µm, which is more than sufficient.

The antenna fabrication then continues by Al-layer sputtering to metallize the second glass wafer including the V-shaped trenches. Finally, a standard dicing with vertical sidewalls is applied to define the remaining three antenna sidewalls and thus the lateral dimensions of the final antenna. The fabricated antenna prototype compared to a 1 eurocent coin is shown in Figure 5. For fabrication simplicity, the antenna feeding pad was defined by laser cutting on the to-be-measured samples only. For the measurement purposes, the antenna was attached to a PCB with a 50 Ω microstrip line, and the antenna feeding pad was connected using multiple bond wire connections (see Figure 6).

Figure 5. Photograph of the folded shorted-patch antenna prototype realized on a stack of two AF-45 glass substrates.

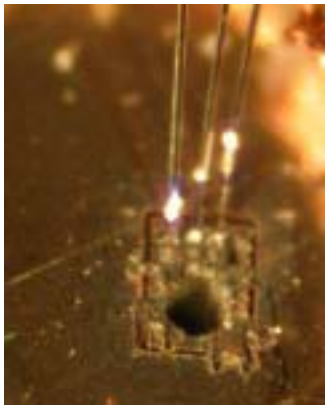

Figure 6. Close-up of antenna backside feeding point connected using multiple bond wires to a PCB.

RESULTS

The characterization of the antenna operating properties was made with a vector network analyzer. Figure 7 shows the measured and simulated antenna input characteristics. The measured results shown were obtained after de-embedding. To obtain the de-embedded data, the antenna was first measured with the backside ground connected also to the feeding microstrip line. In this way, it was possible to remove the contribution of the inductance from the thin wire bonds, and the metal layers, mainly the very thin metal layer that metallizes the vias.

The simulated prototype has an operating frequency of 5.65 GHz, with a –10 dB return loss bandwidth of 50 MHz. This is in a good agreement with the measured values of 5.62 GHz for the operating frequency. This small shift in operating frequency is due to fabrication tolerances. The measured value of 100 MHz for the –10 dB return loss

bandwidth is larger then the predicted by simulation. The measured efficiency was 32 %, which is smaller then the predicted 47 %. We believe that the increase in the measured bandwidth and efficiency reduction is due to higher losses induced by the thin, and difficult to control, metal layer inside the vias. This differences are explained due to higher losses in the fabricated prototype then the accounted by simulation. Since the losses are higher, the quality factor is smaller which leads to a larger bandwidth and smaller efficiency. Simulations indicate that the replacement of rather-lossy sputtered Al layers with electroplated Cu metallization will increase antenna efficiency up to 50 %.

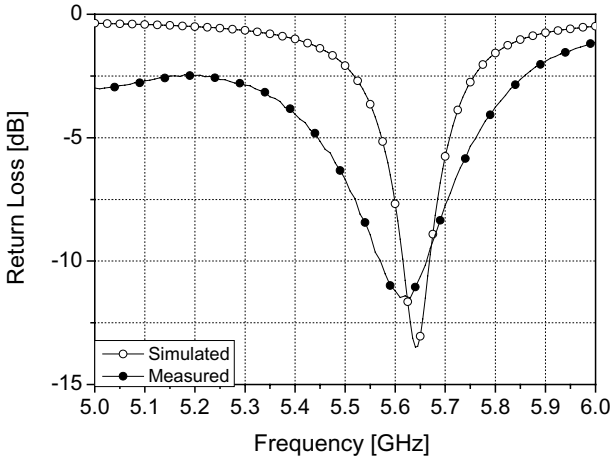

Figure 7. Measured and simulated return-loss of the antenna prototype.

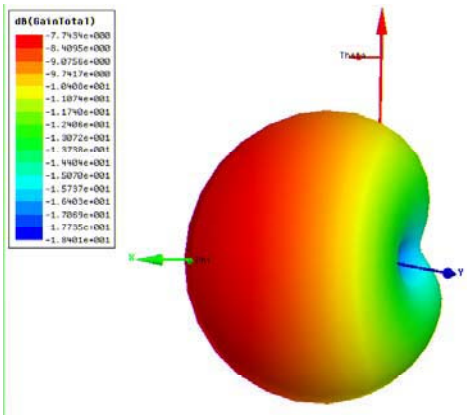

Figure 8. Simulated radiation diagram of the proposed antenna.

Figure 8 shows the simulated radiation pattern. From the figure it is expected that the antenna will radiate mainly from the direction of the aperture.

Further size reduction is possible by using a substrate with higher dielectric constant, like high-resistivity polycrystalline silicon, as we have already demonstrated for a simple patch antenna [7], or using different antenna geometry [8], [9].

CONCLUSIONS

A chip-size antenna for operation at 5.62 GHz was designed and fabricated using wafer-level packaging techniques. The antenna demonstrator realized on a stack of two AF-45 glass substrates has overall dimensions of 4x4x1 mm^3, measured bandwidth of 100 MHz and measured efficiency of 32%.

ACKNOWLEDGEMENTS

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