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Study of TiN/Ti/HfO_2/W resistive switching devices: characterization and modeling of the set and reset transitions using an external capacitor discharge

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ABSTRACT

In this work, we have studied the control of set and the reset transitions in TiN/Ti/HfO_2/W resistive switching devices using a new approach based on the injection of a limited amount of charge through the use of a capacitor discharge. Instead of applying conventional voltage or current signals, the capacitor discharge through the devices is able to perform both transitions. An accumulative process is observed if we apply consecutive discharges, and, when increasing the capacitor voltage in each discharge, the transitions between both resistance states are completed. In addition, it has been shown that faster transitions require larger capacitor voltages. Further, the electrical results were used to tune the dynamic memdiode model, which was employed to simulate set and reset processes driven by the capacitor discharges. The model successfully reproduced the measured memristor response to the capacitor discharge.

1. Introduction

Memristors based on the resistive switching phenomenon, such as valence change mechanism (VCM), are attracting great attention in recent years because of their wide range of applications [1,2]. Their structure is simple and they exhibit high operation speed, good endurance, low power consumption as well as CMOS compatibility [3], and that is why they are currently considered to be one of the next-generation alternatives to traditional non-volatile memories [4,5]. Their operation is based on the resistive switching (RS) phenomenon, where a reversible resistance change takes place: a conductive filament (CF) between two metal electrodes can be formed (set) and ruptured (reset), resulting in two different resistance states, a low resistance state (LRS) and a high resistance state (HRS). In addition, these devices may exhibit tunable resistance states, which can be controlled by an electrical signal [6], since the CF dimensions can be electrically controlled. Therefore, the information in the VCM cells can be encoded in different resistance states, obtaining analog-like multilevel operation. This behavior allows the use of these devices for the implementation of artificial synapses in neuromorphic systems, since the synaptic weight between two neurons can be electrically adjusted [7,8]. Various combinations of metal electrodes and oxide layers have been studied as memristors [9–11]; transition metal oxides-based devices are the most widely studied materials [12], and specifically HfO_x-based devices were found to be CMOS compatible, highly scalable and robust, with ultrafast and low-energy consumption operation [13,14]. The control of the set and reset transitions are important in both memory and neuromorphic applications, and several approaches have been studied, such as programming schemes based on voltage ramp [15]. Previously, we studied both transitions in HfO_2-based ReRAM devices. We studied the switching transitions using voltage pulses [16], but it is difficult to control the set transition as power suddenly increased when keeping the voltage constant (a sudden increase in the current value takes place in this transition). Some solutions have been proposed when using voltage pulses: employing two RRAM devices with opposite weight contribution [17] or applying a proper reset pulse after the potentiation one [18]; the first attempt requires more complex devices, and the second one more complex peripheral circuitry. In order to avoid this problem, we used

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current pulses [19], but this time the reset transition could not be controlled because power suddenly increased when keeping the current value constant (a sudden increase in the voltage value takes place in this transition), and hardware limitations hinder the use of short current pulses. To overcome this issue, in this work we introduce a new approach based on the control of the set and reset processes by the injection of a limited amount of charge through the use of a capacitor discharge. To do so, we use memristors based on a TiN/Ti/HfO_2/W stack. An electrical characterization has been performed, and, in addition to the experimental characterization, the dynamic memdiode model proposed by Miranda et al. [20] has been used in order to simulate the memristor behaviour and calculate the programming events driven by the capacitor discharge by means of transient simulation with LTspice. Using this approach, both set and reset transitions are found to be controllable, and good agreement has been obtained between measured and modeled data using the memdiode model.

2. Experimental

2.1. Sample fabrication

The study was carried out using TiN/Ti/HfO_2/W metal–insulator–metal (MIM) capacitors as resistive switching devices. The fabrication process started with the deposition of a 20 nm-thick Ti adherence layer on a 100 mm-diameter Si-n^{++} wafer, followed by the deposition of a 50 nm-thick W layer. Both layers were grown by magnetron sputtering. Next, a 100 nm SiO_2 isolation oxide was grown by plasma-enhanced chemical vapor deposition (PECVD) using silane (SiH_4) as the precursor, and then patterned by photolithography and dry etching. The active area of the MIM devices is defined by the apertures in the SiO_2 layer. After the active area definition, the 10 nm HfO_2 film was deposited by atomic layer deposition (ALD) at 225 °C using Tetrakis (dimethylamino) hafnium (TDMAH) and H_2O as precursors and N_2 as the carrier and purge gas. The top electrode, consisting of a metal layer of 10 nm-thick Ti and 200 nm-thick TiN, was then grown by magnetron sputtering and patterned by a lift-off process. Finally, a 500 nm Al layer was deposited on the back of the wafer by magnetron sputtering for electrically contacting the W bottom electrode through the Si-n^{++} substrate. The fabricated TiN/Ti/HfO_2/W devices are square-shaped with areas ranging from 2 × 2 μm^2 to 120 × 120 μm^2. A cross-section representation of the fabricated devices is shown in Fig. 1.

2.2. Electrical characterization set-up

The current–voltage (*I–V*) measurements were performed using an HP4155B Semiconductor Parameter Analyzer. The capacitor discharge-based electrical characterization was carried out using the set-up shown in Fig. 2. The capacitor charge and discharge is controlled by two relays (ϕ_1,ϕ_2). First, the switch ϕ_2 is *on* and the switch ϕ_1 is *off*. A Keithley 617 electrometer charges the capacitor to an initial voltage $v_C(t=0) = v_C^0$. Once the capacitor is charged, the switch ϕ_2 opens and immediately the switch ϕ_1 closes, so the capacitor discharges through our resistive switching device, flowing a time dependent current $i(t)$. After the capacitor is fully discharged, the switch ϕ_1 opens and the HP4155B can measure the resistance state of the device by applying + 0.1 V to the top electrode. The internal relays of the Semiconductor Parameter Analyzer channels remain in *off* state unless it measures the resistance state. The equipment was connected to a computer using a GPIB interface and was controlled using Agilent VEE software. The measurement stages are also shown in Fig. 2.

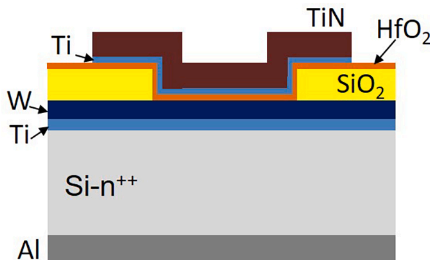

Fig. 1. Cross-section representation of the fabricated devices.

3. Results and discussion

3.1. Electrical characterization results

The fabricated devices show filamentary resistive switching, as found by Poblador et al. [21]. The conductive filaments are due to oxygen vacancy clusters, so the switching mechanism is valence change memory effect (VCM) [22]. Titanium, as an oxygen reservoir material, is able to attract/release oxygen from/to the HfO_2 film. This ion migration is responsible for the formation of percolation paths made of oxygen vacancies [23]. After performing an initial electroforming process to form the conductive filaments, several *I–V* resistive switching cycles were measured and are shown in Fig. 3. The voltage was applied to the top electrode while the bottom electrode was connected to the ground. The voltage ramp speed was about 0.4 V/s. The results revealed bipolar resistive switching behavior, with set and reset transitions at top positive and negative voltages, respectively.

When the capacitor discharges through the resistive switching device, an electrical current flows through the resistive switching devices. The current value can be expressed by:

$$i(t) = C\cdot\frac{dv_C(t)}{dt} = \frac{-v_C(t)}{R(t)} \tag{1}$$

where $R(t)$ is the switching device resistance value and C is the capacitance value. This means the capacitor discharges over time according to the following equation:

$$Q_C(t) = v_C^0\cdot C\cdot\exp\left[\int_0^t \frac{-dt'}{R(t')\cdot C}\right] \tag{2}$$

where v_C^0 is the initial capacitor voltage.

The first experiment consisted in applying different capacitor discharges, when changing the initial capacitor voltage (v_C^0), being the device initially in the HRS to observe the set transition, or in the LRS state to observe the reset transition. When observing the set transition, the initial capacitor charge was always 1 nC, and was always 8 nC when observing the reset transition (charged in this case with negative voltages). The results are shown in Fig. 4 for both transitions. The change in the conductance value depends on the maximum voltage across the devices, which is obtained in $t = 0$ when the capacitor just starts discharging. We have also represented in Fig. 4c the change in the conductance value as a function of the initial power dissipated by the devices ($P_0 = v_C^0\cdot i(t=0)$). The power needed for the LRS→HRS transition is higher than the one necessary for the HRS→LRS transition, as expected from the measured *I–V* characteristics. This control of the resistivity state by the power flowing through the device implies a Joule process, as the conductive filament would be controlled by its local temperature.

Nevertheless, the change in resistance not only depends on the initial power but also on how long the current flows through the device. According to Eq. 2, and defining the time constant parameter τ ($\tau(t) = R(t)\cdot C$), the higher the τ values the wider the current pulses obtained when discharging the capacitor. We are able to modify τ without modifying P_0 by changing the capacitor value while keeping the initial voltage v_C^0 constant. Fig. 5 shows the results obtained, being the device either in HRS (set transition) or in the LRS state (reset transition) before each capacitor discharge. We can observe the initial power required to

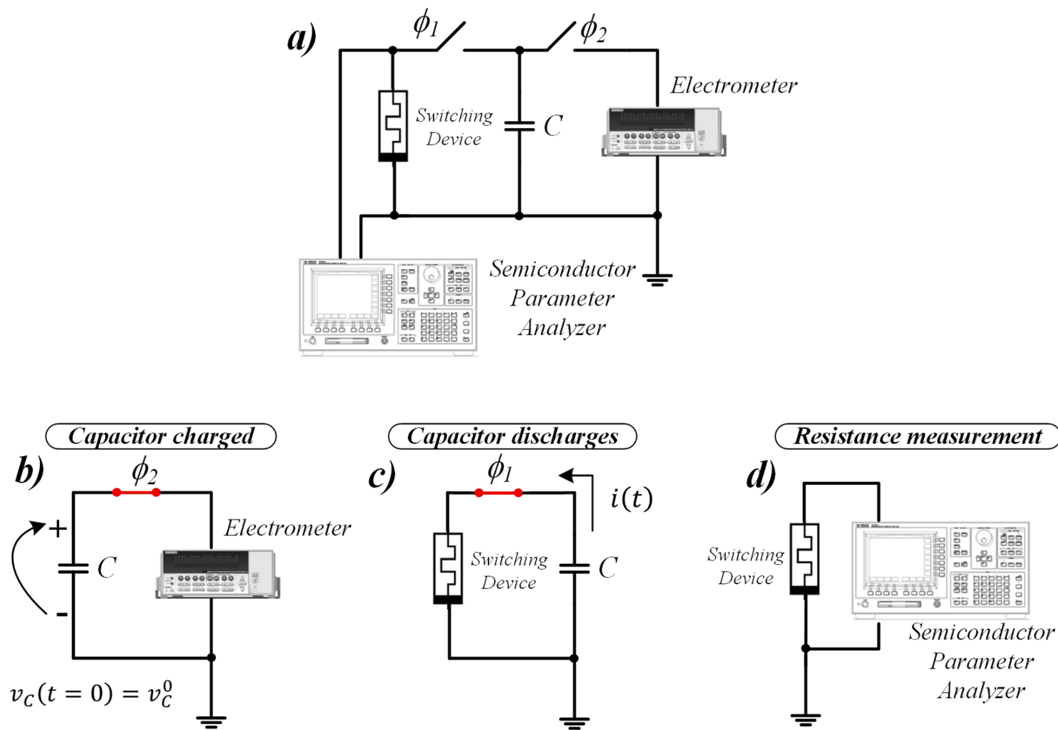

Fig. 2. Electrical characterization set-up used to carry out the measurements based on a capacitor discharge (a). Relay ϕ_2 allows the capacitor to be charged to v_C^0 (b). Relay ϕ_1 allows the capacitor to be discharged through our resistive switching devices (c). The HP4155B Semiconductor Parameter Analyzer measures the resistance state of the device (d).

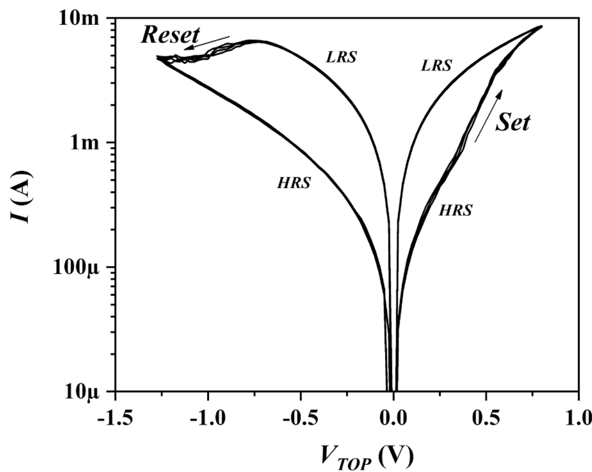

Fig. 3. Several current–voltage (I–V) cycles.

obtain the same change in conductance decreases for longer capacitor discharges. This result agrees with Yu et al. [24], who observed that the switching time in metal oxide ReRAM devices exponentially decreases as voltage pulses amplitude increases. This dilemma (higher bias necessary for higher operation speed) has been reported before [25]. However, if a minimum discharge time is not reached, no change in the conductivity state is found: for instance, when using P_0=14 mW in the reset transition, this transition starts for τ values larger than about 0.1 μs. But if the initial power is too low, the transition could not even take place: for instance, 0.3 mW is not high enough to initiate a set transition regardless of the discharge time. So both power and discharge time can limit the resistance change.

Regarding the set transition, the change in conductance reaches a saturation point as τ value increases. When the conductive filament gets thicker, current can flow without changing its structure. Of course, the conductance saturation value increases for higher P_0 values, because the CF needs to be wider to be able to hold larger currents. However, in the case of the reset transition the conductive filament is ruptured even for P_0=9 mW. Yun et al. found the CF retraction in the reset transition in ReRAM devices is due to the motion of oxygen ions with the help of an electric field and Joule heating [26]. When the CF gets thinner its resistance value increases, and the Joule heating should increase for larger capacitor discharges, which helps the CF rupture.

The fact that longer discharges increase the conductance change could lead to an accumulative effect: applying several short discharges is equivalent to one longer discharge. In the case of the set transition, we applied several consecutive and identical discharges. After driving the device to the HRS, identical discharges, biasing the capacitor with + 0.75 V, were applied. We used three different capacitance values. The results are shown in Fig. 6a. A large conductance change is observed after applying the first pulse. This change increases as the capacitance value also increases, as expected from the results in Fig. 5, since larger capacitances correspond to higher τ values. After the first pulse is applied, the conductance value has increased, so when the following discharges are applied P_0 value is increased and the cumulative effect can be observed. However, the conductance value finally saturates after some discharges take place. This can be explained as follows: after a capacitor discharge is applied, not only the resistance value decreases but also τ value decreases. The discharge time becomes so short that no change in conductance is possible. Jang et al. obtained a complete set transition when applying increasing voltage pulses [27], so increasing the capacitor value in each of the consecutive discharges could balance the decrease in τ value and the complete transition could be obtained. Accordingly, we then applied consecutive but not identical discharges: after each pulse is applied, v_C^0 is increased. Fig. 6b shows the results. We can observe a minimum v_C^0 value is needed (so a minimum P_0 value) to start the transition, which increases for low capacitor values (so for low τ values). However, now the set transition can be fully completed for

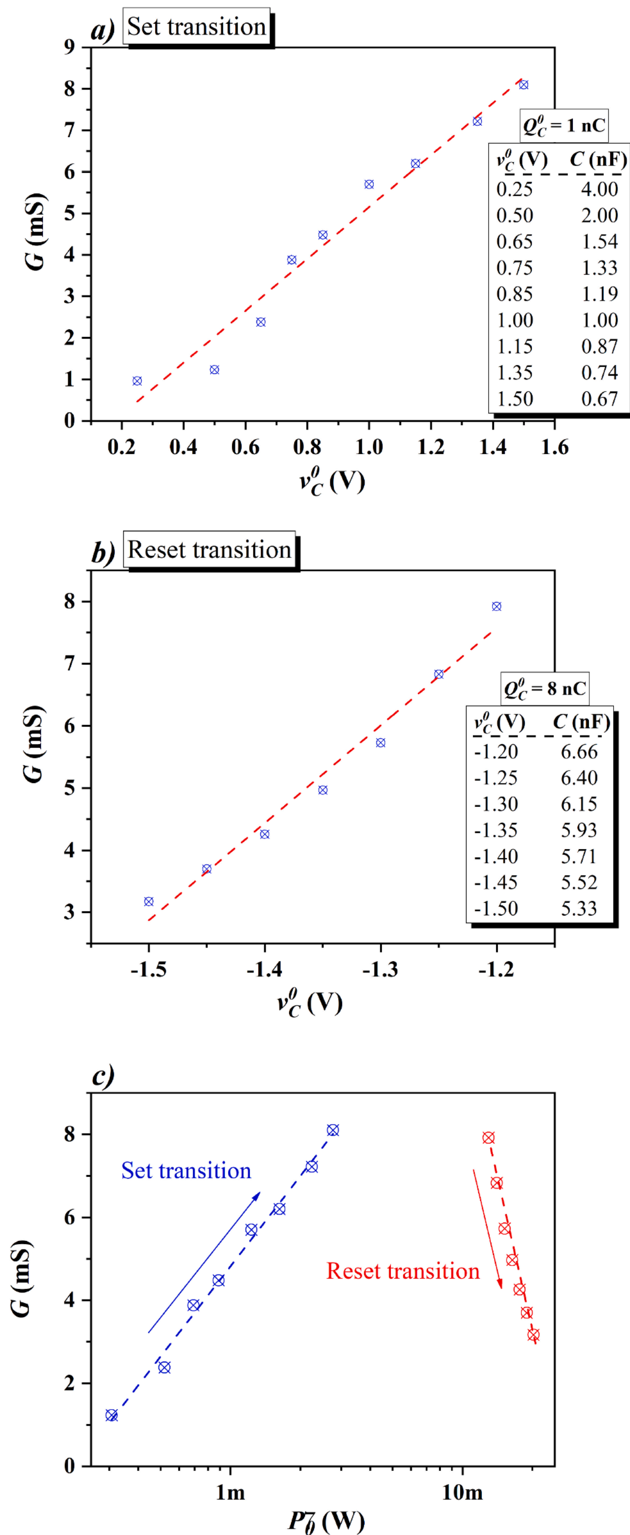

Fig. 4. Set (a) and reset (b) transitions obtained when discharging the capacitor charged using different voltage values. Both transitions are represented using the initial power absorbed by the devices (c).

consecutive capacitor discharges. Of course, higher v_C^0 values are necessary for lower capacitor values in order to perform a complete transition.

Finally, we studied the reset transition by using again consecutive and identical capacitor discharges. Now, the device was first biased in the LRS, and the capacitor was always biased with −1.5 V. Three

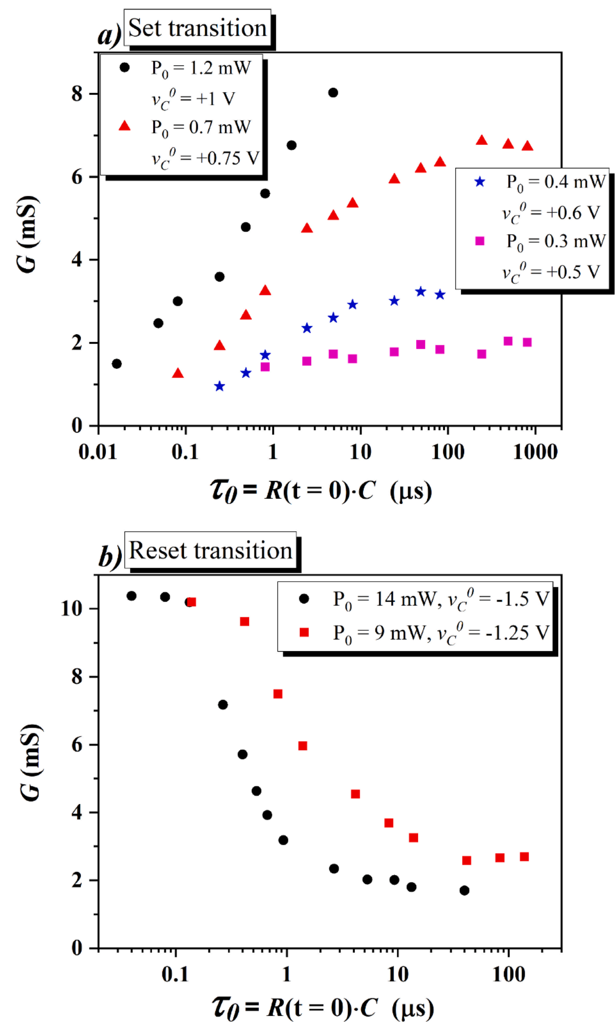

Fig. 5. Conductance for the set (a) and reset (b) transitions obtained when keeping P_0 constant and varying τ_0. The initial voltage value (v_C^0) has been added for each initial power.

different capacitance values were also used. We can see the results in Fig. 7a. In this transition the conductance value decreases for each discharge, which means P_0 value also decreases. However, we can observe an accumulative effect as conductance keeps decreasing for consecutive pulses. The reason is that now the discharge time increases as discharges take place, so the increase in τ value balances the decrease in P_0 value. We can see in Fig. 5 that the reset transition could be almost completed using low power values if τ value is high enough. However, after about 10 discharge cycles, a larger number of cycles are necessary for a small conductance change. This means the conductance finally remains almost constant for very low power values. The discharge time was the limiting factor in the set transition, but now, in the reset transition the power is the limiting issue. As in the case of the set transition, we also used consecutive but non identical discharges: v_C^0 value is increased after each discharge. Results are shown in Fig. 7b. Again, a minimum v_C^0 value (i.e. a minimum P_0 value) is necessary to start the transition. This minimum value increases for low capacitor values, because of their lower τ values. Now, the v_C^0 increase balances the increment in $R(t=0)$ values, giving place to a complete reset transition.

3.2. Device modeling and programming simulation results

As pointed out by Eq. 1, the discharge proccesses are limited by a time-dependent resistance. As a consequence, the common $R{\cdot}C$ current

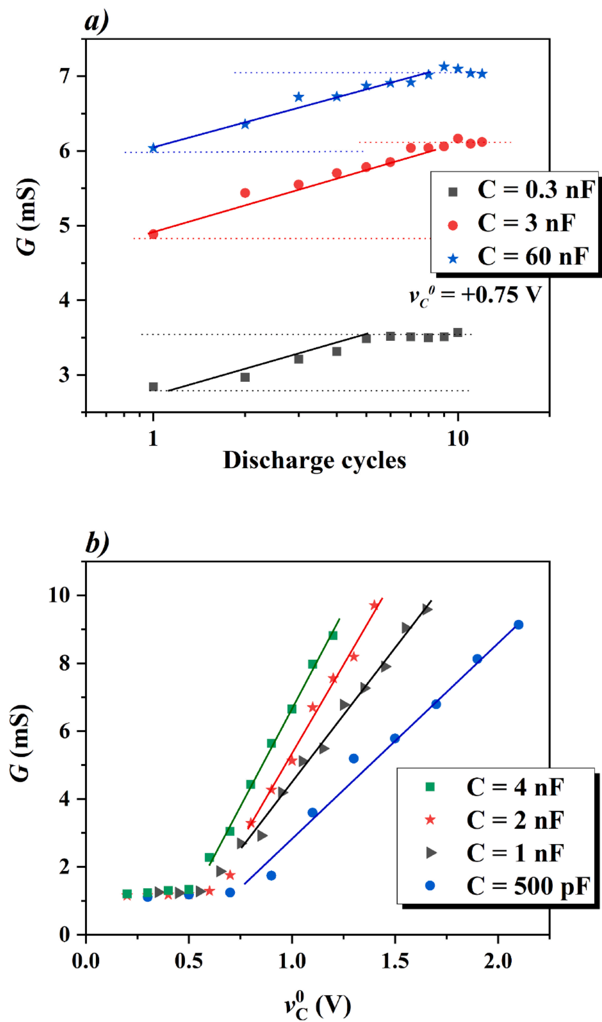

Fig. 6. Conductance during the set transition obtained when applying consecutive and identical capacitor discharges for three different capacitor values, always initially biased with + 0.75 V (a) and when applying consecutive capacitor discharges increasing the capacitor voltage for four different capacitor values (b).

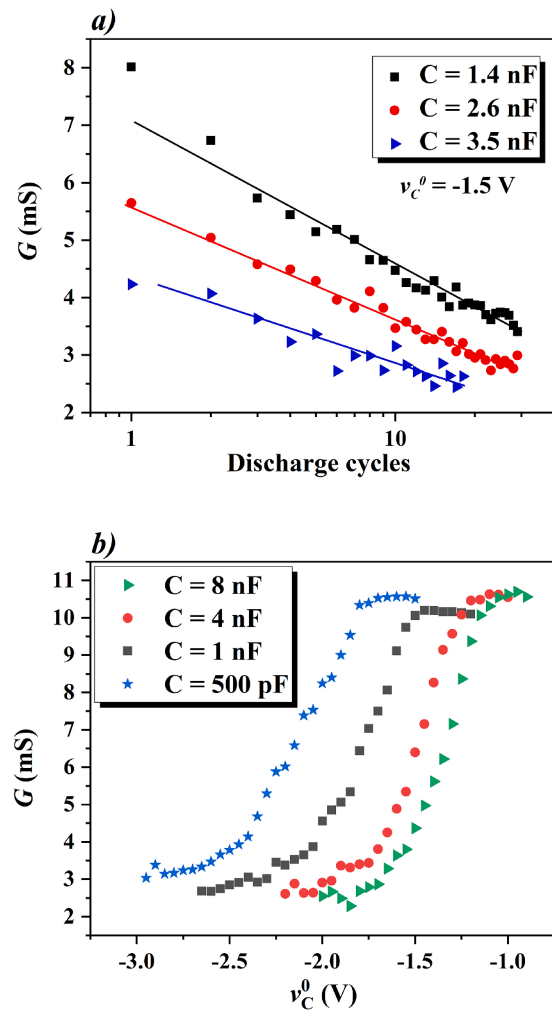

Fig. 7. Conductance during the reset transition obtained when applying consecutive and identical capacitor discharges for three different capacitor values, always initially biased with −1.5 V (a) and when applying consecutive capacitor discharges increasing the capacitor voltage for four different capacitor values (b).

discharge exponential expression (with a single and known time constant) can not be used for calculating the current over the time. Therefore, in order to study and characterize the previously described programming experiments through a capacitor discharge, we have used the dynamic memdiode model [20] for describing the memristor resistance as a function of time by means of LTspice simulations. In this general memristor model, the current depends on the applied voltage (v_C) and on the actual value of a state variable (λ):

$$i = i(v_C, \lambda) \quad (3)$$

The maximum device conductance is obtained when $\lambda = 1$ (for a valence change memory device, this situation physically corresponds to a minimum gap distance between the CF tip and one of the electrodes, after a set process [28]). On the other hand, the minimum memristor conductance is obtained if $\lambda = 0$ (maximum gap distance, after a reset process). The time evolution of the device is modelled by the following expressions:

$$\frac{d\lambda}{dt} = \frac{1-\lambda}{\tau_S(\lambda, v_C)} \quad (\text{set}, v_C > 0) \quad (4)$$

$$\frac{d\lambda}{dt} = \frac{-\lambda}{\tau_R(\lambda, v_C)} \quad (\text{reset}, v_C < 0)$$

where $\tau_{S,R}$ are characteristic times related to the set and reset events. More details about the model and expressions for $\tau_{S,R}(\lambda, v_C)$ can be found in reference [20]. Again, as $\tau_{S,R}(\lambda, v_C)$ are not constant during the programming processes, a simulation tool is required.

The measured *I–V* characteristics were employed to obtain the model parameters (according to the methods shown in [20]). Fig. 8 shows that a good fit is achieved using the memdiode model. The inherent cycle-to-cycle variability [29] of these devices could also be modeled, although we have not considered this issue here [15,30,31]. It is important to highlight that the model parameters (obtained from the fitting of the measured *I–V* traces) have not been changed, but the same values have been used in all the simulations performed in the present work, under different operation conditions.

Once tuned, the device model has been employed in order to analyse the transients of the programming processes and visualize the device operation point evolution. Set events using different capacitors previously charged with 1 nC were simulated. All the devices are assumed to be in the high resistance state ($\lambda = 0$) at the beginning. As the device current is a function of the applied voltage (v_C) and the state variable, λ,

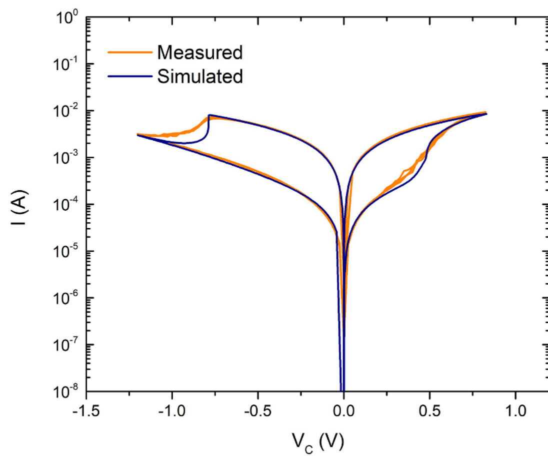

Fig. 8. Measured (orange) and simulated (purple) *I–V* curves.

the trajectories drawn on the $i(v_C, \lambda)$ surface by the memristor evolution during the set transients have been plotted in Fig. 9a. On that surface, we have plotted the trajectories during the transient simulation of a set programming driven by different capacitors previously charged with the same charge (1 nC), so that the initial voltage (v_C^0) is different. In all the cases, the initial memristor state is λ =0.

After these set programming events shown in Fig. 9a have finished, the final conductance is read (at 0.1 V) and plotted as a function of the initial voltage (v_C^0) in Fig. 9b. For the experimental measurements, the devices were driven to the high resistance state previously. Afterwards, different capacitors were charged with 1 nC and discharged through the memristor following the setup shown in Fig. 2. The final conductance is shown versus the initial capacitor voltage. As can be seen, a good agreement with the experimental values measured under the same conditions has been achieved, showing that the lower the capacitance (the higher the initial voltage), the higher the final memristor conductance (the set process advances further).

As can be seen in Fig. 9a, the state variable λ evolves at the beginning of the process (the orange arrows indicate the evolution direction), while the voltage remains almost constant. However, as the set process goes on and the device demands more current, the capacitor behaves as a current limiting component and the state variable change rate is slowed down. In order to check that the final device state is controlled by the capacitor limiting action, simulated trajectories departing from different device initial states (λ_0) are shown in Fig. 10 for the case with C = 500 pF ($v_C^0 = 2$ V). As can be seen, the final state (λ value) does not depend on the initial one (it has been assured that λ_0 is lower than the final λ value obtained when λ_0=0), but the memristor and current changes are limited approximately at the same point.

The dynamic memdiode model has been also used for modelling reset processes. In this case, different capacitors were previously charged with 6 nC (which implies different initial voltages) and used for driving the memristor reset process according to the setup shown in Fig. 2. The simulated trajectories (current and state variable evolution) are shown in Fig. 11a, while the resulting experimental and simulated conductance (measured at 0.1 V) is plotted in Fig. 11b. As expected, lower initial voltages (higher capacitance) generates less effective reset events (higher λ and final conductance values). In general, a good agreement has been obtained between measured and modeled data. Fig. 11b shows the accuracy of the model decreases for v_C^0 values between −1.6 V and −1.4 V. The model parameters were calculated by fitting the experimental *I–V* curve (the voltage swing was 0.83 V to −1.2 V). Because of the exponential dependence of the current on the applied voltage [32], a deviation of the modeled behaviour at −1.6 V could separate the model and experimental currents, even if the model parameters work well for the voltage range used for the fitting process.

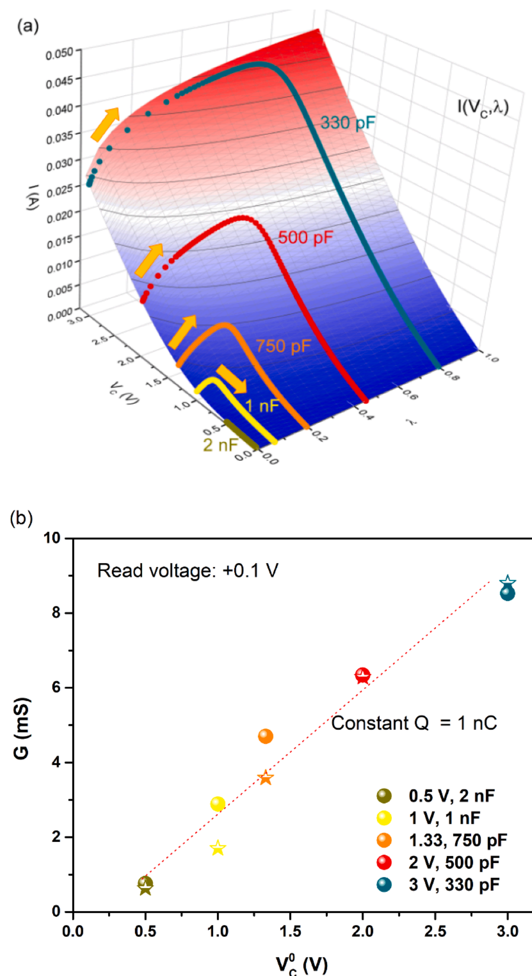

Fig. 9. The $i(v_C, \lambda)$ function obtained by means of the dynamic memdiode model is shown as a 3D surface (a). Comparison of the experimental (stars) and simulated (balls) final conductance (the read voltage is 0.1 V) measured once the programming processes shown in (a) have finished. The dashed line is the linear fitting of the measured data (b).

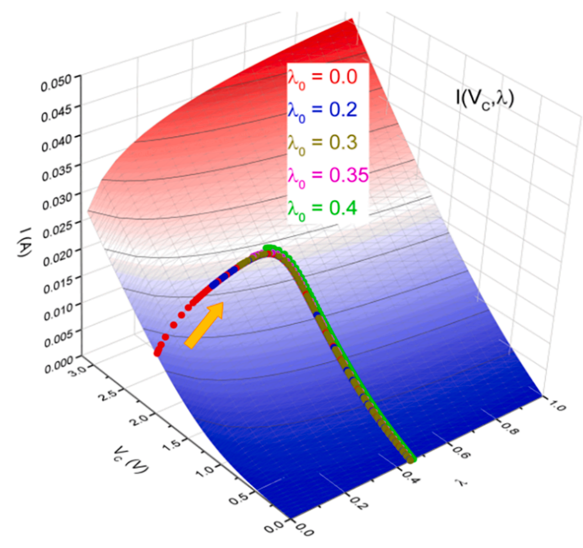

Fig. 10. Trajectories followed by the memristor evolution on the $i(v_C, \lambda)$ surface during the set programming when different initial states (λ_0) are considered (C = 500 pF, $v_C^0 = 2$ V).

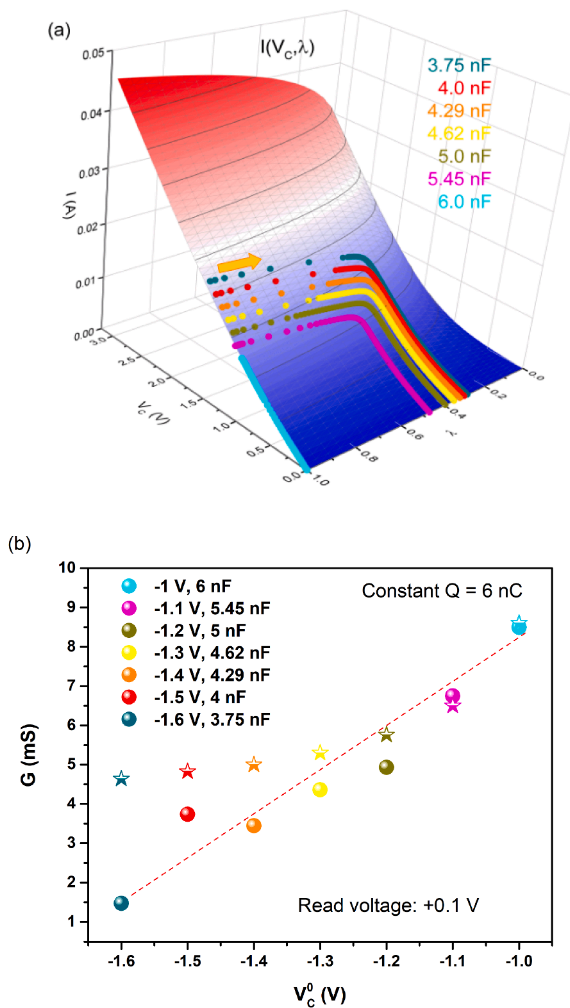

Fig. 11. Simulated trajectories on the $i(v_C, \lambda)$ surface during a reset process for different capacitors previously charged with 6 nC (a). Measured (balls) and simulated (stars) conductance at 0.1 V as a function of the initial capacitor voltage (v_C^0) after the reset processes modeled in (a). The dashed line is the linear fitting of the experimental data (b).

4. Conclusions

In this work, the use of a capacitor discharge through a memristor device has allowed us to study the set and reset transitions between high and low resistivity states, as this operation enables controlling the widthness of the conductive filament in TiN/Ti/HfO_2/W stacks. The initial capacitor voltage and the initial device resistivity fixes the maximum power, and the capacitor value influences the time the current flows through the devices. Both the initial voltage and the capacitor value can be independently controlled in an easy way. A dilemma has been observed: the increase of one of these parameters balances the decrease of the other one. This means high operation speed requires using higher voltages, although a minimum value of power and discharge time is necessary for a resistance change, because if any of these values is not high enough no resistance change is observed at all. The use of a capacitor has allowed us to obtain short current pulses, a more difficult issue when using a current source, only by limiting the amount of charge stored in it. In this way, an accumulation process is observed when applying consecutive discharges: we can obtain the same change in conductivity applying one longer discharge or several shorter discharges. Identical capacitor discharges revealed a not linear process, and a limited conductance change. These limitations can be avoided if consecutive but different discharges are applied: both transitions can be fully completed in a linear way if the capacitor voltage is increased after each discharge. The devices have been modeled by the dynamic memdiode model. In that way, the memristor evolution during the capacitor discharge could be simulated by LTspice. The electrical measurements have been used to test the model when a limited charge flows through the memrisotrs. The model succesfully reproduces the measured memristor response under different operation regimes (ramped voltage and capacitor discharge transient) using the same set of model parameters. Finally, it is important to note that we have used this setup to study the transitions between both resistance states. Although this setup could be an interesting issue for synaptic applications, it is important to note that this operation have important drawbacks: capacitors with high capacitance values could not be integrated due to area consumption, the time required for charging the capacitor and the fact that turning on and off the relay devices is also time consuming.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

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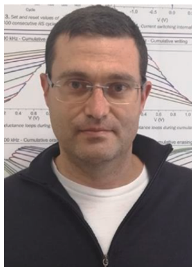

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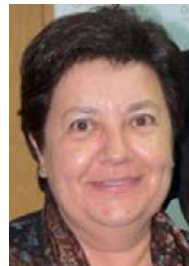

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