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Electrospun Stacked Dual-Channel Transistors with High Electron Mobility Using a Planar Heterojunction Architecture

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Thin-film transistors based on metal oxide semiconductors have become a mainstream technology for application in driving low-cost backplanes of active matrix liquid crystal displays. Although significant progress has been made in traditional marketable devices based on physical vapor deposition derived metal oxides, it has still been hindered by low yield and poor compatibility. Fortunately, developing solution-based 1D nanofiber networks to act as the fundamental building blocks for transistor has proven to be a simpler, higher-throughput approach. However, oxide transistors based on such princesses suffer from degraded carrier mobility and operational instability, preventing the ability of such devices from replacing present polycrystalline Si technologies. Herein, it is shown that double channel heterojunction transistors with high electron mobility (>40 cm^2 V^{-1} s^{-1}) and operational stability can be achieved from electrospun double channels composed of In_2O_3 and ZnO layers. Adjusting the stacking order and the stacking density of In_2O_3 and ZnO layers can effectively optimize the interface electron trap, leading to the formation of 2D electron gas and the reduction of stress-induced instability. These findings further elucidate the significant advance of electrospinning-derived double channel heterojunction transistors toward practical applications for future low-cost and high-performance electronics.

1. Introduction

In the past decades, metal oxide semiconductors (MOS) have been perceived as competitive channel components in thin-film transistors (TFTs) for next-generation displays owing to their excellent carrier mobility, high transparency, low manufacturing cost and good environmental stability.[1–4] Among these MOS candidates, 1D oxide semiconductor nanostructures, such as nanotube, nanowires and nanofiber networks (NFNs), have been widely explored as the fundamental building blocks for various technological applications owing to the size-confined physical properties and solving scaling limiting problem.[5–9] Up to now, considerable novel synthesis techniques have been devoted to the development of 1D nanomaterials, including chemical vapor deposition (CVD),[10] and solution-based process.[11] However, despite this progress, these fabrication schemes still suffer from different process-related disadvantages. CVD-based technique is incompatible with current large-scale manufacturing platform due to high fabricating cost and complicated preparation process. Although solution-derived thin-film electronics could partially satisfy the requirements for practical devices applications, it is still challenged by low yield and low yield and poor compatibility, limiting their practical utilizations. To realize thin-film electronics with large-scale and low-cost, further technological innovations in achieving thin-film are highly desired.

Among the different strategies for producing 1D building blocks, electrospinning is a straightforward, versatile and low cost route to produce continuous nanofibers with high specific surface area and uniform diameters.[12] Moreover, the electrospinning-based method usually exhibits some advantages over others, such as easy operation, high throughput, low fabrication cost and convenient assembly into films, which benefits the mass production and consumption of functional electronics. Recently, much progress in 1D MOS nanofibers has been achieved, especially in the emerging field of low-cost and disposable electronics. Among the MOS-based nanofibers developed to date, electrospun In_2O_3 and ZnO NFNs have been regarded as the representative examples of high-performance metal-oxide nanomaterials due to their high electron mobility and large bandgap for excellent transmittance in the visible region.[13,14] Currently, NFN-based TFTs with electron mobilities

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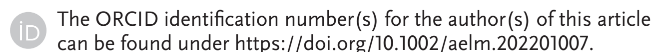
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in the range of 25 to 45 $cm^2 V^{-1} s^{-1}$ have been achieved, and demonstrated the great potential to meet all the stringent requirements in large-area, low-cost, and high-performance integrated circuits.[15–18] However, despite this potential, TFTs based on electrospun NFNs still suffer from operational instability and degraded carrier mobility, which can be attributed to charge trapping due to the non-stoichiometric nature and the inherent surface roughness of the electrospinning-grown nanofibers. All these reported works have indicated that electrical performance of the electrospun oxide NFN TFTs has to be further improved for the practical deployment.

Recently, a successful strategy for manufacturing high-performance oxide TFTs is based on the use of low-dimensional heterojunction (HJ) channels.[19,20] Among these HJ devices, conduction-band-offset- driven electron transfer and confinement occur at the heterointerface in a process similar to that observed in conventional AlGaAs/GaAs high electron mobility transistors (HEMTs).[22–25] In these devices, the formation of 2D electron gas (2DEG) near the heterointerface will lead to the reduced ionized impurity scattering and the increased carrier mobilities, exceeding those made of single oxide layer channels, which can be attributed to the transition of conduction mechanism from a trap-limited process to a percolation-limited process. To date, 2DEG HJ TFTs based on ZnO/ZnMgO and In_2O_3/ZnO heterojunctions are being investigated.[20–22,26–29] For instance, sputtering-derived MgZnO/ZnO HJ TFTs exhibit a higher mobility (≈84.2 $cm^2 V^{-1} s^{-1}$) than ZnO-only TFTs (≈1.5 $cm^2 V^{-1} s^{-1}$).[30] Anthopoulos[22] has observed a significant increase in the electron mobility and a dramatic change in the charge transport mechanism for the solution-driven In_2O_3/ZnO HJ TFTs. These pioneering results have indicated the potential application of oxide-based 2DEG technology in large-area thin-film electronics. Despite these amazing progress, its widespread applications in practical electronics is currently blocked by the complicated operation of vacuum-based method and the required high temperature solution manufacturing processes to ensure the heterointerface formation with high-quality. Inspired by the aforementioned electrospun NFNs, an intriguing question arises as to whether oxide heterointerfaces with high quality can be achieved based on electrospun oxide nanofibers. Zhai et al. have demonstrated that electrospun ZnO/SnO_2 HJ nanofibers are potential candidates for fully transparent high performance photodetectors.[31] Meanwhile, Chen et al. have declared that electrospun conjugated polymers with heterojunction configuration have demonstrated potential application in constructing TFTs with elevated mobilities.[32] Despite the progress, there are no related reports on the construction of oxide HJ TFTs based on electrospinning. Thus, developing electrospinning strategy to implement oxide-based HJ TFTs will help to overcome important bottlenecks related to the performance and manufacturing level of TFT technologies.

Herein, we report a stacked dual-channel (DC) HJ TFTs Transistors consisting of alternating layers of In_2O_3 and ZnO treated by electrospinning. By carefully designing the TFT channel architecture and changing the stacking density in both nanofibers, significant enhancement in both the electron mobility and TFT stress stability have been observed. Results have revealed that HJ TFTs based on ZnO/In_2O_3 (Z-On-I) configuration show higher electron mobility than these TFTs made of In_2O_3/ZnO (I-On-Z) HJ configuration due to the enhanced 2DEG and the reduced interface state density. By using the resistor load inverter based on ZnO/In_2O_3/Al_2O_3 TFT, the practical application of low-voltage operation logic circuit has obtained high voltage gain and excellent swing characteristics. The findings of this work bring a new perspective to the design principle of the next generation high-performance electrospun HJ TFT.

2. Results and Discussion

2.1. Characterizations of Electrospun Stacked Nanofibers

We have recently shown the capability to grow continuous and uniform high-quality In_2O_3 nanofiber networks (NFNs) by electrospinning a suitable precursor solution.[33] Herein, by using the solution-based strategy, we deposited In_2O_3 and ZnO stacked NFNs with different stack order on Al_2O_3/p+-Si substrates by electrospinning of precursors comprising $In(NO_3)_3 \cdot xH_2O$ and $Zn(NO_3)_3 \cdot 5H_2O$ in *N,N*-dimethylformamide (DMF), integrating bottom-gate, top-contact (BG-TC) double-channel (DC) TFTs based on aluminum (Al) source-drain (S-D) electrodes. Schematic diagram of manufacturing process for DC NFN TFTs is shown in Figure S1 (Supporting Information). As-electrospun DC NFNs (I-On-Z and Z-On-I) with diameters of 100–200 nm are found to be randomly distributed to form a 3D network structure as determined by scanning electron microscope with different magnification (**Figure 1**a,b). Due to the terrible adhesion performance between NFNs and the gate dielectric, poor electronic contact and high interfacial state density will lead to the degraded device performance inevitably.[13] The optimization of NFNs adhesion with substrates has been achieved based on UV-exposure combined with an annealing treatment. To investigate the feasibility of this approach, we treated the as-electrospun DC NFNs using UV irradiation and annealing. It can be seen that this treatment reduces their diameters of these NFNs with uniform morphology to a critical dimension (Figures S2 and S3, Supporting Information), which can be attributed to the release of the volatile molecules and the decomposition of organic polymer. This finding are also confirmed by the corresponding magnified view of SEM images of single In_2O_3 and ZnO nanofiber, as displayed in Figure 1c.

To further investigate the microstructure of nanofibers, the transmission electron microscope (TEM) and high resolution TEM (HRTEM) images were shown in **Figure 2**. The low magnification TEM images clearly show smooth and straight individual nanofibers (Figure 2a–e). The enlarged area of HRTEM images reveals the coexistence of the crystalline In_2O_3 and ZnO in the In_2O_3-ZnO stacked nanofibers (Figure 2b,c,f,g). The fast fourier transformation (FFT) of Figure 2b–f (Figure 2d–h) compare the calculated lattice spacing value with the theoretical values and indicate the formation of the polycrystalline NFNs, confirmed by elemental mapping and x-ray diffraction (XRD) (Figure 2j). The stacked NFNs after treatment presented two fiber composite phases, suggesting the formation of cubic phase of In_2O_3 and wurtzite structure of ZnO layers.[33,34] In current work, the reason why to choose 500 °C for annealing can be noted from the detailed analysis of the thermogravimetric (TG) curve (Figure S4, Supporting Information). Based

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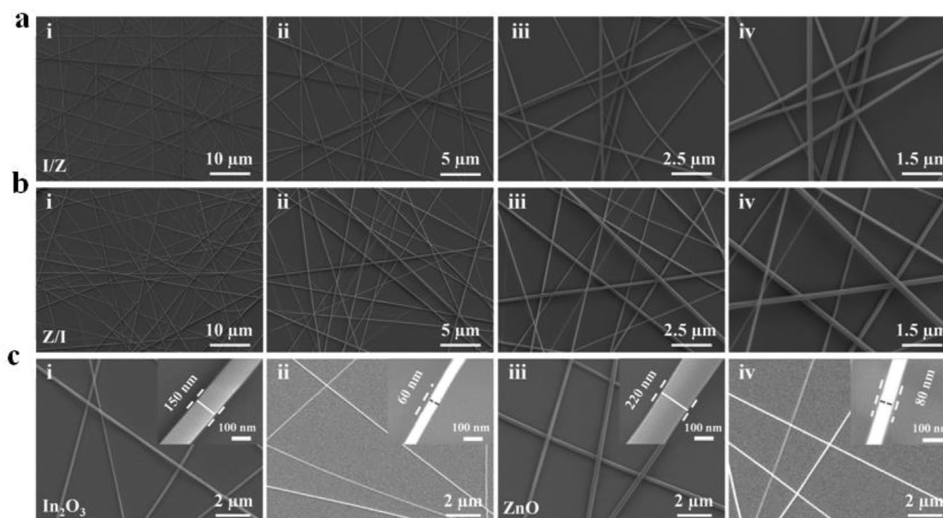

Figure 1. SEM images of as-electrospun DC NFNs. a) I-On-Z and b) Z-On-I configurations with different magnification. c) SEM images before and after UV and annealing treatment of single In_2O_3 (i,ii) and ZnO (iii,iv) NFNs. The inserts in c show the corresponding individual nanofiber images.

on all the findings, it can be evident that each nanofiber is composed of single phase of either the In_2O_3 or the ZnO phase, rather than the solid-solution phase of In_2O_3-ZnO. The scanning TEM (STEM) images of the stacked NFNSs obtained with elemental mappings (Figure S5, Supporting Information) show high uniformity of component distribution, suggesting the realization of In_2O_3-ZnO HJ nanofibers with high-quality and their potential applications in electronic devices.

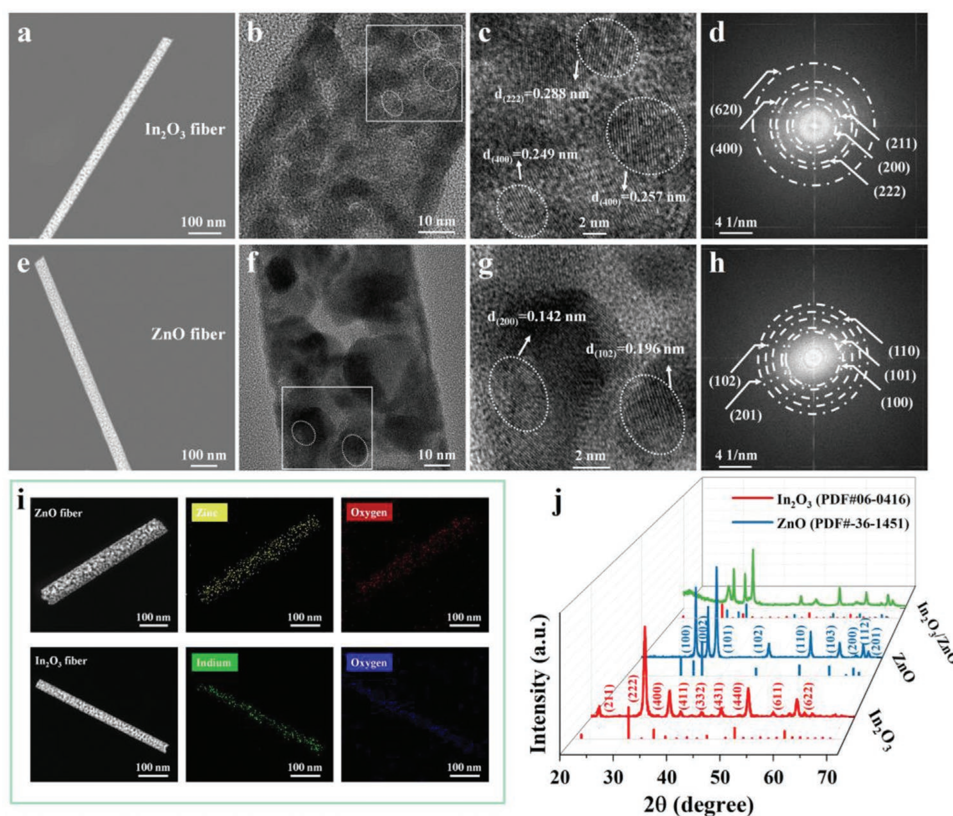

Figure 2. Low- magnification TEM images of a) In_2O_3 and e) ZnO nanofibers. HRTEM images of b,c) In_2O_3 and f,g) ZnO nanofibers. d,h) FFT images of figure b and f. i) The corresponding elemental mapping of In_2O_3 and ZnO nanofibers. j) XRD patterns of In_2O_3 and ZnO nanofibers annealed at 500 °C for 2 h.

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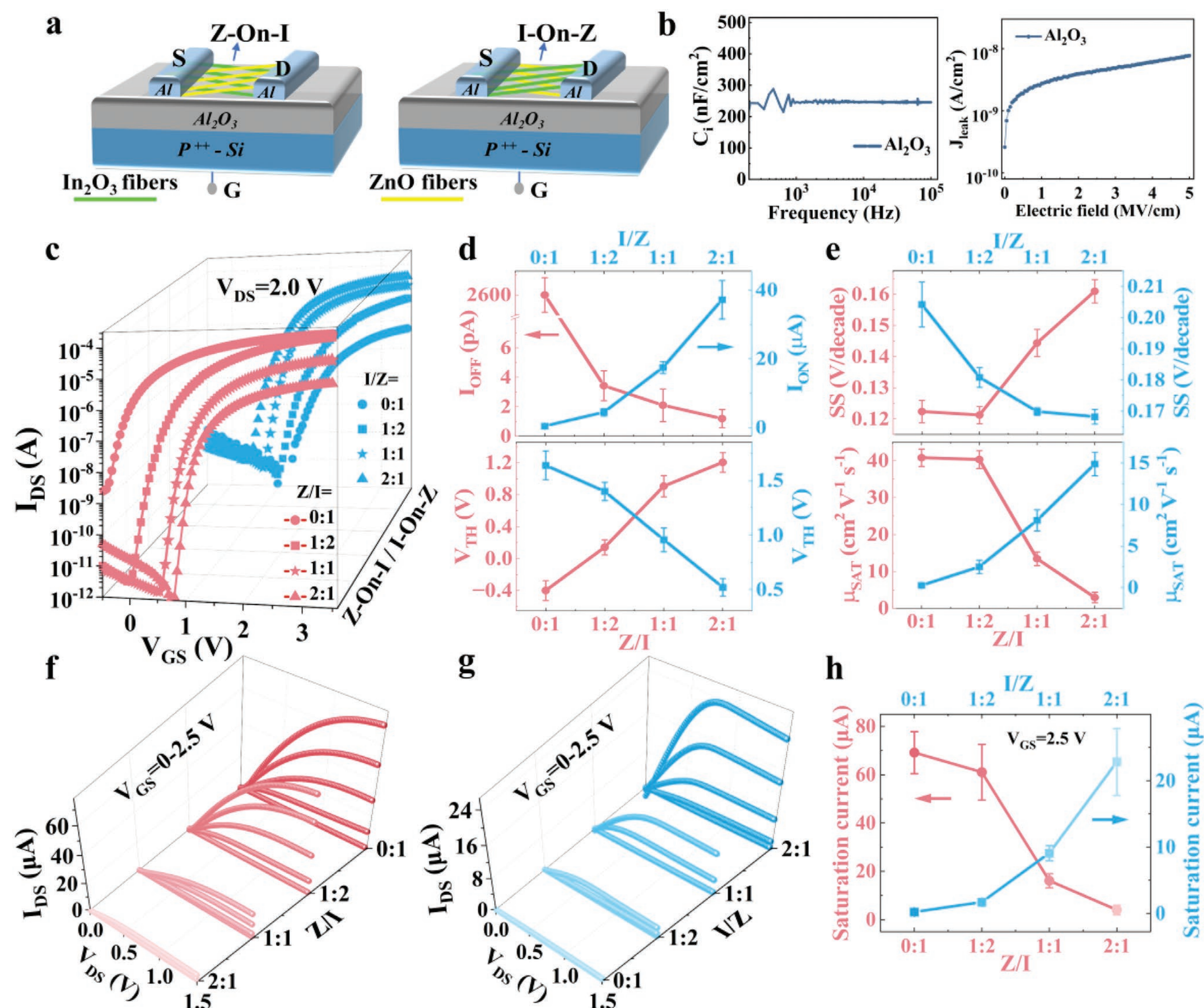

Figure 3. a) Model diagram of DC NFN TFTs for Z-On-I and I-On-Z. b) Areal capacitance and leakage-current density of Al_2O_3 dielectric layer. c) Transfer characteristic curves for Z-On-I and I-On-Z TFTs with various proportions of Z/I and I/Z. d,e) Corresponding I_{ON}, I_{OFF}, V_{TH}, SS, and μ_{SAT} of Z-On-I and I-On-Z TFTs devices. f,g) Output characteristics of Z-On-I and I-On-Z TFTs with various proportions of Z/I and I/Z. h) Saturation current at a V_{GS} of 2.5 V for Z-On-I and I-On-Z TFTs.

2.2. Performance Regulation of DC NFNs based TFTs

To investigate the performance evolution of electrospun DC NFNs TFTs, we fabricated BG-TC TFTs employing DC NFNs with different stacking order. **Figure 3**a demonstrates schematics of the various TFT architectures, consisting of Z-On-I (left) and I-On-Z (right) DC NFNs being integrated onto Al_2O_3/Si substrate. In general, the electrical properties of TFTs devices not only depend on the semiconductor layer, to some extent, the existence of a high-quality gate dielectric layer can optimize the device performance. Atomic layer deposition (ALD) derived Al_2O_3 layer was chosen to act as the gate dielectrics. The larger area capacitance density of 250 nF cm^{-2} at a frequency of 20 Hz and smaller leakage current density of 5×10^{-9} A cm^{-2} at 2.0 MV cm^{-1} guarantee its potential application in TFT devices (Figure 3b).[33,35] Figure 3c shows the transfer characteristics for Z-On-I and I-On-Z DC NFN TFTs with different stacking order and different stacking density ratios (Z/I and I/Z), in which all devices exhibit a typical *n*-type characteristics. More importantly, all the devices performance can be optimized significantly by adjusting the ratio of the upper and lower oxide nanofibers of Z-On-I and I-On-Z DC NFNs, respectively. Especially, all devices performance varies from single channel (SC) In_2O_3 NFN to SC ZnO NFN and in between (Figure S6, Supporting Information). This provides a feasibility to balance the electrical performance of a SC by stacking two different oxide NFNs with different stacking density.

Figure 3d,e summary the functional relationship between electrical performance parameters and proportion of stacked nanofibers, in which these parameters are extracted from

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10 devices. For devices with Z-On-I architecture, with increasing the top ZnO fibers density, the reduced I_{ON} and I_{OFF} have been detected. The calculated saturation mobility (μ_{SAT}) decreases from 40.80 to 2.96 $cm^2 V^{-1} s^{-1}$and V_{TH} changes from –0.4 to 1.2 V, indicating the working mode from depletion to enhancement type. These findings suggest that DC NFN TFTs have the electrical characteristics of two different oxides, which offset and optimize each other, and the ZnO nanofibers layer plays an important regulatory role. It can be noted that Z-On-I devices with Z/I of 1/2 demonstrate the optimized electrical performance, including a high μ_{SAT} of 40.32 $cm^2 V^{-1} s^{-1}$, a low V_{TH} of 0.14 V, a large I_{ON}/I_{OFF} of 4.7×10^7 and a small SS of 0.12 V/decade. Correspondingly, for I-On-Z TFTs, with the increase of the proportion of In_2O_3 fibers, the device performance is close to that of In_2O_3 and I-On-Z TFTs with I/Z of 2:1 display the best optimized performance. However, from the perspective of using In_2O_3 to adjust ZnO layer, the proportion of In_2O_3 NFNs should not exceed that of main ZnO NFNs, leading to the acceptable and optimal I/Z ratio of 1:1. However, it cannot be ignored that fixing the same stacking density ratios, Z-On-I TFTs have a more outstanding performance compared to that of I-On-Z TFTs with different stacking order. Therefore, it can be inferred that Z-On-I architecture can be selected to act as the optimal stacking NFNs for constructing DC TFTs. Figure 3f,g present representative sets of output characteristics measured for Z-On-I and I-On-Z DC NFNs TFTs. It can be noted that the output characteristic is enhanced with increasing the In_2O_3 nanofiber content, reflected by the saturation current at a V_{GS} of 2.5 V (Figure 3h). It is obvious that highly conductive In_2O_3 nanofibers are beneficial to the promotion of the current. More detailed electrical performance parameters of these TFTs are summarized in Table S1 (Supporting Information). Electrical performance parameters after regulation are much better than the previous reported SC NFN FETs (Table S2, Supporting Information), suggesting that DC NFNs structure seems to be more effective and accurate to tune the performance of the TFT devices, compared with the traditional doping modification.

Further experimental evidence on the existence of completely different electron transport mechanisms between DC TFTs and SC TFTs has been observed. As well known, when a gate voltage V_{GS} is provided, a large number of carriers (electrons or holes) will be induced to form a channel with thickness of about several nanometers between the semiconductor layer and the dielectric layer. **Figure 4**a displays the electronic transmission mechanism of the DC TFT under operation. Under the action of V_{GS}, the electrons are gathered at the Al_2O_3 interface. Meanwhile, a suitable V_{DS} is applied between source and drain electrodes, and the current loop is formed between the channel and the electrode. Figure 4b shows the off-state and on-state primary electronic transmission path in Z-On-I and I-On-Z NFN TFTs. When V_{GS} is less than V_{TH} ($0 < V_{GS} < V_{TH}$), the conductive channel located on the interface between the lower fibers and Al_2O_3 layer is in a high-resistance state and closed before the device is turned on. Under these conditions, the I_{OFF} paths are in the top channel layer, as shown by the purple arrow. On the other hand, when the device is in the active state ($V_{GS} > V_{TH}$), the electrons are repulsed to the Al_2O_3 interface at the positive voltage.[36–38] At this point, the paths of I_{ON} are shown by the red arrow. Regardless of the stacking method, the I_{OFF} is determined by the free electron density (N_e) of the upper layer and

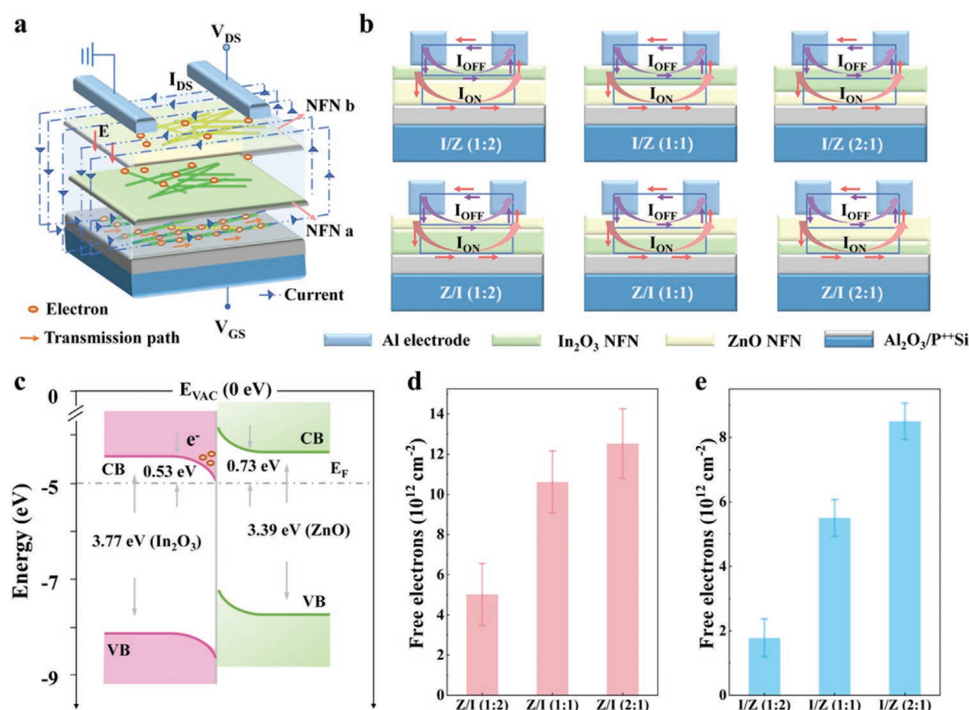

Figure 4. a) Schematic diagram of electronic transmission model of DC HJ NFN TFTs. b) The main electronic transmission paths in on and off states of DC TFTs. c) The energy band diagram for the DC HJ structure. The areal density of electron in d) Z-On-I and e) I-On-Z configuration with different stacking density.

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the stacking density of the upper fibers. Furthermore, the I_{ON} and μ_{SAT} are directly proportional to the N_e of the entire active layer, which is consistent with the behavior of the transfer curves displayed in Figure 3c.

It must be noted that for Z-On-I structure, the μ_{SAT} is extremely excellent at Z/I of 1:2, similar to that of SC In_2O_3. The performance has been previously related to the existence of a 2DEG near the ZnO/In_2O_3 heterointerface, where the Fermi energy (E_F) alignment between ZnO and In_2O_3 in contact leads to band bending (Figure 4c). The calculation and extraction of the values are displayed in Figure S7 (Supporting Information). In general, 2DEG could provide the high mobility of the anterior channel and reduce the I_{OFF} of the posterior channel. In addition, it could lower the carrier scattering and improve the mobility.[3,32] This is clearly affected by interfacial 2DEG in Z-On-I and I-On-Z configuration with the same proportion of In_2O_3 and ZnO nanofibers, and the differences between them will be discussed in the next section.

Interestingly, the turn-on voltage (V_{ON}) and SS are determined by the lower nanofibers in both Z-On-I and I-On-Z stacking modes. They deviate from the value of SC devices as the stacking density of the underlying nanofibers decreases, and close to the value of SC devices composed of the upper nanofibers. In fact, this shift is still correlated with the evolution of N_e in the channel. By using the following formula,[21] the N_e alterations have been estimated taking the difference in the V_{TH} between Z-On-I and I-On-Z and SC In_2O_3 and ZnO NFNs, respectively.

$$\Delta e = \frac{C_i |\Delta V_{TH}|}{q} \quad (1)$$

where C_i is the gate oxide capacitance per unit area and q is the elementary charge. Analyses from on Equation (1) yield the areal density of excess electrons for Z-On-I and I-On-Z DC NFN TFTs, respectively (Figure 4d,e). It can be noted that N_e can be adjusted by modifying the stacking density of the upper nanofibers in DC configuration.

After interchanging the stacking order of the DC nanofibers, it can be noted that the performance of the device has been adjusted greatly. In the process of modulation, the optimized performance of DC HJ TFTs has been observed in Z-On-I TFTs with Z/I of 1:2 and 1:1, respectively.

To explore and explain this transition, the 2DEG between ZnO/In_2O_3 HJ interfaces and the interface state density (N_i) of the nanofibers are linked. Compared to I-On-Z structure, the Z-On-I configuration with a 2DEG system, charges accumulate at the interface, leading to the elevated μ_{FE} and I_{ON}. When the two oxides contact with each other, electrons transfer from ZnO to In_2O_3, and the surplus holes and electrons produce a built-in electric field (E_{BI}) at the HJ interface, leading to the energy band bending. The 2DEG in the confined triangular potential well is expected to be delocalized along the channel plane on the In_2O_3 side, but is limited in the out-of-plane (z) direction.[20,39–41] For Z-On-I, the positive gate voltage is identical to E_{BI} at the ZnO/In_2O_3 HJ interface, and the potential well depth increases, thus increasing the 2DEG concentration. The enhanced 2DEG will form an electronic transmission path at ZnO/In_2O_3 HJ interface, which cooperates with the back channel to optimize the electrical performance. However, at a low gate voltage, the 2DEG provides very limited carriers. However, for I-On-Z configuration with In_2O_3/ZnO HJ interface, the gate voltage will reverse with E_{BI}, inhibiting the accumulation of 2DEG (Figure S8, Supporting Information). In comparison, the 2DEG effect on I-On-Z is limited,[42,43] resulting in lower I_{ON} and μ_{SAT} and a positive shift of V_{TH}. About the effect of 2DEG between fiber networks on HJ TFTs, more work will be needed to deeply understand the detailed mechanism.

Figure 5a shows the atomic force microscopy (AFM) of In_2O_3 (i and ii) and ZnO (iii and iv) nanofibers, respectively. Smoother In_2O_3 nanofibers than ZnO nanofibers have been observed, leading to the improved electrical performance confirmed by previous reports.[20,44] In addition, the chemical states of the nanofibers were analyzed by x-ray photoelectron spectroscopy (XPS) (Figure 5b,c; Figure S9, Supporting Information). As shown in Figure 5b,c, the O 1s peaks can be deconvoluted into three subpeaks, which may be due to oxygen bound to metal (O_i, M—O—M,), oxygen vacancy (O_{ii}, V_O), and hydroxyl groups (O_{iii}, M—OH), respectively.[45,46] The surface of M—OH is well known for the carrier trap and captures electrons. The O_{iii} ratio of 9.4% in In_2O_3 is much lower than of ZnO (15.5%), providing a strong proof of the poor surface state of ZnO NFNs.

The N_i, consisting of surface roughness, M—OH bonding state, and some other factors, can be extracted from equation $N_i = \left[\frac{SSlog(e)}{KT/q} - 1 \right] \frac{C_i}{q}$, where K and T are the Boltzmann constant and the absolute temperature.[47] Figure 5d shows the extracted N_i for devices with different HJ configuration. It can be noted that N_i increases with increasing density of ZnO nanofibers, which is extremely evident in the case of I-On-Z structure. In fact, to evaluate the effect of 2DEG and N_i on the electrical performance, we can estimate the relative mobility of Z-On-I to I-On-Z, which have the same proportion of In_2O_3 and ZnO fibers density (Figure S10, Supporting Information). As a result, it can be observed that the mobility in Z-On-I is larger than that of I-On-Z, suggesting the formation of more 2DEG and less N_i in Z-On-I structure.

To further understand the interface trap density and reliability of the DC HJ NFN TFTs, low-frequency noise (LFN) measurements were carried out with a fixed gate overdrive voltage (V_{GS}–V_{TH}) of 1.0 V as well as V_{DS} of 2.0 V as shown in Figure 5e,f. At low drain voltage, the carrier density distributes uniformly along the channel, implying that LFN can demonstrate the average defect density of the entire channel region.[48] Based On LFN measurements, it can be noted that DC HJ NFN TFTs conforms to the classical $1/f$ noise theory in the fixed frequency range.[10,48,49] Observably, compared with I-ON-Z TFTs, the normalized drain current noise spectral density (S_{ID}/I_{DS}^2) of I-ON-Z TFTs demonstrate a reduced trend, suggesting that the average trap density and interface trap density for I-ON-Z TFTs are reduced. To further confirm the main source of LFN of DC HJ TFTs, normalized S_{ID}/I_{DS}^2 properties were estimated and demonstrated in Figure 5g,h. In general, the mobility fluctuation ($\Delta\mu$) model and carrier number fluctuation (ΔN) model have been adopted to explain the origin of the $1/f$ noise.[50,51] Here, the carrier number fluctuation model as well as mobility fluctuation model (ΔN–$\Delta\mu$) is mostly used to analyze the LFN in DC NFN TFTs.[49,51] The slope values extracted from Figure 5g,h

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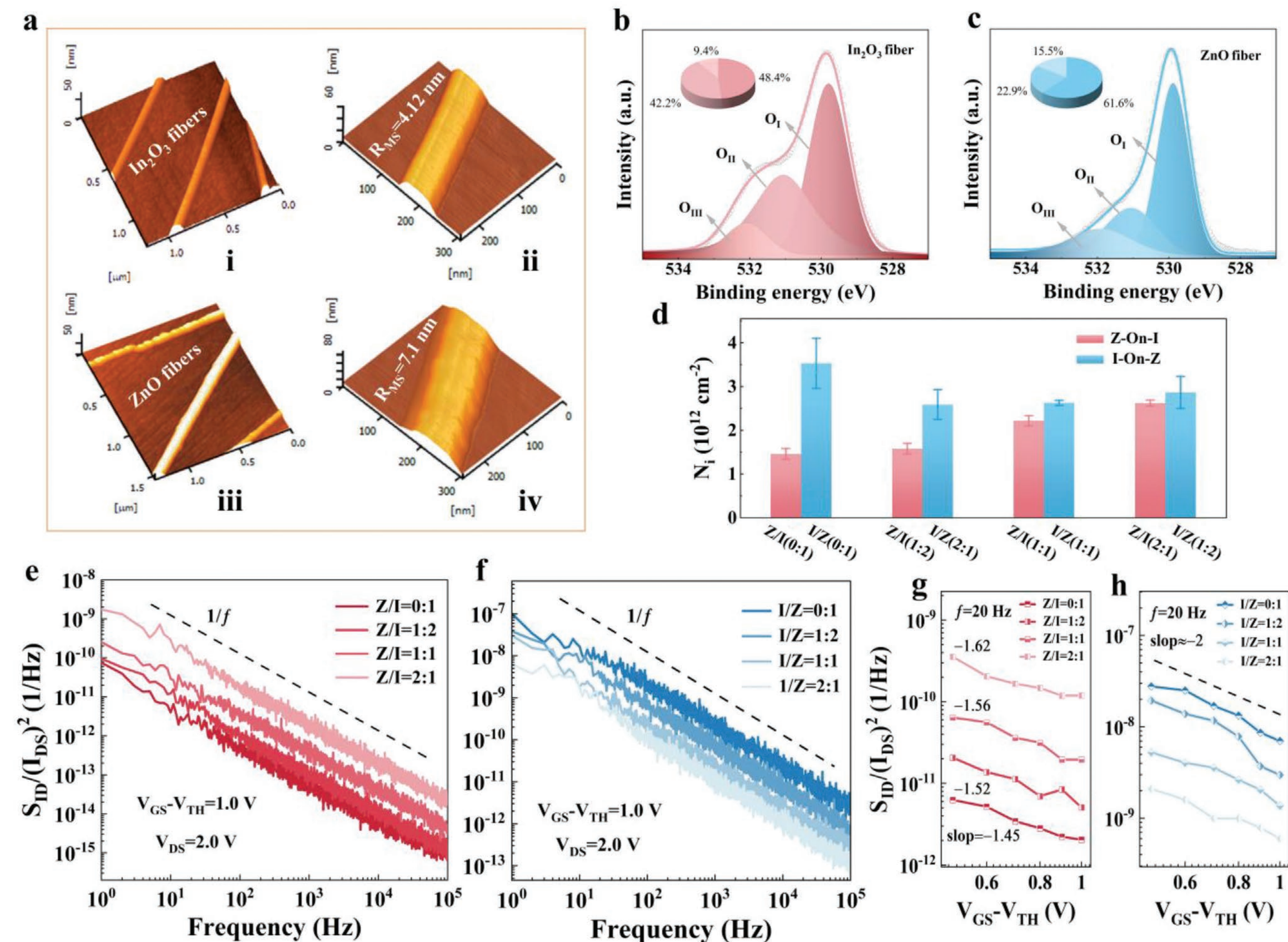

Figure 5. a) AFM images of nanofibers. O 1s XPS spectra of b) In_2O_3 and c) ZnO nanofibers. d) N_i of DC HJ TFTs with different ratio of I/Z and Z/I. Normalized LFN spectra of e) DC Z-On-I and f) DC I-On-Z TFTs at V_{GS}-V_{TH} = 1.0 V and V_{DS} = 2.0 V. The normalized $S_{ID}/(I_{DS})^2$ curves as a function of (V_{GS}–V_{TH}) for g) DC Z-On-I and h) DC I-On-Z TFTs at f = 20 Hz.

are about between –1.4 and –2, indicating the feasibility of ΔN–Δμ model. Therefore, the carrier number fluctuation attributed to the capture and release of carriers by defect traps at the interface and localized states leads to the main source of 1/*f* noise. For device, local electrons in the conduction band tail state at low V_{GS} can affect carrier capture and release on mobility more strongly than at the interface.[52] In this case, Δμ dominates the 1/*f* noise. Correspondingly, when providing the over V_{GS}, the fermi level rises to the conduction band, leading to an increase in the channel carriers, which facilitates the capture of the interface trap carriers.[53] Here, ΔN dominates the 1/*f* noise. Note that in Z-On-I device, the slopes value shift from –1.45 to –1.62 with an increasing In_2O_3 density ratio, which may be caused by HJ 2DEG. The physical distance between 2DEG and the gate dielectric surface is expected to suppress both long-range coulomb scattering by trapped charges and short-range scattering from dielectric surface topological imperfections and chemical defects,[32] which seems to weaken the dominant role of ΔN on 1/*f* noise. The various slope values of the I-On-Z are maintained around –2, indicating more ZnO nanofibers interface defects, confirmed by previous XPS and AFM results.

2.3. Reliability Evolution and Application of DC HJ TFTs

Besides their high electron mobilities and the reduced interface trap density, the DC HJ TFTs with Z-ON-I configuration are also expected to exhibit improved bias stability, which is another key figure of merit for their practical applications. Here, we subjected both transistors (Z/I of 1:2 and 1:1) to a continuous positive bias stress (PBS), negative bias stress (NBS) and negative bias illumination stress (NBIS), respectively. **Figure 6**a–d present the transfer characteristics for both devices measured during PBS and NBS operation. Remarkably, the associated PBS and NBS-induced shifts in V_{TH} (ΔV_{TH}) for Z-ON-I TFTs with Z/I of 1:1 are comparatively larger than those of Z-ON-I TFTs with Z/I of 1:2, indicating an improved stability behavior for TFTs with Z/I of 1:2. The smaller ΔV_{TH} demonstrates the existence of less trapped charges at the dielectric and channel interface during PBS and NBS, confirmed by previous N_i characterization.

We have shown that an NBS-stable Z-ON-I DC HJ TFTs can be created by eliminating interface defect states and trapped charges. However, in practical application, TFTs are exposed

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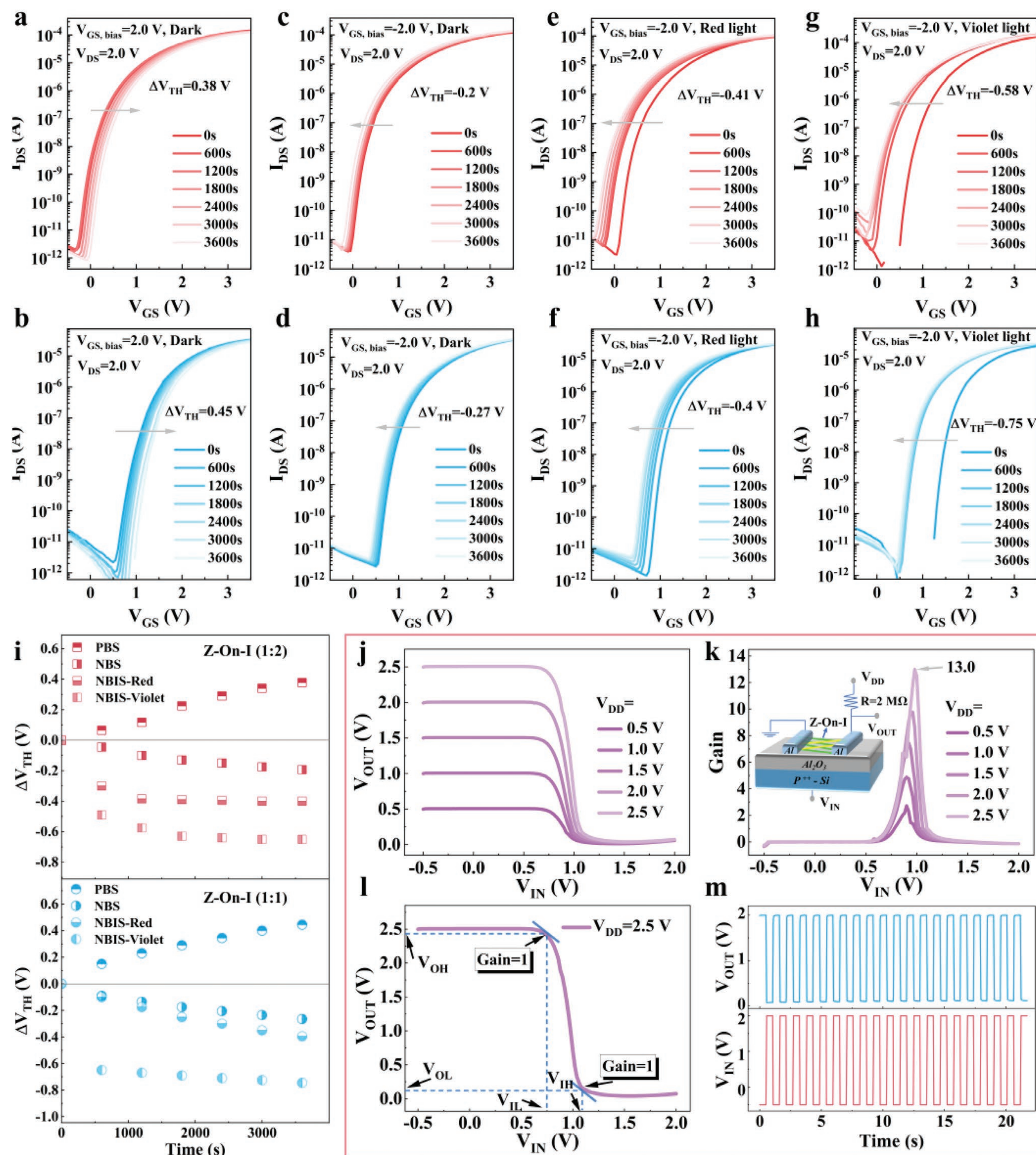

Figure 6. a,b) PBS, c,d) NBS, e,f) NBIS-Red and g,h) NBIS-Violet of DC HJ Z-On-I TFTs with Z/I of 1:2 and 1:1, respectively. i) Corresponding changes in threshold voltage (ΔV_{TH}) for the Z-On-I TFTs with Z/I of 1:2 and 1:1shown in figure a–h. j) VTCs, k) voltage gains and schematic diagram of the resistor-loaded inverter based on the Z-On-I (1:2) TFT. l) The noise margin extracted from the VTC curve at V_{DD} = 2.5 V) The dynamic response behavior under AC square wave signal at 1 Hz.

to much light illumination stresses. Herein, NBIS measurements were carried out to investigate the stability of Z-ON-I DC HJ TFTs with different Z/I ratios (Figure 6e–h). Commercially, NBIS instability is not as problematic as NBS and PBS because it can be easily overcome by using a light-shielding layer. However, for fully transparent electronic products, NBIS is a problem that should be solved soon. Compared to NBS, the ΔV_{TH} for TFTs is more pronounced during prolonged light

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exposure, especially in purple light. Obviously, the impact of light illumination on the TFTs device is beyond doubt. Three models have been adopted to give plausible explanations of the instability behavior of the TFTs device under NBIS. Ambient interaction model is often used to explain the NBIS instability for devices, in which oxide layers are exposed to the atmosphere.[54] In addition to H_2O releasing electrons on the surface, desorption of adsorbed O_2 increases the carrier in the channel is also the source of negative ΔV_{TH}.[54–56] This interpretation seems plausible for nanofibers with a large specific surface area. Based on the oxygen-vacancy model, V_O in the ground state transforms into an excited state of V_O^{2+} under light excitation, which will serve as a shallow state to provide delocalized free electrons for the conduction band.[54,57,58] Sufficient V_O in the nanofibers will provide conditions for excitation, leads to a pronounced shift under red and violet light. The hole-trapping model is the third models.[49,47,59] At a large gate bias stress, the holes generated by light excitation are captured by the V_O or injected into the dielectrics, causing the negative ΔV_{TH}. However, relative to violet light, electron-hole pairs are not easily generated by red light. Therefore, much larger instability under violet light has been observed.

The evolution of ΔV_{TH} for Z-ON-I DC HJ TFTs with different channel configurations under PBS, NBS, and NBIS is displayed in Figure 6i. Noticeably, the Z-ON-I (1:1) DC HJ TFT suffers severe degradation caused by PBS (NBS), as evidenced by the larger ΔV_{TH}. Increasing the stacking density of the bottom In_2O_3 layer (1:2) decreases the bias-stress effect, as the larger I_{ON} has been observed, as compared to Z-ON-I (1:1) TFT. In addition, it is interesting to see that a change has occurred in the NBIS by adjusting the stacking density of DC HJ TFTs. Ignoring the NBIS behavior under red light (the difference in ΔV_{TH} between Z-ON-I (1:1) and Z-ON-I (1:2) TFT is only 0.01 V), the ΔV_{TH} of Z-ON-I (1:2) TFT achieves smaller values under violet light. Furthermore, we attributed the relatively low NBIS stability of Z-ON-I (1:1) TFT to its higher defect states and lower free electron density. As a result, it can be concluded that the bias stability of the Z-ON-I DC HJ TFTs can be optimized by adjusting the stacking density of top and bottom layer, yielding transistors with high stress stability.

To explore the potential application of DC HJ NFN TFTs in logic circuits, the Z-ON-I TFT (Z/I = 1:2) with optimized electrical performance was selected to construct a resistor-loaded inverter by connecting the external load resistance of 2 MΩ (See the inset in Figure 6k). The typical voltage-transfer characteristics (VTCs) of the inverter are shown in Figure 6j, where the output high voltage (V_{OH}) is close to the supply voltages (V_{DD}), while the output low voltage (V_{OL}) is close to 0 V. This benefits from the low off-state current of TFT and good negative bias stability, allowing that the inverter can effectively convert the input voltage signal and display good full swing characteristics.[60,61] Moreover, a sufficiently low subthreshold swing can ensure a good gain for the inverter.[49] Figure 6k shows the voltage gain values ($-\partial V_{OUT}/\partial V_{IN}$) under different V_{DD}. Note that the extracted voltage gain has been found to increase with the increased V_{DD}. The extracted maximum gain of 13.0 at V_{DD} = 2.5 V exceeds the minimum voltage gain required to drive the logic circuit components. Compared to the inverters based on NFN TFTs reported in recent years (Table S3, Supporting Information), the gain of 5.2 per unit voltage in this work is excellent enough. Noise margins (low-level noise and high-level noise margins) are also important parameters to describe the static characteristics of the inverter. As shown in Figure 6l, the high-level noise margins ($N_{MH} = V_{OH}$-V_{IH}) and low-level noise margins ($N_{ML} = V_{IL} - V_{OL}$) of the inverter are determined to be 1.32 and 0.57 V at V_{DD} = 2.5 V, respectively. The ratio of N_{MH} to the V_{DD} (52.8%) is higher than that required for logic circuit application (30%), indicating a strong anti-inverter interference ability and keeping the logic accuracy within a certain range.[60] To obtain the alternative current (AC) characteristic of the inverter, the dynamic response behavior under AC square wave signal was carried out and demonstrated in Figure 6m. The output signal responds well to the input square wave signal, showing its possible applications in complex logic circuits.[16,62] The low operating voltage and full swing characteristic have turned out to be an effective way to construct low power logic electronic devices by using DC HJ NFN TFTs.

3. Conclusions

In summary, we have developed electrospinning-driven DC NFN architectures by adjusting the stacking order and the stacking density of In_2O_3 and ZnO layers. DC NFN TFTs based on Z-On-I and I-On-Z configurations were implemented, which produced excellent electrical performance, including high electron mobility (>40 cm^2 V^{-1} s^{-1}) and operational stability. The successful design strategy in our devices originates from the improved 2DEG and the reduced N_i in Z-On-I HJ architecture. The adjustment of the stacking density of NFNs has been shown to enable controlled density of electron of the DC HJ TFTs, providing additional modification over the characteristics of these high-electron-mobility TFTs. Bias and illumination-stress stability characterizations, combined with LFN analysis, have indicated that the DC HJ design can effectively eliminate the operational instability of SC while maintaining a high-performance device. Successful integration of resistor-loaded inverter with excellent logic capabilities implied the potential application of DC HJ NFN TFTs in future logic electronics. Our electrospinning-derived DC HJ design strategy could potentially solve the inherent shortcomings of SC TFTs s and provide a feasible and reliable route in building TFTs with operating characteristics exceeding the current state of the art.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D electron gas, double-channel, electrospinning, heterojunction transistors, nanofiber networks

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[1] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.
[2] C. P. T. Nguyen, J. Raja, S. Kim, K. Jang, A. H. T. Le, Y.-J. Lee, J. Yi, *Appl. Surf. Sci.* **2017**, *396*, 1472.
[3] J. L. Shi, J. Y. Zhang, L. Yang, M. Qu, D.-C. Qi, K. H. L. Zhang, *Adv. Mater.* **2021**, *33*, 2021.
[4] M. Lorenz, M. S. R. Rao, T. Venkatesan, E. Fortunato, P. Barquinha, R. Branquinho, D. Salgueiro, R. Martins, E. Carlos, A. Liu, F. K. Shan, M. Grundmann, H. Boschker, J. Mukherjee, M. Priyadarshini, N. DasGupta, D. J. Rogers, F. H. Teherani, E. V. Sandana, P. Bove, K. Rietwyk, A. Zaban, A. Veziridis, A. Weidenkaff, M. Muralidhar, M. Murakami, S. Abel, J. Fompeyrine, J. Zuniga-Perez, R. Ramesh, et al., *J Phys D Appl Phys.* **2016**, *49*, 433001.
[5] T. Y. Zhai, X. S. Fang, M. Y. Liao, X. J. Xu, H. B. Zeng, B. Yoshio, D. Golberg, *Sensors* **2009**, *9*, 6504.
[6] J. Yoon, H. Jung, J. T. Jang, J. Lee, Y. Lee, M. Lim, D. M. Kim, D. H. Kim, S.-J. Choi, *J. Alloys Compd.* **2018**, *762*, 456.
[7] H.-C. Liu, Y. -C. Lai, C.-C. Lai, B.-S. Wu, H.-W. Zan, P. C. Yu, Y.-L. Chueh, C.-C. Tsai, *ACS Appl. Mater. Interfaces* **2015**, *7*, 232.
[8] Y. Meng, K. H. Lou, R. Qi, Z. D. Guo, B. Shin, G. X. Liu, F. K. Shan, *ACS Appl. Mater. Interfaces* **2018**, *10*, 20703.
[9] Z. Zheng, L. Gan, T. Y. Zhai, *Sci. China Mater.* **2016**, *59*, 200.
[10] D. Wan, A. Abliz, M. Su, C. S. Liu, C. Z. Jiang, G. L. Li, H. P. Chen, T. L. Guo, X. Q. Liu, L. Liao, *IEEE Electron Device Lett.* **2017**, *38*, 1540.
[11] H. Wu, C. Y. Hou, G. Z. Shen, T. Liu, Y. L. Shao, R. Xiao, H. Z. Wang, *Nano Res.* **2018**, *11*, 5866.
[12] J. J. Xue, T. Wu, Y. Q. Dai, Y. N. Xia, *Chem. Rev.* **2019**, *119*, 5298.
[13] Y. Meng, G. X. Liu, A. Liu, Z. D. Guo, W. J. Sun, F. K. Shan, *ACS Appl. Mater. Interfaces* **2017**, *9*, 10805.
[14] G. Cadafalch Gazquez, S. Lei, A. George, H. Gullapalli, B. A. Boukamp, P. M. Ajayan, J. E. T. Elshof, *ACS Appl. Mater. Interfaces* **2016**, *8*, 13466.
[15] H. C. Zhang, Y. Meng, L. F. Song, L. Q. Luo, Y. B. Qin, N. Han, Z. X. Yang, L. Liu, J. C. Ho, F. Y. Wang, *Nano Res.* **2018**, *11*, 1227.
[16] C. Seung-Hoon, J. Bong-Hoon, P. Jin-Seong, D. Renaud, T. H. L , K. Il-Doo, *ACS Nano* **2014**, *8*, 2318.
[17] M. Belyaev, V. Putrolaynen, A. Velichko, N. Markova, *ECS. J. Solid State Sci.* **2016**, *5*, Q92.
[18] Z. Wang, Y. Meng, Y. C. Cui, C. X. Fan, G. X. Liu, B. Shin, D. J. Feng, F. K. Shan, *Nanoscale* **2018**, *10*, 14712.
[19] D. Khim, Y.-H. Lin, S. Nam, H. Faber, K. Tetzner, R. P. Li, Q. Zhang, J. Li, X. X. Zhang, T. D. Anthopoulos, *Adv. Mater.* **2017**, *29*, 1605837.
[20] D. Khim, Y.-H. Lin, T. D. Anthopoulos, *Adv. Funct. Mater.* **2019**, *29*, 1902591.
[21] Y.-H. Lin, W. Li, H. Faber, A. Seitkhan, N. A. Hastas, D. Khim, Q. Zhang, X. X. Zhang, N. Pliatsikas, L. Tsetseris, P. A. Patsalas, D. D. C. Bradley, W. Huang, T. D. Anthopoulos, *Nat. Electron.* **2019**, *2*, 587.
[22] H. Faber, S. Das, Y.-H. Lin, N. Pliatsikas, K. Zhao, T. Kehagias, G. Dimitrakopulos, A. Amassian, P. A. Patsalas, T. D. Anthopoulos, *Sci. Adv.* **2017**, *3*, e1602640.
[23] Y. S. Rim, H. J. Chen, X. L. Kou, H.-S. Duan, H. P. Zhou, M. Cai, H. J. Kim, Y. Yang, *Adv. Mater.* **2014**, *26*, 4273.
[24] C. H. Ahn, K. Senthil, H. K. Cho, S. Y. Lee, *Sci. Rep.* **2013**, *3*, 2737.
[25] D. C. Dumka, H. Q. Tserng, M. Y. Kao, E. A. Beam, P. Saunier, *IEEE Electron Device Lett.* **2003**, *24*, 135.
[26] H.-A. Chin, I.-C. Cheng, C.-I. Huang, Y.-R. Wu, W.-S. Lu, W.-L. Lee, J. Z. Chen, K.-C. Chiu, T.-S. Lin, *J. Appl. Phys.* **2010**, *108*, 054503.
[27] J. Falson, Y. Kozuka, M. Uchida, J. H. Smet, T. H. Arima, A. Tsukazaki, M. Kawasaki, *Sci Rep* **2016**, *6*, 26598.
[28] H. Tampo, H. Shibata, K. Maejima, A. Yamada, K. Matsubara, P. Fons, S. Kashiwaya, S. Niki, Y. Chiba, T. Wakamatsu, H. Kanie, *Appl. Phys. Lett.* **2008**, *93*, 202104.
[29] D. W. Yue, S. B. Guo, S. Han, P. J. Cao, Y. X. Zeng, W. Y. Xu, M. Fang, W. J. Liu, D. L. Zhu, Y. M. Lu, Y. T. Qian, *J. Alloys Compd.* **2021**, *873*, 159840.
[30] B.-S. Wang, Y.-S. Li, I. C. Cheng, *IEEE Trans. Electron Devices* **2016**, *63*, 1545.
[31] W. Tian, T. Y. Zhai, C. Zhang, S.-L. Li, X. Wang, F. Liu, D. Q. Liu, X. K. Cai, K. Tsukagoshi, D. Golberg, Y. Bando, *Adv. Mater.* **2013**, *25*, 4625.
[32] Y. Chen, W. Huang, V. K. Sangwan, B. H. Wang, L. Zeng, G. Wang, Y. Huang, Z. Y. Lu, M. J. Bedzyk, M. C. Hersam, T. J. Marks, A. Facchetti, *Adv. Mater.* **2019**, *31*, 1805082.
[33] Y. F. Xia, G. He, W. H. Wang, Q. Gao, Y. M. Liu, *IEEE Trans. Electron Devices* **2021**, *68*, 2522.
[34] H. Wu, D. D. Lin, R. Zhang, W. Pan, *J. Am. Chem. Soc.* **2008**, *91*, 656.
[35] A. Liu, G. X. Liu, H. H. Zhu, F. Xu, E. Fortunato, R. Martins, F. K. Shan, *ACS Appl. Mater. Interfaces* **2014**, *6*, 17364.
[36] Y. Y. Cong, D. D. Han, X. L. Zhou, L. L. Huang, P. Shi, W. Yu, Y. Zhang, S. D. Zhang, X. Zhang, Y. Wang, *IEEE Electron Device Lett.* **2016**, *37*, 53.
[37] Y. Y. Cong, D. D. Han, J. C. Dong, S. D. Zhang, X. Zhang, Y. Wang, *Sci. Rep.* **2017**, *7*, 1497.
[38] K. M. Kim, W. H. Jeong, D. L. Kim, Y. S. Rim, Y. Choi, M.-K. Ryu, K.-B. Park, H. J. Kim, *IEEE Electron Device Lett.* **2011**, *32*, 1242.
[39] Y. H. Lin, H. Faber, J. G. Labram, E. Stratakis, L. Sygellou, E. Kymakis, N. A. Hastas, R. Li, K. Zhao, A. Amassian, N. D. Treat, M. McLachlan, T. D. Anthopoulos, *Adv. Sci.* **2015**, *2*, 1500058.
[40] S. R. Thomas, P. Pattanasattayavong, T. D. Anthopoulos, *Chem. Soc. Rev.* **2013**, *42*, 6910.
[41] L. Liu, S. J. Chen, X. C. Liang, Y. L. Pei, *Adv. Electron. Mater.* **2019**, *5*, 1900550.
[42] M. M. Billah, A. B. Siddik, J. B. Kim, D. K. Yim, S. Y. Choi, J. Liu, D. Severin, M. Hanika, M. Bender, J. Jang, *Adv. Electron. Mater.* **2021**, *7*, 2000896.
[43] F. C. He, Y. Qin, L. J. Wan, J. Su, Z. H. Lin, J. C. Zhang, J. J. Chang, J. S. Wu, Y. Hao, *Appl. Surf. Sci.* **2020**, *527*, 146774.
[44] Y. W. Li, C. Zhao, D. L. Zhu, P. J. Cao, S. Han, Y. M. Lu, M. Fang, W. J. Liu, W. Y. Xu, *Nanomaterials* **2020**, *10*, 976.
[45] M. G. Kim, M. G. Kanatzidis, A. Facchetti, T. J. Marks, *Nat. Mater.* **2011**, *10*, 382.
[46] J. W. Hennek, J. Smith, A. Yan, M. G. Kim, W. Zhao, V. P. Dravid, A. Facchetti, T. J. Marks, *J. Am. Chem. Soc.* **2013**, *135*, 10729.
[47] A. Liu, H. H. Zhu, S. Bai, Y. J. Reo, T. Y. Zou, M.-G. Kim, Y.-Y. Noh, *Nat. Electron.* **2022**, *5*, 78.
[48] L. N. Wang, G. He, S. S. Jiang, W. H. Wang, X. F. Xu, Y. M. Liu, Q. Gao, *IEEE Trans. Electron Devices* **2022**, *69*, 3169.
[49] Y. C. Zhang, G. He, L. N. Wang, W. H. Wang, X. F. Xu, W. J. Liu, *ACS Nano* **2022**, *16*, 4961.
[50] Y. Liu, H. Y. He, R. S. Chen, Y.-F. En, B. Li, Y.-Q. Chen, *IEEE J. Electron Devices Soc.* **2018**, *6*, 271.
[51] W. E. Muhea, T. Gneiting, B. Iñiguez, *J. Appl. Phys.* **2019**, *125*,144502.

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[52] M. X. Cai, R. H. Yao, *J. Appl. Phys.* **2017**, *122*, 154503.
[53] M. Ghittorelli, F. Torricelli, Z. M. Kovacs-Vajna, *IEEE Electron Device Lett.* **2015**, *36*, 1340.
[54] J. K. Jeong, *J. Mater. Res.* **2013**, *28*, 2071.
[55] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, J. K. Jeong, J.-Y. Kwon, B. Koo, S. Lee, *Appl. Phys. Lett.* **2009**, *95*, 232106.
[56] S. Yang, D.-H. Cho, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, J. Jang, J. K. Jeong, *Appl. Phys. Lett.* **2010**, *96*, 243505.
[57] S.-Y. Na, Y.-M. Kim, D.-J. Yoon, S.-M. Yoon, *J. Phys. D: Appl. Phys.* **2017**, *50*, 495109.
[58] X. M. Huang, C. F. Wu, H. Lu, F. F. Ren, Q. Xu, H. L. Ou, R. Zhang, Y. D. Zheng, *Appl. Phys. Lett.* **2012**, *100*, 243505.
[59] B. Ryu, H.-K. Noh, E.-A. Choi, K. J. Chang, *Appl. Phys. Lett.* **2010**, *97*, 022108.
[60] Y. C. Zhang, Y. J. Lin, G. He, B. H. Ge, W. J. Liu, *ACS Appl. Electron. Mater.* **2020**, *2*, 3728.
[61] Y. H. Liu, X. Wan, L. Q. Zhu, Y. Shi, Q. Wan, *IEEE Electron Device Lett.* **2014**, *35*, 1257.
[62] B. Yang, G. He, W. H. Wang, Y. C. Zhang, C. Zhang, Y. F. Xia, X. F. Xu, *J. Mater. Sci. Technol.* **2021**, *70*, 49.

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