S-Parameter Measurement and EM Simulation of Electronic Devices towards THz frequency range

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***Abstract*—In this paper, we present on-wafer S-parameter measurement of silicon-based devices up to 500 GHz and EM simulation analysis up to 750GHz. The EM simulation is carried out with RF probe models and without RF probe model (intrinsic EM simulation) up to 750 GHz. To understand difference between EM simulation predictions with and without RF probe model in frequency range 500 - 750 GHz, electric field distributions in the DUTs are analysed.**

***Index Terms*—Calibration kit Design; On-wafer S-parameter Measurement; TRL; Sub-THz; THz; EM Simulation; Electronic Devices.**

I. Introduction

Recent development in high frequency characterization equipment has enabled S-parameter measurement beyond 1 THz [1]. Over time, the high frequency performance of transistors fabricated on silicon substrate has also improved significantly [2], [3]. The process design kit (PDK) is one essential requirement for analog and RF circuit designs and it is usually prepared by foundries [4]. Accurate characterization and modeling of the electronic devices in upper sub-THz and THz frequency range is essential for circuit and system design in these very high frequency ranges [4]. It is reported that on-wafer measurements of electronic devices are more accurate compared to off-wafer measurement in upper sub-THz [5]. In order to perform on-wafer S-parameter measurement of a device under test (DUT), on-wafer calibration kit design is an essential requirement.

II. On-Wafer Calibration Kit Design

To perform the on-wafer TRL calibration, an on-wafer calibration kit is designed (see Fig. 1) and fabricated on the silicon substrate [6]. The kit consists of a long Line for measurement below 110 GHz and a short Line for beyond 110 GHz. In the kit, designed Thru standard length is 35 μm and designed open type Reflect standard is used in this study. A detailed description about the designed on-silicon on-wafer TRL calibration kit can be found in [6]. In this work, meander line and transistor-open shown in Fig. 2 are used as DUTs. The error-terms are calculated using the designed on-wafer TRL calibration kit standards. The position of the reference plane after applying the on-wafer TRL is shown in see Fig. 2 by green dashed line. The step-by-step procedure adopted to apply the on-wafer TRL calibration on DUTs is shown in Fig. 3. To know suitability of the designed on-wafer calibration kit in the on-wafer measurement beyond 500 GHz, a close EM simulator model of a RF probe reported in [7] is developed in HFSS (see Fig. 4).

III. Results and Discussions

The terminal capacitances of transistor-open and S-parameters of meander line are shown in Fig. 5 and Fig. 6, respectively. The terminal capacitances of transistor-open are calculated using S-parameters. In Fig. 5 and Fig. 6, orange color solid lines shows on-wafer measurements obtained using four sets of RF Picoprobe probes [8]. To assess accuracy of the on-wafer measurements 'intrinsic EM simulation' prediction is also included in both figures. The 'intrinsic EM simulation' predictions are obtained by considering only intrinsic part of the device during the EM simulation. In this work, intrinsic part of the device refers to part of the device located between the two reference planes (i.e. between green dashed lines in Fig. 2). The on-wafer measurements shown in orange color are roughly following the 'intrinsic EM simulation' results, but a frequency dependent difference between both results is visible. The observed frequency dependent differences between both are possibly due to the contribution of coupling from the probe heads (coupling from probe heads to wafer, as well as coupling between probe heads) which is not completely corrected by the on-wafer calibration [8], [9].

The EM simulations with RF probe models mimicking on-wafer measurements of DUTs are shown with solid blue lines in Fig. 5 and Fig. 6. In the EM simulation, four different RF Picoprobe probe models (not shown in this paper) are used up to 500 GHz [10] and the EM model shown in Fig. 4 is used for 500 - 750 GHz. The predictions obtained using EM simulations with RF picoprobe probe models are consistent with measurement up to 500 GHz. In 500 - 750 GHz, EM simulation with RF probe predictions are following the 'intrinsic EM simulation' trend but a frequency dependent variation between both the results can also be observed. To find a possible reason behind the variations, electric field distribution in transistor-open shown in Fig. 5b and Fig. 5c are studied. The electric field distribution shows undesired coupling of the DUTs with RF probes, and the substrate which may be a possible reason behind the observed variation. In Fig. 6, S_{21} obtained from the EM simulation with the RF

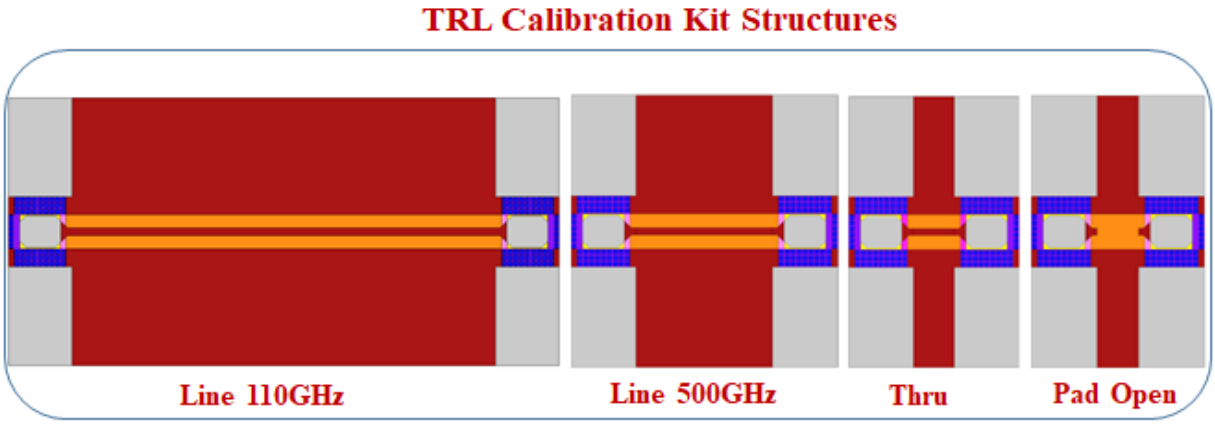

Fig. 1. Top view of on-wafer TRL calibration standards designed and fabricated on Si substrate. The thru and lines have conventional straight line design. In the on-wafer TRL calibration, Line 100GHz is used only up to 110 GHz and Pad Open is used as reflect.

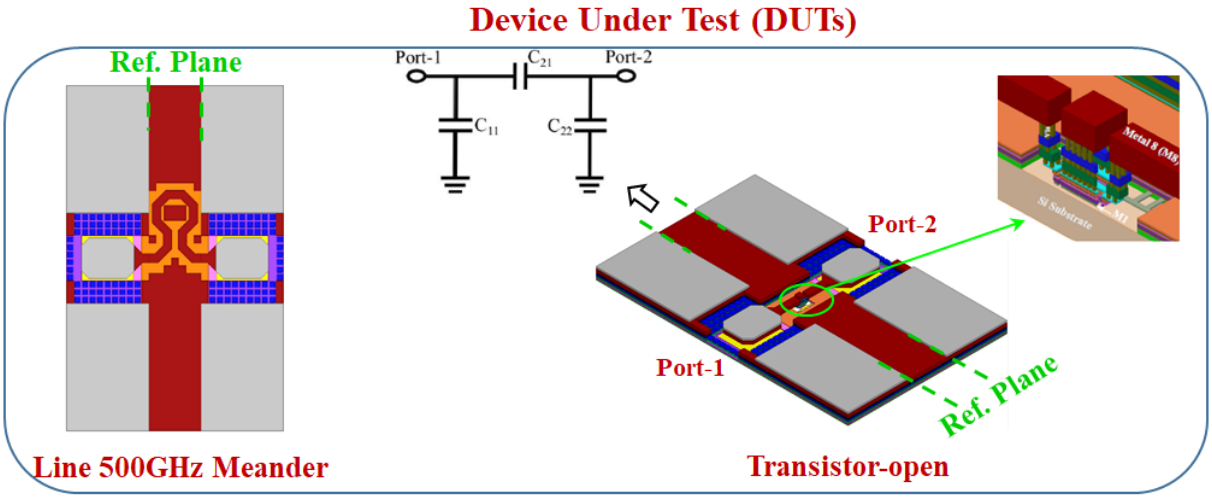

Fig. 2. Top view of DUTs 'Line 500 GHz meander' and 'Transistor-Open'. The 'Ref. Plane' shows the measurement reference planes location after applying the on wafer TRL calibration on the DUTs. For the transistor-open, terminal capacitances C_{11}, C_{21} and C_{22} are also shown.

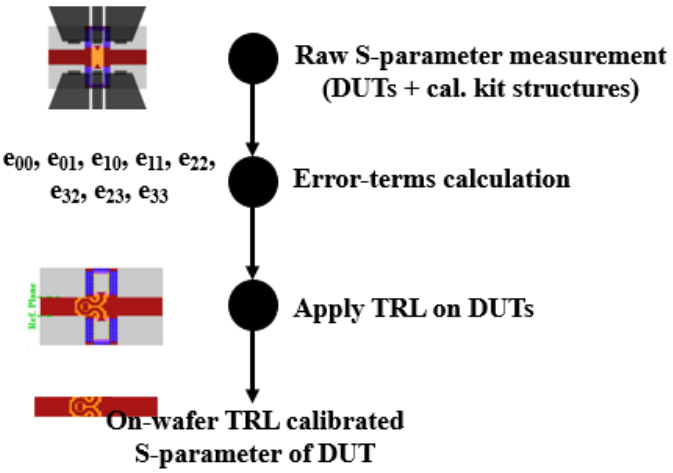

Fig. 3. Illustration of probing on RF pads (grey color) of pad open and location of the measurement reference plane after applying the on-wafer TRL calibration.

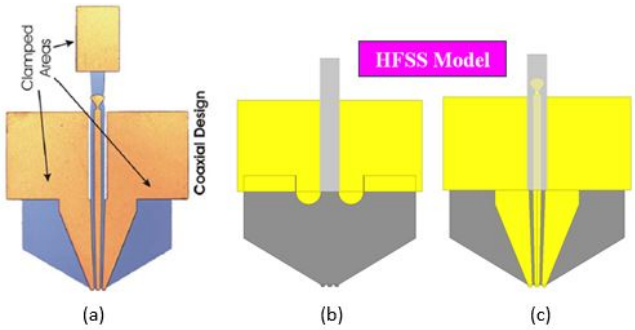

Fig. 4. (a) Top view of a RF probe reported in [7] and reproduced here ©[2011] IEEE. A RF probe model similar to RF probe shown in panel (a) is designed in EM simulator HFSS and its back and front view is shown in (b) and (c), respectively.

probe model is very close to measurements up to 500 GHz; comparing it to intrinsic EM simulation, a discrepancy above 625 GHz is notable between the intrinsic EM simulation and

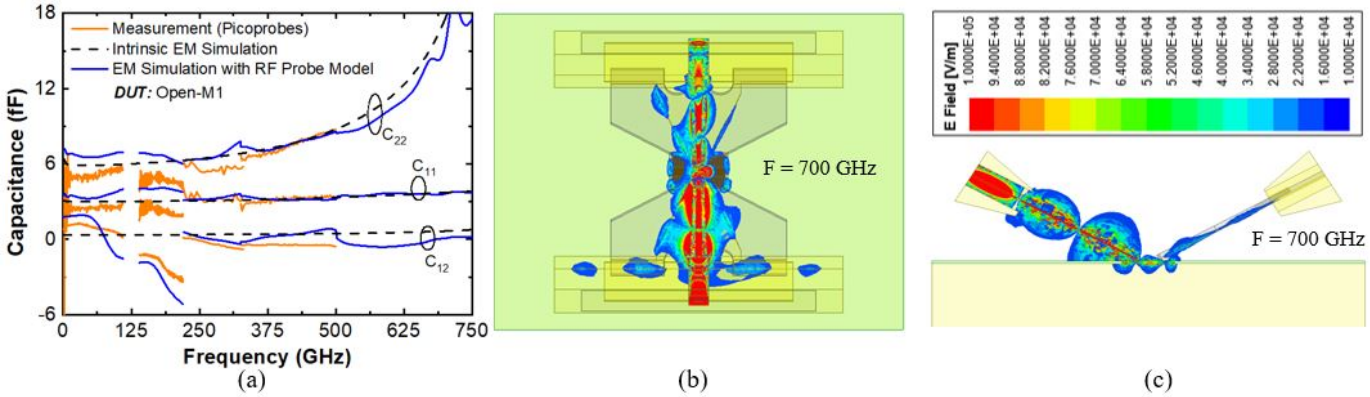

Fig. 5. (a) The capacitance behaviour obtained from on-wafer TRL calibrated S-parameters of transistor-open (open-M1). The electric field distribution in transistor-open at 700 GHz is shown in (b) and (c). The panel (b) shows top view while (c) shows the side view. Note that the electric field scale shown in (c) is used for all the electric field distribution presented in this work.

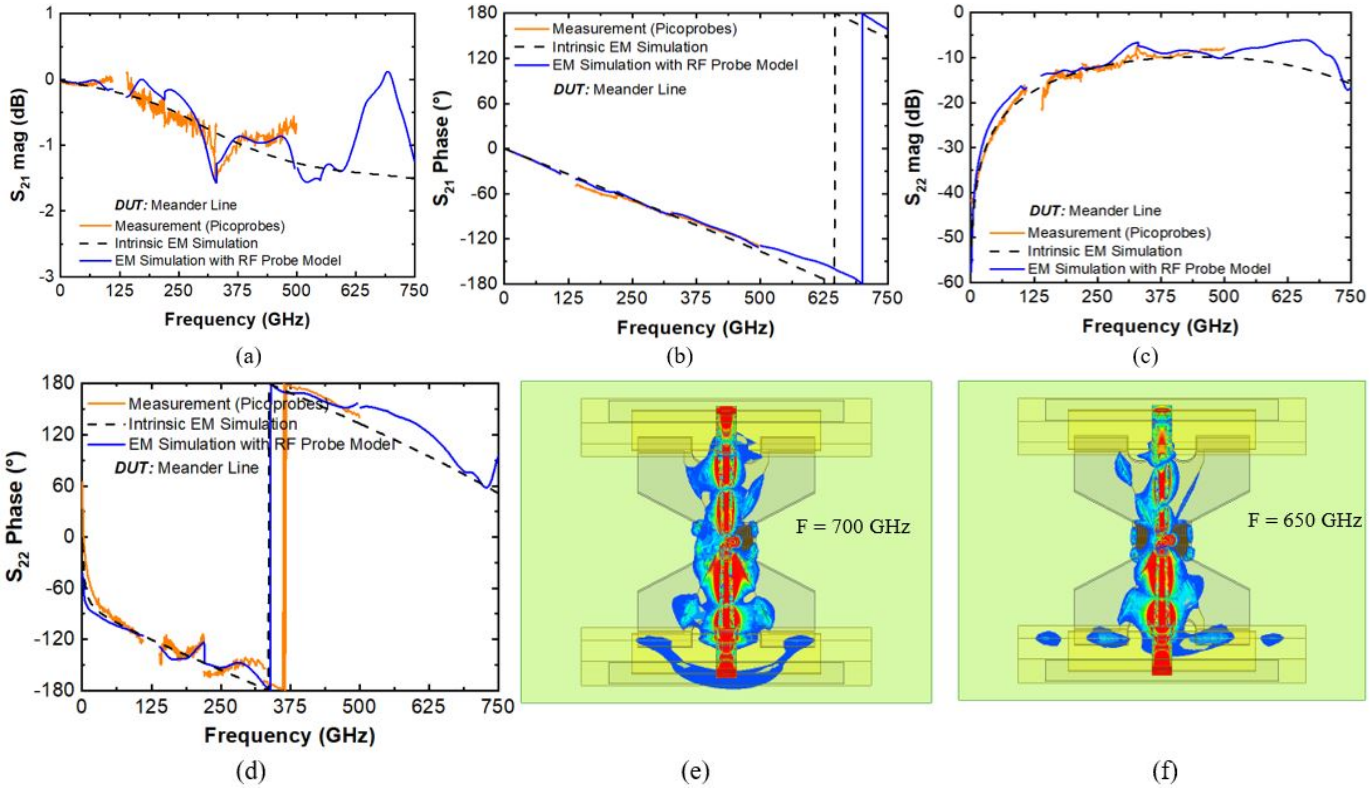

Fig. 6. The S-parameter behaviour of the 500 GHz meander line after applying the on-wafer TRL calibration and obtained from intrinsic EM simulation. The electric field distribution is shown in panel (e) and (f) at 700 GHz and 650 GHz, respectively.

the simulation with probe. Behind these frequency dependent differences, the undesired frequency dependent coupling of the DUT (see Fig. 6e and Fig. 6f) with substrate and RF probe can be a reason. The EM simulation based discussion in 500 - 750 GHz highlights challenges in accurate on-wafer S-parameters measurement of silicon based DUTs in THz frequency range.

IV. Conclusion

We presented on-wafer measurements of silicon based devices in the sub-THz and THz frequency range. The EM simulation study with and without RF probe models are presented up to 750GHz. The frequency dependent difference between intrinsic EM simulation i.e. without RF probe and on-wafer measurements shows requirement of efforts to improve on-wafer S-parameters measurement of DUTs in the sub-THz and THz frequency range. One factor behind these observed differences can be presence of different undesirable couplings.

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