Powerline Communication System-on-Chip in 180 nm Harsh Environment SOI Technology

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***Abstract*—Broadband powerline communication systems using Orthogonal Frequency Division Multiplexing (OFDM) can utilize existing power lines to transmit data packets alongside power distribution. Recent standards focus towards high speed multi-media in-house streaming. With improvements towards robustness and throughput new standards increase the speed and reliability of in-house powerline systems. A very different approach is the use of powerline communication systems in a deep drilling environment where temperatures of more than $150\,^{\circ}\mathrm{C}$ and pressure levels up to $30\,000\,\mathrm{psi}$ are present. Typical applications in this environment usually do not require more than several $\mathrm{kbit/s}$ per node and are more reliant on a stable and continuous connection. Here, a powerline communication system can reduce the amount of wiring needed and increase communication robustness significantly. This work provides a harsh environment suitable, reliable and standard compliant communication ASIC that is manufactured in XFAB $180\,\mathrm{nm}$ Silicon-On-Insulator (SOI) technology allowing operating temperatures of up to $175\,^{\circ}\mathrm{C}$. The die size is $5.25\,\mathrm{mm}$ x $5.25\,\mathrm{mm}$ and contains a complete Homeplug 1.0 communication stack with an environment for boot, interfacing and debugging. The data rate is as high as $6.1\,\mathrm{Mbit/s}$ using the fastest transmission mode and reaches the theoretical maximum of $0.55\,\mathrm{Mbit/s}$ in the robust OFDM (ROBO) mode which is of particular interest for harsh environment applications. To the best of the authors knowledge, this is the first OFDM-based powerline communication ASIC which is particularly designed for harsh environment.**

***Keywords*—Harsh Environment, Homeplug, Powerline, SoC, SOI, XFAB XT018**

I. Introduction

In a deep drilling environment high temperature, high pressure and mechanical shocks are present and impact the electronic components that are part of the drill string. Modern complex drilling systems comprise communication nodes as sensors, actors and controllers and are spread along the lower end of a drill string. In this system energy is provided locally by a generator and supplies all units via a continuous power line. The idea is to use that existing power line to enable communication for existing nodes. The challenge for a communication system is the environment which is a High Temperature High Pressure (HTHP) environment. Here, temperatures of more than $150\,^{\circ}\mathrm{C}$ and high pressure levels up to $30\,000\,\mathrm{psi}$ can occur [1], [6]. Moreover, the power supply and all consumers induce high frequency noise and create a highly distorted transmission channel for any type of communication. Therefore, a very robust system is required.

Starting around year 2000, the Homeplug Alliance began to standardize powerline communication for different in-house use cases. Their first standard was called HomePlug 1.0 (now TIA-1113) in 2001 [7]. Besides its regular communication modes, this standard contains an additional Robust OFDM (ROBO) mode particularly designed for harsh transmission channel conditions. This mode adds extra redundancy that can be used at the receiver to recover the information bits from highly distorted signals and makes it of particular interest for the HTHP environment in this work. The highest possible data rate for the ROBO mode is limited to $0.55\,\mathrm{Mbit/s}$ due to the extensive amount of redundancy. Our goal is a powerline communication ASIC which can withstand high temperatures of up to $175\,^{\circ}\mathrm{C}$ and is robust against highly distorted transmission channel conditions. The power consumption of a single powerline chip should be kept as low as possible since self-heating could further increase the die temperature beyond $175\,^{\circ}\mathrm{C}$. Additionally, the power budget in downhole applications is limited, especially when using multiple communication nodes at once.

The rest of this paper is structured as follows: In Section II the System-on-Chip (SoC) hardware design is described. In Section III the layout of the ASIC chip is presented and its partitioning is shown. Section IV shows the evaluation of the ASIC regarding power consumption and communication performance. The last Section VI concludes this work and gives a brief overview of the new possibilities which arise with the chip.

II. SoC Architecture

The HomePlug 1.0 standard defines the bottom two layers (Data Link Layer, DLL and Physical Layer, PHY) of the Open Systems Interconnection (OSI) model. Fig. 1 shows the basic structure of these layers and its connections. The MAC layer manages package distribution and provides an Automatic Repeat Request (ARQ) protocol, flow control and data encryption. Most of these tasks are state-machine based processes, which fit best onto a programmable processor. The implemented structure with two different processors is shown in the right part of Figure 1. In between the processors, two streaming blocks and a shared memory are attached. The upper MAC Layer Processor (MLP) is a 16-bit processor with 16 registers and multi-cycle architecture that is programmed using C-language. It provides memory-mapped I/O

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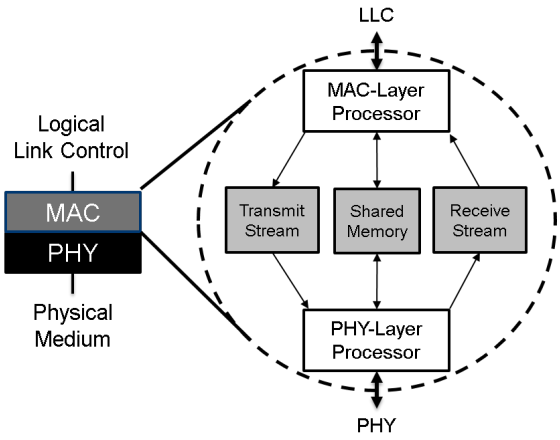

Fig. 1: Layer structure of the Homeplug 1.0 standard and zoom-in to MAC layer implementation consisting of two processors and communications blocks for transmit/receive.

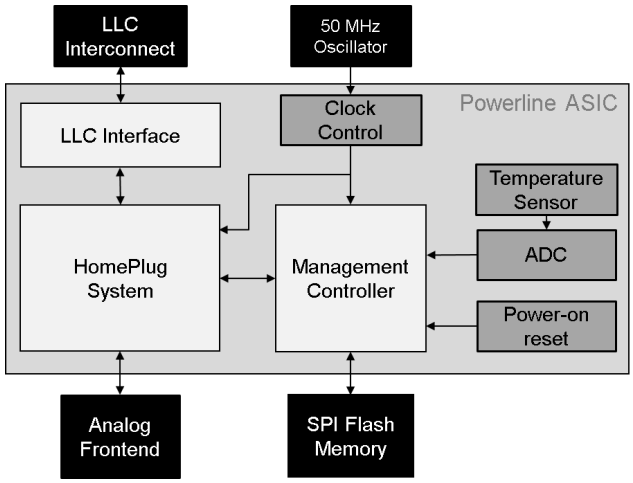

Fig. 2: Block diagram of the ASIC-SoC design, with analog components given in dark grey. Off-chip parts are shown outside of the SoC area in black.

over an interconnection bus that is directly addressable from the processor. Attached to this bus are $32\,\mathrm{kB}$ of instruction memory (IMEM), $4\,\mathrm{kB}$ of data memory (DMEM), the transmit and receive streams and a shared memory for inter-processor communication. The MLP manages all requests/replies from the upper Logical Link Control (LLC), prepares packages for encryption or decryption, creates flow control information and bridges destinations (e.g. Ethernet MAC to Powerline MAC addresses). The PHY Layer Processor (PLP) is a small 8-bit state-machine processor with no DMEM and a 1024 element IMEM, which is programmed using assembly language. The main task of the PLP is to control the data flow from and to the PHY layer and ensure precise timing for the channel protocol and access. The PLP only needs two cycles for each instruction execution making timing deterministic and ensures real-time execution. The connections between the two processors are data processing blocks named Transmit/Receive Stream in Figure 1. These streams contain encryption/decryption, packet formatting and Cyclic Redundancy Check (CRC) calculations, which are implemented as byte-streaming hardware blocks. Further information on implementation details are presented in [10]. The task of the PHY layer is to combine frame control bits and payload data bytes to form a continuous, analog signal to be transmitted on a shared power line bus. Its structure is a block-wise streaming architecture which contains e.g. a Reed-Solomon (RS) encoder and decoder, an (inverse) Fast Fourier Transform ([I]FFT) and a Viterbi decoder with a trace-back length of 60 [5], [7]. An encoded packet can hold from $152\,\mathrm{Bytes}$ up to $1600\,\mathrm{Bytes}$ of payload data depending on the channel conditions. The lesser the amount of bytes per packet the more redundancy is added for error correction. Especially the convolutional encoder block and ROBO mode induce redundancy, which generate up to 8 times more output data than they receive input data. To ensure the required throughput of $50\,\mathrm{MSamples/s}$ at the output of the PHY layer a full custom implementation in VHDL was designed. The challenge here was to maintain a continuous data flow at $50\,\mathrm{MHz}$ clock frequency while keeping pipelining and therefore the resulting die size and power consumption at a minimum.

III. ASIC LAYOUT

For ASIC implementation the XFAB $180\,\mathrm{nm}$ XT018 technology has been selected. It's a Silicon-on-Insulator (SOI) process with technology libraries that are qualified specifically designed for a wide temperature range from $-40\,^{\circ}\mathrm{C}$ up to $175\,^{\circ}\mathrm{C}$ [4]. Moreover, the relatively large node size of $180\,\mathrm{nm}$ and the use of a SOI technology results in a low leakage, which reduces the power consumption and resulting self-heating [11]. This technology is ideal for our targeted application.

Figure 2 shows the structure of the manufactured ASIC containing the HomePlug System (HPS) presented in Sec. II and its environment. The data flow is shown vertically (compare Fig. 1) with pin connections towards the LLC and an Analog Frontend (AFE). Between the HPS and the LLC Interconnect there is an LLC Interface which mainly consist of SRAM memory to store multiple packets ready for transmission or received by the HPS. Additionally, there is a 16-bit MIPS-like management controller (MMC), which handles the power-on sequencing and boot for the powerline modem. Moreover, a Power-On-Reset controller is attached to the MMC to release the global reset only if all supply voltages are stable. The MMC also has access to an off-chip flash memory, which is accessible via a Serial Peripheral Interface (SPI) holding the instruction code for both MAC layer processors as well as for the MMC itself. The ASIC contains a temperature sensor with associated analog-to-digital converter (ADC) that is accessible via the management processor. With this sensor it is possible to get and store the die temperature which can later be used to find correlations between temperature, environment changes and transmission characteristics. Lastly, a clock control distributes and derives the required 6.25/12.5/25/50 MHz from an external $50\,\mathrm{MHz}$ oscillator.

The ASIC layout of the above described system is shown in Figure 3. The memory and analog area of the layout are marked with white boxes. The largest are the IMEMs and DMEMs of the three processors and transmit and receive buffers for upper and lower layers. Additionally, there is a reserved area for future flash memory integration, which is

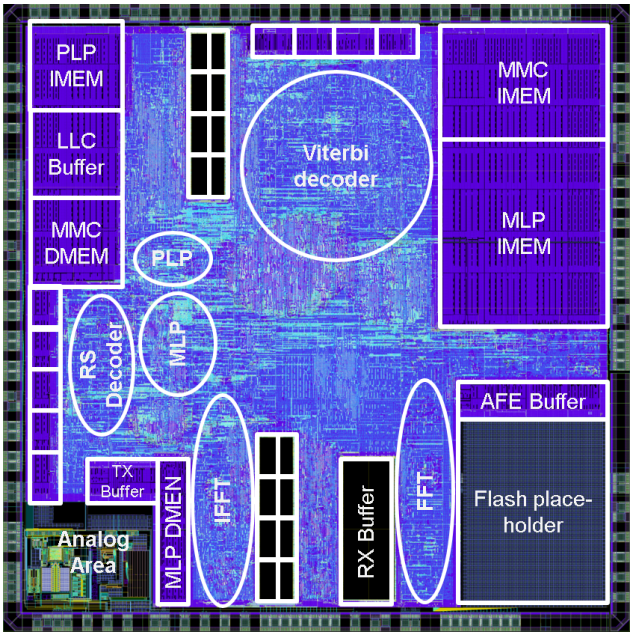

Fig. 3: Layout of the ASIC design post place and route. Analog area marked in the bottom left corner. White squares are memory instances and white circles are processing blocks which show their relative size and position.

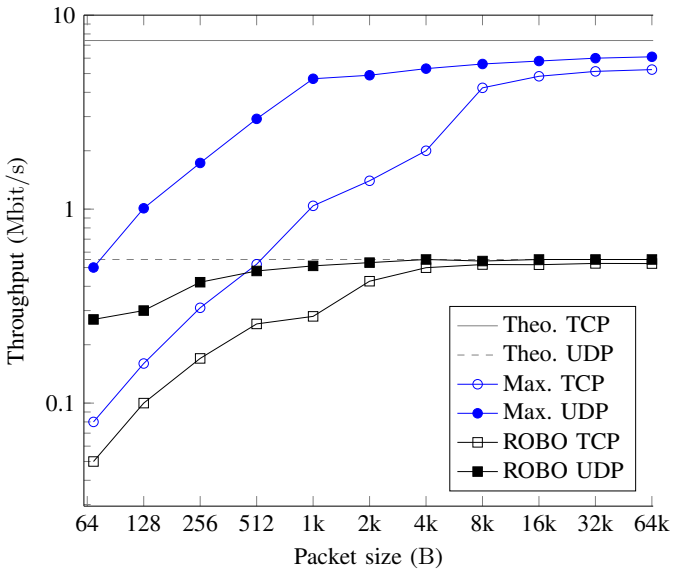

Fig. 4: TCP and UDP peer-to-peer throughput measurements over packet size for maximum utilization (Max. TCP/UDP) and ROBO mode. Both axes are shown in logarithmic scale.

off-chip in this revision. The white circles in the layout are the largest computation blocks with their position and size equivalently given as the position and size of the circle. The biggest among them is the Viterbi decoder with a relative size of 15 % of the layout. In total, the die consists of 47 % memory, 48 % logic gates and 5 % buffers and has 134 pins. The gate count is 1.52 Mgates and a die size of 27.25 mm^2 resulting in a gate density of 72.7 $\mathrm{kGE/mm}^2$ (neglecting the flash placeholder and I/O-pad area).

IV. Evaluation

The evaluation of the system is divided into two parts: Throughput measurement and power consumption estimation.

Throughput measurement

To estimate the throughput of our system we created an ASIC-equivalent FPGA design, which runs at the same clock frequency of 50 MHz as the ASIC design in our target application. This real-time emulation shows the identical performance of the powerline system as the ASIC design will do later on. The FPGA design runs on a National Instruments PXIe-7975R card, which contains a Kintex-7-K410T FPGA and has attached an Analog Frontend (AFE). The latter modulates the digital signal onto the power line medium or vice versa samples analog data and converts them in to digital samples. To measure the maximum peer-to-peer throughput we connected two of these systems via an analog coaxial cable and used a host PC which runs the measurement tool IPerf3 [3]. This tool provides User Datagram Protocol (UDP) based and Transport Control Protocol (TCP) based data streams using a client-server model. For the evaluation a 30 s transmission duration and block sizes from 64 Bytes up to 64 kB were used for both TCP and UDP transmissions. The theoretical maximum throughput, which can be calculated form the timings in the Homeplug 1.0 standard, is approximately 6.2 Mbit/s for TCP and 7.6 Mbit/s for UDP transmission in this two user peer-to-peer scenario [8].

Figure 4 shows the throughput of the system versus the packet size, which doubles for each test point. Here, “Max. TCP” and “Max. UDP” have the highest possible data byte encoding per packet and ROBO TCP/UDP is a transmission in the highly redundant ROBO mode. The theoretical maximum throughput is shown as horizontal lines labeled ”Theo. TCP/UDP”. When using ROBO mode with UDP protocol the theoretical maximum throughput of 0.55 Mbit/s is achieved above 256 B per packet. For ROBO mode with TCP protocol the throughput is lower due to the protocol overhead and saturates above 2 kB per packet at 0.52 Mbit/s. The overall highest throughput can be achieved with “Max. UDP” and is 6.1 Mbit/s. Both protocols scale linearly with the packet size up until 1 kB for UDP and 8 kB for TCP and saturate afterwards. The speed-up of UDP against TCP transmission for large packet sizes is about the expected protocol overhead for TCP transmission [2].

The overall performance of the system in a multi-user scenario meets the theoretical PHY layer throughput of 14 Mbit/s. However, system performance evaluation in a high load peer-to-peer scenario achieved a throughput of 80 % and 85 % from theoretical maximum for UDP and TCP, respectively. To find latency based bottlenecks, we simulated back-

TABLE I: Latencies of the individual layers for transmitting and receiving packets of maximum length.

	unit	MAC	PHY	Total
transmit	μs	350	0.04	350.04
	cycles	17500	2	17502
receive	μs	173	18.72	191.72
	cycles	8650	936	9586

TABLE II: Power estimation results for typical use cases of powerline communication in different technology corner cases.

	1.62 V					1.80 V	1.98 V	
	−40 °C	85 °C	125 °C	150 °C	175 °C	25 °C	−40 °C	0 °C
Boot (m W)	159	156	155	158	158	174	192	187
Idle (m W)	153	157	156	158	159	179	193	186
Max. Util. (m W)	208	211	211	214	215	237	263	258

to-back packet transmissions using the netlist of our die in Cadence INCISIVE 15.2 with the same transmission parameter as for the measurements shown in Figure 4. The analysis of transmit and receive latency for PHY and MAC is shown in Table I. The PHY layer is processing data packets fast enough to stay below the response interval of $26\,\mu$s with $18.72\,\mu$s latency in receive mode and a transmit latency of only $0.04\,\mu$s. However, the specified back-off waiting time of on average $232.96\,\mu$s (from $107.52\,\mu$s to $358.40\,\mu$s[5]) between two consecutive packets is being missed by the MAC layer by $117.04\,\mu$s. This is caused by the $350\,\mu$s latency on the MAC layer while transmitting. Additional transmit buffers need to be added in order to reach the maximum throughput in a peer-to-peer scenario. Since this scenario is unlikely in our multi-node, sparse packet transmission system, this improvement is out of scope of this work.

Power consumption estimation

To estimate the power consumption of our system and verify that no constraints are violated, a post place-and-route netlist simulation using Cadence INCISIVE 15.2 was performed. The netlist used for fabrication got back-annotated to the design library files and statistical switching activities for three use cases of the powerline communication were extracted: Boot (Power-up sequence including boot-loading and Power-on-reset), Idle (No transmission, scanning for new data) and "Max. Util." (Fully utilized powerline bus, system sending and receiving). Afterwards, the power consumption was estimated for various temperatures and supply voltages using Cadence GENUS 19.13. Five temperatures at 1.62 V, two at 1.98 V and the typical use case of 1.80 V for room temperature are available using the XFAB XT018 technology. Each case has an individual set of gate and memory libraries. Other cases than the ones listed in Tab. II (e.g. 175 °C and 1.8 V) are not provided and will be experimentally verified on the fabricated die. The results for a core voltage of 1.8 V (neglecting I/O-cells with 3.3 V) are shown in Table II. For the different use cases it can be seen that Boot and Idle have about the same average power consumption of 157 mW at 1.62 V and increase by 36 % in case of maximum utilization. Over temperature, the power consumption is only slightly changing with a maximum variation of 3 % whereas the power consumption increases by up to 26 % when increasing the supply voltage from 1.62 V to 1.98 V (as it is expected from literature [9]). For the targeted application, this means that the system has a nearly temperature invariant power consumption which allows us to define the required power generation system independent of temperature.

V. Fabricated Die

Figure 5 shows a photo of the bare die, where now the memory placeholders in the netlist are replaced with physical

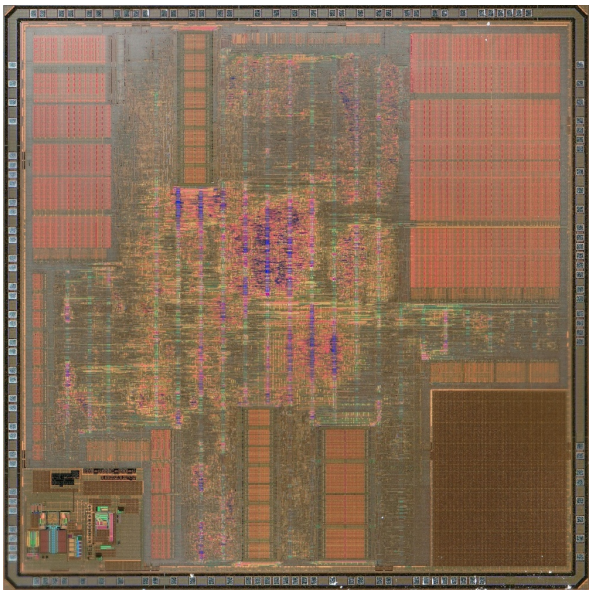

Fig. 5: Photo of the fabricated die.

structures. The rest of the die is partitioned as shown in the layout in Figure 3. Due to a Covid-19-pandemic caused fabrication delay, we are yet to verify our measured values from Section IV using the die instead of our FPGA design. For the throughput we expect no difference, since it is a purely digital replacement of the FPGA. For the power consumption we expect similar relations between the modes of operation as seen in the estimation, but with an offset due to the now placed memories and I/O-cells, which are driven by 3.3 V instead of 1.8 V.

VI. Conclusion

In this paper, we present a powerline communication ASIC which is designed with the XFAB XT018 SOI technology and is therefore able to work in a deep drilling high temperature high pressure environment. The size of the fabricated die is 5.25 mm x 5.25 mm and consists of 47 % memory blocks and 48 % logic gates. Evaluations have shown an average maximum power consumption of 212 mW for maximum utilization at 1.62 V that is mostly independent of temperature. Moreover, our system is able to provide a maximum data rate of up to 6.10 Mbit/s in the highest modulation scheme and 0.55 Mbit/s for the ROBO mode which is also its theoretical maximum throughput. Further evaluation regarding the delays in our system have shown latencies as low as only 2 cycles for the PHY layer which is able to provide the theoretical maximum bus throughput of 14 Mbit/s. To the best of our knowledge, we present the first OFDM-based powerline communication ASIC which is designed for harsh environment.

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