Received: 13 December 2021 | Revised: 7 April 2022 | Accepted: 17 April 2022

DOI: 10.1002/eng2.12520

RESEARCH ARTICLE

Engineering Reports Open Access WILEY

X-ray microscopy and automatic detection of defects in through silicon vias in three-dimensional integrated circuits

Benedikt Christopher Wolz[1] | **Christian Jaremenko**[1,2] | **Florian Vollnhals**[1] | **Lasse Kling**[1] | **Jan Wrege**[3] | **Silke Christiansen**[1,2]

[1]Institute for Nanotechnology and Correlative Microscopy gGmbH, Forchheim, Germany

[2]Fraunhofer IKTS, Forchheim, Germany

[3]Siemens Healthineers, Forchheim, Germany

Correspondence
Silke Christiansen, Fraunhofer IKTS, Äußere Nürnberger Straße 62, 91301 Forchheim, Germany.
Email: silke.christiansen@ikts.fraunhofer.de

Funding information
Bayerische Staatsministerium für Wirtschaft, Landesentwicklung und Energie; H2020 European Research Council, Grant/Award Number: 810316

Abstract

Through silicon vias (TSVs) are a key enabling technology for interconnection and realization of complex three-dimensional integrated circuit (3D-IC) components. In order to perform failure analysis without the need of destructive sample preparation, x-ray microscopy (XRM) is a rising method of analyzing the internal structure of samples. However, there is still a lack of evaluated scan recipes or best practices regarding XRM parameter settings for the study of TSVs in the current state of literature. There is also an increased interest in automated machine learning and deep learning approaches for qualitative and quantitative inspection processes in recent years. Especially deep learning based object detection is a well-known methodology for fast detection and classification capable of working with large volumetric XRM datasets. Therefore, a combined XRM and deep learning object detection workflow for automatic micrometer accurate defect location on liner-TSVs was developed throughout this work. Two measurement setups including detailed information about the used parameters for either full IC device scan or detailed TSV scan were introduced. Both are able to depict delamination defects and finer structures in TSVs with either a low or high resolution. The combination of a 0.4× objective with a beam voltage of 40 kV proved to be a good combination for achieving optimal imaging contrast for the full-device scan. However, detailed TSV scans have demonstrated that the use of a 20× objective along with a beam voltage of 140 kV significantly improves image quality. A database with 30,000 objects was created for automated data analysis, so that a well-established object recognition method for automated defect analysis could be integrated into the process analysis. This RetinaNet-based object detection method achieves a very strong average precision of 0.94. It supports the detection of erroneous TSVs in both top view and side view, so that defects can be detected at different depths. Consequently, the proposed workflow can be used for failure analysis, quality control or process optimization in R&D environments.

KEYWORDS

3D IC, deep learning, object detection, through silicon vias, x-ray microscopy

JEL CLASSIFICATION

Electrical and electronic engineering

[Correction added on 04 June 2022, after first online publication: figure 2 has been corrected in this version.]

1 | INTRODUCTION

1.1 | 3D-IC and through silicon via technology

The conventional two-dimensional integrated circuit (2D-IC) packaging design for microelectronic chips will soon reach its limit due to the demand of power, size and performance. One solution to this problem is the use of the three-dimensional integrated circuit (3D-IC) design, where wafer and dies are stacked and vertically interconnected in order to generate a single device with improved performance, reduced wiring length, and enhanced functional density.[1,2]

One common type of 3D-IC integration is the use of through silicon vias (TSVs), which was developed in the last two decades as a promising concept for the enabling of complex 3D-IC components.[1] A typical TSV consists of a metal embedded into a silicon wafer that is electrically isolated by a dielectric intermedium layer. This construction enables an electrical connection through the silicon wafer substrate. A common metal used in TSV interconnections is copper (Cu) due to its good electrical and mechanical properties in comparison to other materials like polysilicon or tungsten.[3-6] TSVs are versatile and can be used for either low or high-density applications. There exist three types of TSV technologies (via-first, via-middle, via-last) depending on the placement of the fabrication during front end of line (FEOL) and back end of line (BEOL) processing. Via-first TSVs are manufactured before FEOL and BEOL, via-middle TSVs after FEOL but before BEOL and via-last TSVs after FEOL and BEOL.[7]

For via-last TSVs and depending on the number and density of TSVs and the geometrical TSV dimensions on a silicon wafer two types of TSVs can be fabricated, the so-called fulfilled TSVs or Cu liner-TSVs. Fulfilled TSVs are created in a process involving etching of the Si wafer material in order to form well-defined blind holes, cleaning and isolation processes, deposition of barrier and seed layers, and a final electroplating process of the Cu material to fill out the holes.[8] Depending on the depth and diameter chosen for the application specific process, it is possible to create fulfilled TSVs of high aspect ratios using this workflow today. In order to minimize the electroplating process times and costs and to minimize thermomechanical expansion of Cu inside the TSVs the Cu liner-TSV technology can be used. Here, the TSVs are not completely filled by Cu but only wall-deposition is performed. This via-last Cu liner-TSV technology is used on applications where a low to increasingly high density of low aspect ratio TSVs is required.[9-12]

Throughout the fabrication process, thermal stress can be induced on the TSV structures during annealing procedures. Generally, this thermo-mechanical stress at the Si–Cu interface originates from the large difference in the coefficient of thermal expansion and will most likely lead to structural failure like via extrusion, Si cracking, wall delamination and degradation of Cu liner, and fulfilled TSV structures. Furthermore, during the electroplating process for Cu liner-TSV structures process variability such as Cu thickness variations or small gaps inside the Cu layer due to irregularities in the insulation, barrier, or seed layers can occur. Hence, the complete fabrication process needs to be controlled and optimized in order to reduce device failure and limit the yield loss.[2,13-15]

1.2 | Failure analysis methodologies of TSVs

It is therefore necessary to perform failure analysis during the development of a proper TSV fabrication process in order to determine and identify the origin of defects in the devices. Common analytical methods are optical- and electron microscopy inspection for the investigation of TSV defects or high-resolution X-ray diffraction (HR-XRD), focused ion beam based deformation analysis by correlation (fibDAC), and micro-Raman spectroscopy for the analysis of internal stresses at the TSV interfaces.[16] While these approaches yield highly specific and/or high resolution data, they require extensive sample preparation via embedding, mechanical grinding, and polishing of the samples to create physical cross sections of the devices. However, this may be undesired under specific circumstances as these processes are quite time consuming, leading to low turnaround or lack of statistical power. In addition, the required sample preparation makes these approaches destructive in nature. Furthermore, the sample preparation can cause unwanted stress and damages at the TSVs and disables further investigation methods that require untreated samples.[14]

3D x-ray microscopy (XRM) is a versatile imaging technique that enables internal analysis of certain structures by applying an x-ray beam onto the sample, using geometric and optical magnification by the use of a scintillator-coupled objective to magnify the projection and detecting the weakened transmitted photons. By rotating the sample and recording an image for each specific angle, a dataset of projections for 3D reconstruction can be collected.[17] In contrast to common x-ray microtomography, XRM enables high resolution imaging of large samples due to the improved spatial

resolution originating from the addition of optical objectives to the magnifying process.[18] This whole analysis process leads to a 3D inspection tool that enables non-destructive analysis of internal defects such as voids, delamination, or even cracks inside the device structures. Furthermore, using the 3D dataset one can either create virtual cross-sections by presenting only single slices of the reconstructed dataset or image a complete 3D reconstructed image with respective software.[17,19]

Therefore, XRM is used in R&D and in industrialization processes to inspect 3D ICs with TSVs on a regular basis to control and improve fabrication processes for metrological applications for process control, failure and defect localization in combination with other techniques or as a standalone investigation method.[19-21] One drawback of XRM, however, is the long measurement time that is required to image small micro- and nanometer sized cracks and voids inside the investigated samples. The measured voxel sizes are directly dependent on the investigated field of view, which depends mainly on the geometric and optical magnification of the system, resulting in a trade-off in resolution and the measured volume of the sample.[17,22] Here, other methods such as FIB-SEM or optical inspection after sample preparation perform better in terms of image quality and may compete in terms of overall analysis procedure time. In contrast, measuring a high number of TSVs in one single low-resolution scan is usually possible in a few hours scan time and generates much more statistical verification than sample preparation and single optical or electron microscopic identification or FIB-SEM, which usually requires several hours of work on a limited number of TSVs.[23,24] For a comparison of typical inspection techniques and the spatial resolution, probing depth, or sample preparation, see the work by Kong et al.[3]

In XRM, one can either image the sample in full field of view with a low resolution or zoom inside a certain structure and record a high resolution scan of a single structure of the sample. 3D-ICs will most likely possess a high number of TSVs on a single chip. It is therefore favorable to measure XRM with the sample in full field of view at first to check every single TSV on a chip for damages and then continue with high resolution scans of selected TSVs for the detection of smaller defects and other artifacts.

1.3 | Automated deep learning approaches for failure analysis

It is difficult to accomplish the simultaneous analysis and specific identification of a large number of TSVs to determine the characteristics or defects of certain TSVs of interest. Especially for recurring quality inspections or for the quantification of process changes, automated machine learning solutions in general and in particular deep learning approaches are well suited for this purpose. In recent years, such solutions have been established in many diverse domains and on different scales, such as face recognition,[25] tumor detection,[26] material characterization,[27] sheet metal forming surveillance,[28] defect detection for sewer pipes,[29] or for automotive parts.[30]

For object detection, the trend has gradually shifted from traditional machine learning methods toward modern end-to-end optimized deep learning models. This transition from hand-crafted, customized features to data-driven and automatically adapted or learned features emerged at the latest in 2014 with the ImageNet Large Scale Visual Recognition Challenge.[31] This competition uses the ImageNet database, which consists of 14 million manually annotated images with more than 20,000 classes and was developed for visual object recognition. While the best traditional machine learning algorithm achieved a top-5 classification error of 25%, this metric was improved to 3.67% by using deep learning.[32] In this context, the top-5 classification error is the portion of test images for which the actual ground truth label is not included among the classifier's top-5 predictions. One of the reasons for the success of deep learning approaches is the underlying end-to-end optimization, such that no classical approach has been able to outperform a deep learning-based method in object recognition challenges as for example PASCAL VOC[33] and MS COCO[34] since 2014. Fundamentally, the aim of object detection algorithms is to predict a bounding box around an object of interest, including the determination of its class membership, regardless of scale or partial occlusion. State-of-the-art results have been reported in the areas of pedestrian and face detection,[33,34] in autonomous driving by means of car detection,[35] or in the medical context within digital pathology by means of cell detection.[36] Approaches for object detection are generally categorized into single-stage and two-stage methods. Two-stage methods, such as Faster-R-CNN,[37] solve the task of detection and classification in separate steps. For this purpose, the location of the object is first determined by means of a region proposal network (RPN) and subsequently its class is determined by means of an additional network. While the two-stage variants have slight advantages regarding their precision, single-stage methods, such as YOLO,[38] SSD,[39] and RetinaNet,[40] which solve both the detection and classification in only one step, offer the better ratio of precision to inference speed.

The RetinaNet architecture is often used in microscopy image analysis[41-43] because it provides a decent trade-off between performance and complexity and proved to be applicable in class imbalance conditions.[42,44] Consequently, as

this study encounters large volumetric XRM data and class imbalance conditions, a RetinaNet is used for the detection and classification of TSVs.

1.4 | Current state of research for XRM and deep learning-based TSV analysis

Several publications that use XRM as an investigation method for TSVs were published in the last ten years. Gelb et al.[45] were one of the first groups to propose XRM as a non-destructive method to analyze interconnects using an Xradia nanoXCT. Since then several publications used lab-based 3D-XRM for analysis of, for example, fabricated TSV interposer technology,[46] thermal induced interconnects[3] or complete 3D-IC packages.[47] Pahwa et al.[20,48,49] focused in a series of recent publications on automated 3D metrology using XRM and deep-learning object detection workflows for void detection and segmentation of fulfilled TSVs and other buried structures.

Even though, there is still a lack of described workflows for the development of evaluated scan recipes and best practices regarding the parameter settings for the generation of optimal image data particularly for Cu liner-TSVs in the current state of literature. Especially in combination with deep learning, current approaches mainly focus on the detection of objects in the 3D volume[50] and do not focus on a micrometer accurate localization of defects within the individual TSV structures. Most of the presented studies were performed on high aspect ratio fulfilled TSVs rather than small aspect ratio Cu liner-TSVs, which are the focus of this study. None of the studies examined automatic defect detection of wall delamination defects of liner-TSVs. In addition, most object detection-based publications did not describe the workflow of finding the correct recipes and scan parameters for the XRM scans. This shows the necessity of developing an automatic workflow for micrometer-sized liner-TSVs of low aspect ratio in combination with an object detection pipeline for micrometer accurate localization of wall delamination defects.[20,46,49,50]

1.5 | Aim of this study

This study addresses the aforementioned shortcomings and provides not only two suggested XRM workflows for Cu liner-TSV analysis but demonstrates also an automated object recognition solution that can be already used for automatic failure analysis in production processes or quality control. XRM is chosen as a non-destructive technique that enables a fast defect analysis of a large number of TSVs, such as 70 or more, with defect identification down to the sub-micron scale. Furthermore, wall delamination defects that origin from the thermal mismatch of Si and Cu will lead to TSV degradation and is an important reliability failure as it reduces the electrical signal transfer in dies.[15,51,52] Therefore, the types of defects studied in this work are wall delamination defects of Cu liner-TSVs in the micrometer to sub-micrometer range. Overall, the XRM workflow is designed to suit that size range and being able to detect large delamination defects in micrometer range via a full device scan recipe and submicron defects with detailed TSV scan recipe. Such suitable scan recipes will be developed and presented in this work. No comparison of different deep learning architectures will be performed, as this work handles only a limited and imbalanced dataset, and will implement a well-suited RetinaNet architecture for the automated microscopic object recognition workflow. Overall, the method presented here is able to identify Cu liner-TSVs of interest using low resolution XRM scans and characterize them further using high resolution scans afterwards.

2 | RESULTS AND DISCUSSION

2.1 | Scan parameter finding process

In order to develop a suitable XRM workflow for Cu liner-TSV defect analysis on application specific integrated circuits (ASICs) it is necessary to find two XRM scan recipes. In contrast to defective TSVs, a non-damaged Cu liner-TSV possesses an intact wall and pad region without any bulge-like defects or small sub-micrometer-sized wall gaps as shown in XRM scans of intact standard ASICs (cf. Figure 1).

The ASICs used in this study possessed low aspect ratio via-last Cu liner TSVs fabricated and provided by Fraunhofer IZM-ASSID. The adapted fabrication process was optimized to yield a high density of low aspect ratio TSVs and does not count as a generalized process for all TSV architectures that commonly exist. The samples consists of processed Si wafers with 73 Cu-filled liner-TSVs of aspect ratio 3.0 with a top pad. The top side chip is occupied by a microball array.

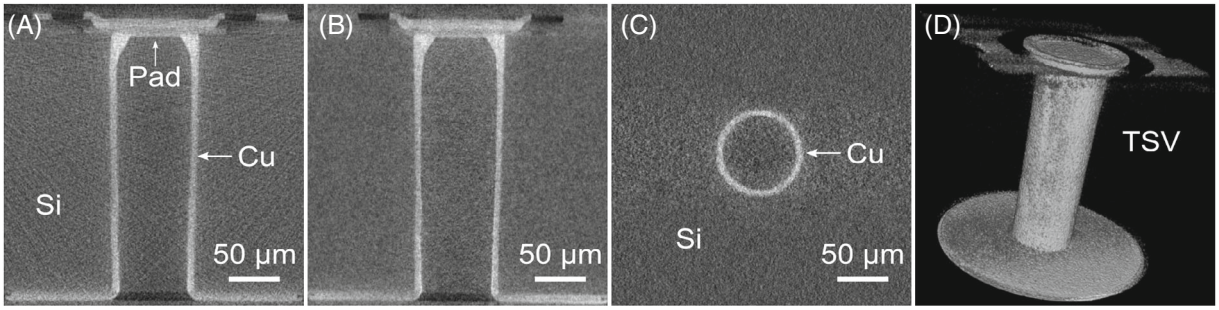

FIGURE 1 XRM scan of a single intact TSV on an ASIC in three different cross-sectional views and a single 3D-rendered view. (A, B) Orthogonal vertical cross-sections in XZ and YZ; (C) horizontal cross-section in XY at center height; (D) 3D render of the Cu liner and associated metallic components. Bright areas correspond to material of higher x-ray extinction, in this case the Cu liner and TSV top pad. Si and the oxide layer are quasi-transparent to x-rays and appear as noise. The TSV pad is shown on the top side of the structure. The scan was performed using 140 kV voltage, 21 W source power, high energy x-ray filter, 20× objective, 2401 projections, 184° rotation, 30 s exposure, a detector pixel binning value of 2 a voxel size of 0.95 µ.

These solder balls are made of a metal alloy of high Z materials, which leads to strong metal artifacts in most of the tomographic images. The workflow presented in this work will concentrate on such micrometer-sized low aspect ratio Cu liner-TSV structures and does not count as a general workflow for all TSVs.

All XRM measurements were performed on a Zeiss Xradia Versa 620 by placing an ASIC sample into the field of view of the Xradia system using a custom built sample holder. The XRM system is equipped with a 0.4× and 20× scintillator-coupled objective and combines geometric and optical magnification, enabling measurements from low to high magnification, field of views from 90 mm down to 0.5 mm and voxel sizes from 30 to 0.2 µm. The voxel size corresponds to the size of a single 3D pixel in the 3D dataset. The system consists of a 2048 × 2048 pixel noise suppressed charge-coupled detector and a high power sealed transmission source ranging from 30 to 160 kV with a maximum power of 2 W. The reconstruction was performed using the Zeiss Scout and Scan Reconstructor, which is based on filtered back projection (FBP) algorithms. This work focused on using the available reconstruction software from Zeiss and, therefore, does not consider changes in image quality via the use of other methods such as iterative or deep-learning based reconstruction. All datasets were manually reconstructed by applying the Zeiss standard beam hardening correction and center shift correction. A smoothing filter of 0.5 value was used. The dataset was globally scaled for reconstruction. Image editing and analysis was performed in Fiji.[53] All images shown in this work were brightness-contrast corrected on the minimum and maximum gray value. Quantitative analysis was performed without brightness-contrast correction.

First, a full device scan, where all TSVs are visible in one reconstructed dataset, needs to be found. The main objective of this recipe is to detect large micrometer-sized delamination defects that can occur during development of TSV wall fabrication processes. These scans should be aimed to be as short as possible in order to be suitable for a scan. Second, a detailed TSV scan recipe will be needed in order to depict detailed defects of micron or sub-micron size. These scans will be only performed after full device checkup. Finding the correct beam voltages and other scan parameters is a critical part of this recipe development. Therefore, the development of a full device scan was started using the 0.4× scintillator-coupled objective of the Zeiss Versa 620, which is suitable for scanning a complete ASIC chip. The source and detector were positioned as close as possible to the sample to fill out the field of view completely with the chip in all rotational positions. The overall magnification was set to approximately 1.8, which leads to raw projection images including the complete ASIC chip and also a small unattenuated reference around it. Before performing actual tomographic scans, focus was set on optimizing the single projection image quality by recording a single image at the short view, where the x-ray beam is directly perpendicular to the ASIC. For this, the voltage of the x-ray tube was varied from 40 to 140 kV and a reference-corrected single projection was recorded for a series of exposure values ranging from 0.05 up to 30 s. For each voltage a corresponding standard filter for the voltage regime was chosen according to the instrument manual. Furthermore, the exposure was increased for each voltage up to a value where detector saturation occurred. The raw projection images were analyzed by measuring the mean gray values of the complete ASIC (S_{ASIC}), the unattenuated reference region with noise that can be associated only to the measurement setup (S_{Noise}) and the standard deviation of the noise region σ_{Noise}. Fiji was used for this procedure.[53] Using these parameters, one can calculate the contrast-to-noise ratio (CNR) by using Equation (1).[54]

$$\mathrm{CNR} = \frac{S_{\mathrm{ASIC}} - S_{\mathrm{Noise}}}{\sigma_{\mathrm{Noise}}}. \quad (1)$$

Plotting the determined CNR values against each exposure of each voltage curve leads to the plot shown in Figure 2A. One can see that the highest CNR can be reached for the CNR-exposure curves of 40 and 60 kV beam voltage. The corresponding CNR and exposure values for 40 and 60 kV are (69, 25 s) and (60, 15 s), respectively. However, the 60 kV CNR-curve does not grow continuously and shows a kink around 10–14 s. This is a clear sign for source stability issues. Setting the focus on a single TSV on the center of the ASIC and taking the raw projection with the highest CNR value for each voltage and comparing them leads to the images shown in Figure 2B–G. Qualitatively, 40 and 60 kV show again generally the best gray value ranges with less noise and a clear distinction of the TSV wall and the surrounding area. This supports the finding from the quantitative measurements, where 40 kV and 60 kV possessed the highest CNR values for the complete ASIC chips. In order to keep the overall measurement time low, the exposure value should be set below 10 s. At around 8 s exposure the CNR value of the 60 kV curve is 50, which is slightly higher than the CNR value of 45 for the 40 kV of the same exposure time. However, because the 60 kV curve shows some clear source stability issues, it is inevitable to precede with a 40 kV beam voltage.

2.2 | Development of a full device scan recipe

Based on this recipe tomographic XRM scans were performed on a chosen ASIC using 40 kV beam voltage at a maximum power of 3 W and varying other parameters. Overall, four different tomographies, Figure 3A–D, were performed by varying the detector pixel binning values, projection numbers, exposure time or the use of the variable exposure time (VET) function. Binning is the process of combining a cluster of pixels on the detector to a single pixel in order to increase the overall intensity and thereby reducing the overall number of pixels. Therefore, pixel binning induces a loss in terms of image resolution, however, leading to a higher signal level and, thereby, reducing the scan time and improving the contrast. VET is a technical procedure used for samples that are thin and wide, such as typical ICs. At "long view" angles, where the wide side of the sample is parallel to the x-ray beam, typical artifacts can be introduced into the system because of the low x-ray transmission at these long view angles. In order to remove these, the use of VET enables the increase of the exposure time at these specific angles to solve this problem. Another technique commonly used for high aspect ratio samples is high angle resolved tomography (HART). HART is a technique that allows to acquire higher angular density projections for the long view angles using the same total number of projections. Altogether, all four tomographic XRM scans used 40 kV beam voltage, 3 W power, no x-ray filter, 226° rotation, the same overall magnification of 1.8, and the

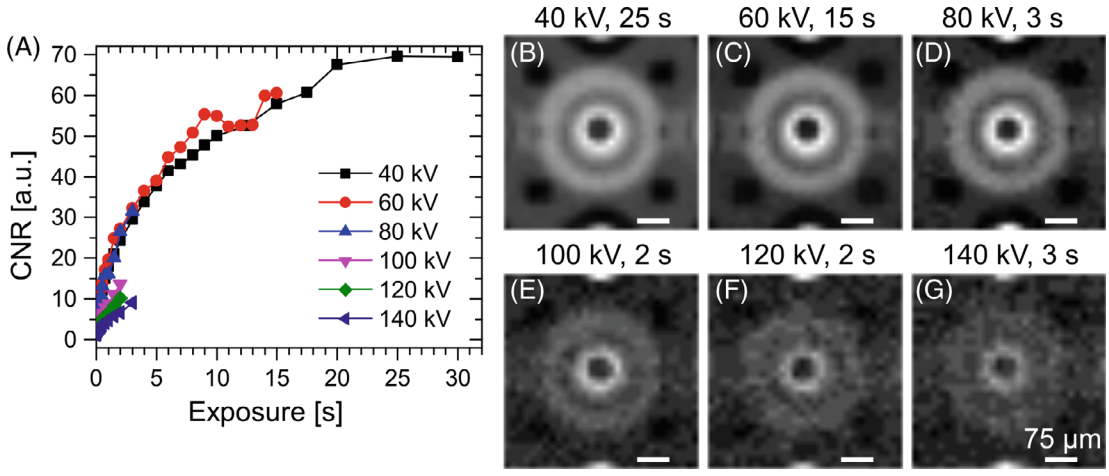

FIGURE 2 (A) Comparison of the CNR in dependence of the exposure time for voltages 40–140 kV. (B–G) Comparison of raw projection images of a single TSV on an ASIC taken with the 0.4× scintillator-coupled objective at a binning value of 2. The voltage was varied from 40 to 140 kV in 20 kV steps with maximum power of the x-ray tube possible for each voltage. The x-ray filters were varied according to the Zeiss standard procedure for each voltage. Exposure was set to 25, 15, 3, 2, 2, and 3 s for (B–G), leading to the highest CNR value for each voltage without overexposing the detector.

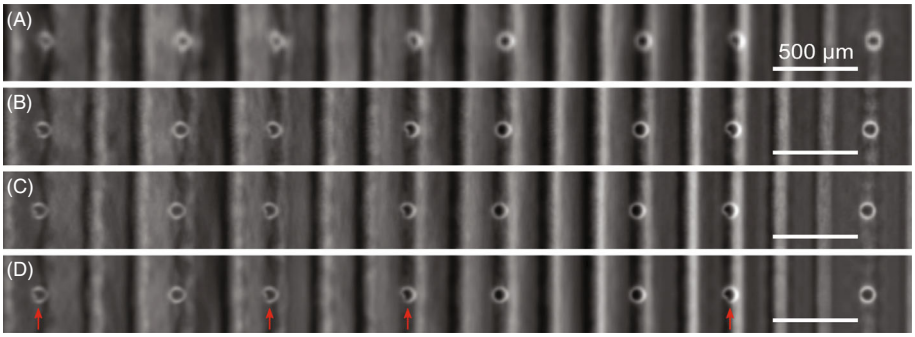

FIGURE 3 Reconstructed virtual cross sections of a TSV row on an ASIC from complete ASIC XRM tomographies with 0.4 × scintillator-coupled objective and varying binning numbers, projection numbers, exposure times and the use of variable exposure time (VET). All four scans were performed with 40 kV voltage, 3 W power, no x-ray filters, 226° rotation and high angle resolved tomography (HART). Differences in scan parameters are (A) binning of 2, 1601 projections, exposure of 1 s, and voxel size of 15.23 µm, (B) binning of 1, 901 projections, exposure of 8 s, and voxel size of 7.56 µm, (C) binning of 1, 1601 projections, exposure of 8 s, and voxel size of 7.56 µm, (D) binning of 1, 1601 projections, exposure of 8 s, voxel size of 7.56 µm, and multiplying the exposure time at long view angles by factor 5 using VET. Delamination defects are marked with red arrows.

HART function. The other scan parameters were varied as followed. For scan A, 1601 projections, a binning value of 2, and an exposure of 1 s was chosen in order to perform a very short scan of 1 h overall time with a high count-rate due to the increased binning value. However, the voxel size was also reduced by this to 15.23 µm. Scan B used a binning value of 1 to gain a smaller voxel size of 7.65 µm, an exposure value of 8 s to overcome the lack of counts and a decreased number of projections of 901 to shorten the measurement time to 3 h. For scan C, only the number of projections was increased up to 1601 projections compared to scan B, which leads to an overall measurement time of 5 h. At last, for scan D the same parameters of scan C were chosen but made use of the VET function with a factor of 5, which multiplies the exposure time for the long view angles by the given factor and leads to a total measurement duration of 14 h. All of these scans possessed strong line artifacts arising from the solder ball array on top of the ASIC. These strong artifacts are most likely to appear on solder ball alloys of high Z materials and are called metal-artifacts. They are well-known in micro-CT applications and are created during the reconstruction process.[55,56] The use of higher voltages and additional filters is a typical way of reducing metal artifacts. This was tested by performing other tomographies using parameters with higher voltages and filters. However, all of these scans showed the same strong metal artifacts and, therefore, are not shown in this work. Figure 3 shows digital cross sections of a single TSV row on the ASIC from these four tomographic datasets. All four images depict the approximate same virtual cross-section of a TSV row and possess strong vertical line artifacts, which arise due to the metal artifacts mentioned before.

In order to determine, which settings are optimal for a full device scan recipe, these four scans will be compared with each other. Detailed line profile analysis was performed and shown in Figure S1 the supplementary information available online. Scans A and B differ mostly in the voxel size value due to the higher binning value of scan A. By decreasing the voxel size from 15.23 to 7.56 µm and using a higher exposure time and less projections, the images get much more detailed and sharper while keeping the time below 5 h. Generally, there are two type of defects that can be distinguished from the top view virtual cross-section of the XRM data, delamination defects and layer interruptions due to processing issues. As delamination is an adhesive rupture between two layers, the defect occurs as a bulge-like or non-circular defect in the top view virtual cross-section. Layer interruptions, however, appears as an interrupted circle without any deviation from the circular form. As marked by the red arrows in the figure, there are delamination defects present in the reconstructed virtual cross sections. While these defects are clearly observed for scans B–D, the TSV walls for scan A are very blurry and the presence of delamination defects is not obvious. Scans B and C differ mostly by the increased number of projections of 1601 instead of 901. In general, one would make the assumption that the increased number of projections should lead to an increased fine structure and edge sharpness on the left side of the image (outer chip zone) while the right side (inner chip zone) is equally good. However, there is nearly no change in image quality present for these two scans. In addition, scans C and D differ only in the use of VET, which should in theory lead to slightly more detailed edges on the left side of the TSV row compared to the disuse of VET. However, there is nearly no change in image quality observed again. As also the line profiles shown in the supplementary information do not show any improvement in peak sharpness on the edges, this fact shows that there is no apparent improvement in image quality observed for either increasing the number of projections to 1601 for a full field of view scan or the use of VET to increase the exposure time on the long

view projections. Usually a high number of projections is recommend for tomographic studies of well-reconstructed high image quality, however fewer projections can often provide adequate results in a shorter time period. Therefore, there is always a trade-off in the choice of number of projections and measurement time. The increased number of projections might only lead to slightly or no improvement in this specific case, however, might lead to improvements for other ASIC scans. Therefore, regarding the time-quality factor the most efficient and most reliable results with a high number of projections this work will use scan C with a measurement time of 5 h, which is still within the bounds of a reasonable batch standard IC checkup. Therefore, the full chip scan recipe for this work will be chosen to match scan C, which is the use of 0.4× scintillator-coupled objective, 40 kV beam voltage, 3 W power, no x-ray filter, 226° rotation, use of HART function, binning of 1, 1601 projections, and an exposure time of 8 s.

2.3 | Development of a detailed TSV scan recipe

To image finer details inside the TSVs and detect small micrometer to sub-micrometer sized defects it is necessary to use a higher overall magnification and obtain a smaller voxel size. Therefore, the 20× scintillator-coupled objective will be used to get a detailed view on the TSVs and exclude solders balls in the field of view (FOV) in order to minimize metal artifacts created afterwards in the reconstruction. Due to the wide size of the chip and the low x-ray transmission for high magnification scans it is necessary to verify if there is an actual improvement in image quality for a pillar-like ASIC sample possessing only one line of TSVs compared to the full non-sliced device of high aspect ratio dimension. For this reason, an ASIC chip was sliced using a Leica TXP (diamond saw blade, 2500 RPM) to get a pillar like ASIC section for detailed XRM scans with a reduced long view. Furthermore, another non-sliced ASIC chip was taken for detailed XRM scans. Both chips possess defect TSVs from outdated production processes in contrast to the intact and optimized TSV shown in Figure 1.

Overall, four tomographic scans were performed on four different TSVs—two from the sliced chip and two from the non-sliced chip using either 40 or 140 kV shown in digital cross section images in Figure 4. The source and detector position was set to as close as possible to the sample. All scans were performed with the 20× scintillator-coupled objective, an overall magnification of 56×, a voxel size of 0.95 µm, 2401 projections, and 184° rotation. Due to the low count rate at the detector, a binning value of 4 and an exposure of 15 s were used to get a sufficiently strong signal. Scans A and C were performed with 40 kV beam voltage, 3 W power and used VET with a strength of factor 2 (multiplying the exposure at long view angles by factor 2) at the non-sliced and sliced chip, respectively. Scans B and D were performed using 140 kV beam voltage, 21 W power and with VET of factor 4 (multiplying the exposure at long view angles by factor 4) at the non-sliced and sliced chip, respectively.

Comparing the scans a) and b) for the non-sliced chip one can clearly see that the 140 kV scan B shows sharper structures at the TSV wall and at the TSV pad on the top of the image. In contrast, the 40 kV scan A image is blurry in the

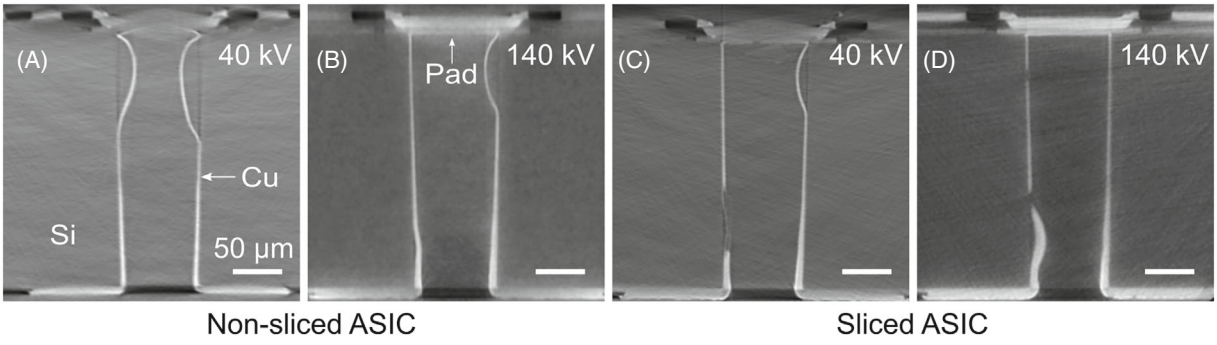

FIGURE 4 Reconstructed virtual cross sections of four single defect TSVs on ASICs from detailed TSV XRM tomographies with 20× scintillator-coupled objective. Scans (A) and (B) belong to non-sliced ASIC chips while scans (C) and (D) belong to sliced ASIC chips, which were used to increase the transmission on the long-view axis during rotation of the flat high-aspect ratio chip sample. All four scans used a binning of 4, exposure of 15 s, a voxel size of 0.95 µm, 2401 projections, and 184° rotation. The remaining scan parameters for (A) and (C) were 40 kV voltage, 3 W power, and using VET to multiply the exposure time at long view angles by factor 2, while (B) and (D) used 140 kV voltage, 21 W power, and using VET to multiply the exposure time at long view angles by factor 4.

TSV pad region. This effect most likely arises from high Z material parts in this pad region. For the sliced chip shown in scans C and D, the same trend at the TSV pad is observed. 140 kV shows a clearer fine structure at the pad there, however, it is also generally brighter than the 40 kV scan and exhibits a different gray value range. The contrast at the TSV wall, however, is now much better for the 40 kV scan as for the 140 kV scan. There are also some details and an increased edge sharpness in the pad region visible. However, the 140 kV still depicts most details at the TSV pad much clearer than 40 kV. Generally, the signal to noise ratio is improved for the low voltage scans but has a lack of general intensity. The reason for this is that the maximum power at this voltage is much lower compared to the high voltage scans. In contrast, high voltage scans improve the overall intensity but have a general lack of contrast and signal to noise due to the reduced number of low energy photons that are filtered away by the filters for high voltage regimes.

Overall, one can conclude that slicing the chip clearly improves the image quality for 40 kV beam voltage and leads to an overall better CNR at the TSV wall. However, the TSV pad region is still not properly imaged like for the 140 kV scan. In summary, a voltage of 40 kV works well for a sliced ASIC chip. However, if the destructive sample preparation is unwanted, the use of 140 kV voltage might be favored in order to get overall sufficient contrast and resolution.

2.4 | Summary of XRM recipes and suggested analysis workflow

Two recipes required for an XRM analysis workflow were successfully developed: (a) a full device scan recipe using a voltage of 40 kV and the 0.4× objective according to Figure 3C and (b) a detailed TSV scan recipe using a voltage of 140 kV and the 20× objective according to Figure 4D. Both workflows and general XRM setups are shown in Figure 5A,B. The next goal is to combine this together with object detection in order to develop an automatic analysis workflow. Altogether, the following workflow depicted in Figure 5C is proposed: a chip is scanned with the full device scan recipe shown in Figure 5A with the parameters described in Figure 3C. The reconstructed volumetric dataset is manually annotated for deep learning. As the Cu liner-TSVs appear non-circular (wall delamination defect) or circular (intact) in virtual cross sections from the top view, it is possible to label each TSV for each single slice with a defect or intact bound-box around the structure. This method will primarily focus on such delamination defects inside the TSV structures. After annotation, the neural network will be trained and optimized.

The trained network can be used for the evaluation of new datasets generated from further full device scans. In this step, defect and intact TSVs should be classified in terms of wall delamination defects or integrity. Based on these results, one can decide whether a further detailed TSV scan is required on any single TSV on the chip or if the chip can be used for further analysis, sample preparation for other investigation methods or complete device fabrication. Furthermore, this workflow is designed to assist the development of a fabrication process to either detect or exclude the presence of defect artifacts on a large number of TSVs on an ASIC chip.

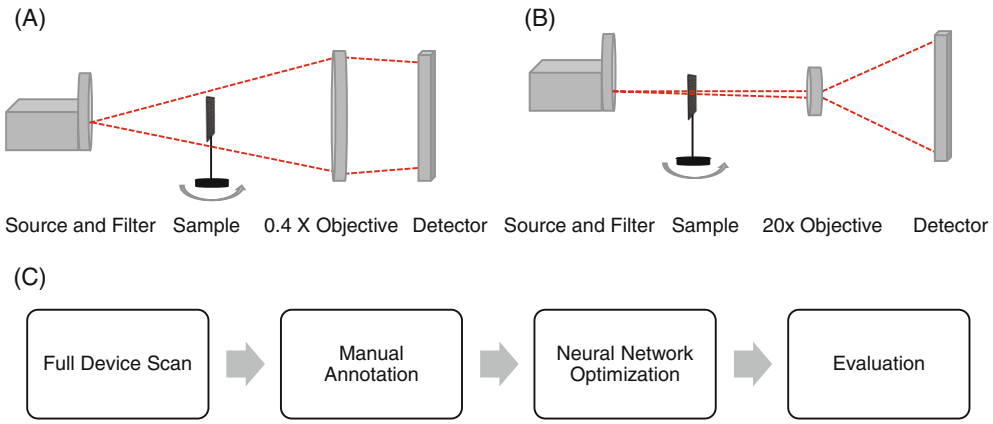

FIGURE 5 (A) General XRM setup for a full device scan workflow using the 0.4× scintillator-coupled objective. (B) General XRM setup for a detailed TSV scan workflow using the 20× scintillator-coupled objective. (C) Suggested workflow for object detection that uses a full device XRM scan, followed by manual annotation of the volumetric data and optimization of the neural network by training. In the end, the trained network can be used for the evaluation and automatic detection of further full device scans in order to decide whether a detailed TSV scan is necessary or not.

2.5 | Dataset for automated defect detection system

This part focuses on the development of an automated defect detection system that can be easily integrated into the measurement process. As previously described, the labels required for this are derived using manual annotation. Each ASIC contains multiple TSVs, and the respective state of each TSV is of interest. For the manual annotation, the TSV is individually analyzed slice by slice from top pad to bottom orifice of the TSV by an expert. The expert's task is to locate the positions of the TSVs and to classify the state of the TSVs at this depth and highlight them accordingly by means of a bounding box. Here, a distinction is made between defective TSVs due to delamination defects and intact TSVs. Examples of these two classes are provided in Figure 6, which illustrates single layer images of TSVs from a top-view perspective.

These vary in terms of the corresponding depth, the spatial positioning on the ASICs and originate from different batches. With the exception of the TSV pad at the top (cf. left side of Figure 6), intact TSVs are predominantly characterized by their perfect circular appearance from the top-view perspective. Delamination defects are typically associated with deviations from this circular shape. The light and dark vertical lines are metal artifacts that result, as mentioned in Section 2.1, from the composition of the ASICs within the reconstruction step and are not associated with the condition of the TSVs. The database was created using the open source software EXACT,[57] which provides a variety of annotation options via web interface, allows integration of developed deep learning models for inference and furthermore does not require the use of external data service providers. In total, 29,784 slices of 876 TSVs from 12 different ASICs were annotated for the object detection task, whereby a majority of intact TSVs were identified (cf. Table 1). Consequently, there is an overall class imbalance, which needs to be addressed by the algorithm.

2.6 | RetinaNet

Object recognition networks mimic expert behavior by detecting and classifying objects while assessing the reliability of their detection by means of scores. In this study, a RetinaNet[40] is used for this purpose, which provides a good trade-off between accuracy and speed. The RetinaNet architecture consists of a single network that uses a ResNet18[32] backbone as feature extractor (cf. Figure 7). Multi-scale features are then generated by means of a feature pyramid network (FPN),[58] as visualized in Figure 7. These are composed of low-resolution but semantically strong features, since more context is covered at the down-sampled layers, and high-resolution but semantically weak features at the layers that are closer to the original image size. Each layer of the FPN in this process is used for classification and regression via subnetworks in order to provide predictions on different scales. For this purpose, the classification subnetwork predicts the probability of the presence of a target object and its class membership for each anchor (small defined rectangles in the image domain of different shape and extent). The regression network is used to determine the coordinates for the bounding box containing the target object. In order to address the class imbalance, the FocalLoss[40] is employed in this study, that dynamically down-weights the contribution of easily and well classified samples and let the model focus on the difficult instances.

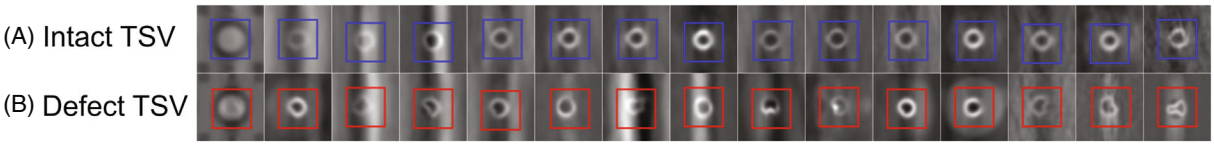

FIGURE 6 Ground truth annotations of (A) intact TSVs and (B) defect TSVs, taken from different production badges and different depths of the volumes. Note that bright vertical spots are location-dependent with respect to the position of each TSV on the ASIC, and its position with respect to the detector. In addition, varying levels of noise are emphasized by the images on the right-hand side. The position of the ground truth bounding boxes varies slightly, since it is difficult for a user to precisely determine the center of these small structures.

TABLE 1 Data distribution in terms of number of ASICs, analyzed TSVs, and defect and intact TSV slices

ASICs	TSVs	Defect TSV slices	Intact TSV slices	Image resolution	Bounding box size
12	876	8946	20,838	1440 × 1120 px	25 × 25 px

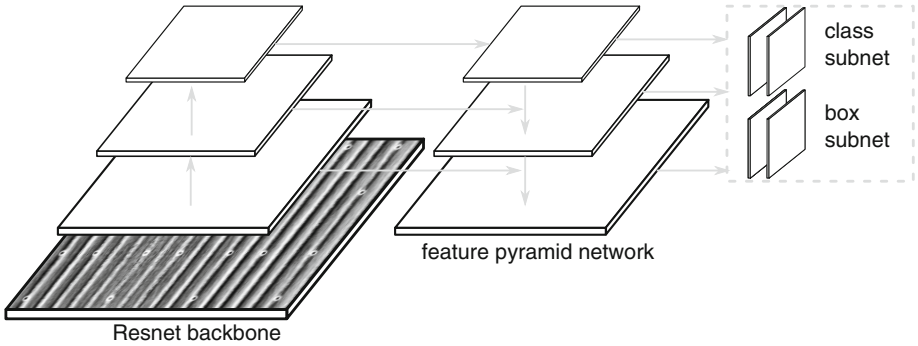

FIGURE 7 Object detection using RetinaNet. The ResNet18 architecture is employed as the backbone for the feature pyramid network that is used to generate multi-scale features. The classification subnetwork predicts the class membership, whereas the regression subnetwork estimates the coordinates for bounding boxes.

2.7 | Evaluation metrics

Independent of the selected network architecture and the different approaches of established object detection methods, several potential bounding boxes are predicted as detections, of which ultimately one is considered to be the final detection. The intersection over union (IoU), which describes the overlapping area of the predicted and ground truth bounding boxes, is used as the decisive metric for this. This metric is derived from the ratio between the area of the overlap and the area of union (cf. Equation 2), which is additionally illustrated in Figure 8. In this study, an IoU of 0.5 is used as threshold for a correct prediction of the bounding boxes, so that it is guaranteed that the region of interest is included in the prediction, if detected correctly. The performance of the algorithm is evaluated by precision and recall (cf. Equation 3).

$$\text{IoU} = \frac{\text{Area of intersection}}{\text{Area of union}} = \frac{B_{\hat{y}} \cap B_y}{B_{\hat{y}} \cup B_y}, \tag{2}$$

$$\text{Precision} = \frac{\text{TP}}{\text{TP} + \text{FP}}, \quad \text{Recall} = \frac{\text{TP}}{\text{TP} + \text{FN}}. \tag{3}$$

Here, recall indicates how many of the actual positive examples were detected during classification, whereas precision indicates which of the detected positive examples were actually positive. To calculate these metrics, a differentiation is made between true positives (TP), false positives (FP), and false negatives (FN) of the individual detections. These metrics work with binarized outputs, whereby real-valued output is usually provided by the algorithms. Consequently, a part of the information is discarded by means of threshold value procedures. Therefore, the precision and recall metrics depend on the choice of the threshold value. For this reason, the average precision (AP) metric, which uses all available threshold values and represents the area under a precision-recall curve, is used for detection methods. By averaging the AP over all available classes, the mean average precision (mAP) is obtained according to the PASCAL Visual Object Classes (VOC) challenge,[33] which is used as a single quantification metric to assess the overall performance of the classifier.

2.8 | Performance evaluation

In order to determine the performance of the object detection technique, a five-fold cross validation procedure is employed. For this purpose, the dataset is randomly divided into five equal parts, of which four parts are used for

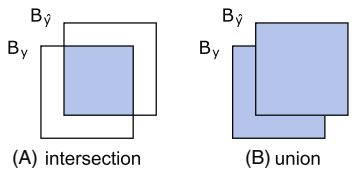

FIGURE 8 Example for (A) intersection and (B) union of bounding boxes

training and validating (60%, 20%) the network. The threshold for assessing the classification quality is determined using the validation dataset and then applied in the evaluation of the hold out test set. The actual performance is assessed using the unseen data which is consequently considered as a new dataset.

Training of the network is accomplished using the Adam optimizer[59] with a learning rate of 0.001. To avoid an overfit on the training data and to generalize to unseen data, the data are flipped randomly in horizontal and vertical directions during training. Additionally, intensity values are modified randomly, followed by the addition of randomized Gaussian noise. Prior to data processing, all slice images are individually normalized by robust scaling, using the 0.05 and 0.995 percentile.

2.9 | Object detection results

Overall, the object detection pipeline yields a very strong mAP of 0.94. Slightly different values are obtained for the different classes (cf. Table 2).

The class of intact TSVs is detected on average more effectively than the class of defective TSVs. Most of the errors occur in the lid region (cf. left-hand side of Figure 6), since even for an expert it is difficult to make consistent and unambiguous class assignments in this region. Further misclassifications occur in the transition range from still intact to slightly defective TSVs. This transition between the classes is difficult to distinguish from each other, especially due to the various very pronounced metal artifacts, so that perfect ground truth annotations cannot be assumed either. False positive detections tend to occur in the lid region as well, since many similar circular structures occur in this region. Due to plausibility, that is, objects must occur in spatial proximity in successive slices throughout the volume, these are not critical and can be easily considered in post-processing.

The annotation of the data was performed by the expert in the top-view, since defective TSVs can be easily identified here based on the deviation from an uniform circular shape. By reslicing, however, it is possible to illustrate the classification results of the individual TSVs from the side-view instead of the top-view (cf. Figure 9).

Consequently, this view emphasizes the depth at which the defects occur. This insight is of fundamental importance, since it enables correlation with the process parameters and thus might lead to the derivation of necessary process changes.

TABLE 2 Object detection results derived on the hold out test set using cross validation

mAP (±STD)	Avg. precision intact/defect (±STD)	Avg. recall intact/defect (STD)
0.94 ± 0.01	0.92 ± 0.01/0.83 ± 0.04	0.99 ± 0.00/0.93 ± 0.02

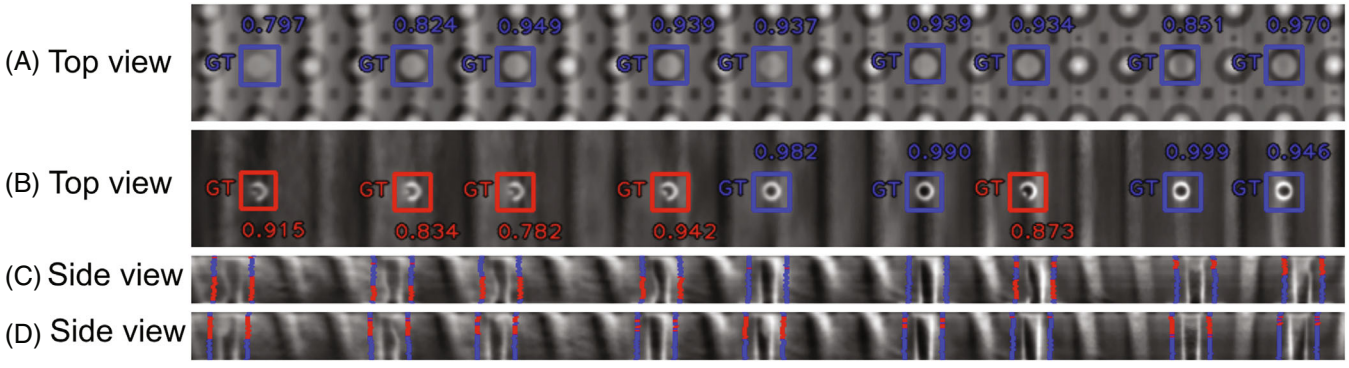

FIGURE 9 Predictions from different perspectives. (A, B) Highlight found objects at varying depths, with the corresponding confidence score beside the bounding box and the ground truth annotation class as encoded by the color. (C, D) Class information from a side-view perspective. This view provides insights on the depth at which defects occur, so that subsequently TSVs of particular interest can be examined in detail.

3 | CONCLUSION

This study provided a functional combined XRM and deep learning workflow for automatic wall delamination defect detection of a large number of Cu liner-TSVs in the micrometer to sub-micrometer range. The influence of several scan parameters on the raw and reconstructed dataset image quality was studied and discussed. Two practical XRM measurement recipes for short full device and long detailed TSV scans were proposed, using either 40 kV beam voltage and a 0.4× objective or either 140 kV and a 20× objective. Deep learning based object detection using datasets generated from several XRM scans from the proposed full device scan recipe indicated promising results in terms of precision and future application. This method focuses on data generated from the full device scans using the 0.4× objective and, hence, cannot be used together with the 20× detailed TSV scan recipe. Therefore, the detailed TSV scan recipe is designed to be used as an additional recipe after the workflow evaluation for more detailed but also longer analysis with sub-micron resolution. The proposed workflow provides promising results, so that an integration into industrial processes like quality control or process optimization during development seems feasible. Compared to other analytical methods such as the combination of sample preparation and optical or electron microscopy that require up to a full day of preparation work for a few TSVs on one cross section, this workflow enables relatively short measurement times of 3–5 h for direct non-destructive defect analysis with a high statistical output of 70 or more TSVs, as no time-consuming and statistically limiting sample preparation is needed for the XRM analysis. In addition, as this workflow is designed to be able to control a fabrication process, it is possible to either detect or exclude the presence of defect artifacts on a large number of TSVs on a ASIC chip depending on the current state of the process. By that, the workflow can successfully support or even improve the evolution of the complex fabrication process through the use of the presented machine learning workflow.

ACKNOWLEDGMENTS

The authors acknowledge Fraunhofer IZM-ASSID for providing the ASIC chips used in this study. S.C. acknowledges funding via the European Research Council (ERC) Synergy grant 4D-nanoSCOPE (grant no. 810316). Furthermore, B.C.W., F.V., L.K., and S.C. thank the Bavarian Ministry of Economic Affairs, Regional Development and Energy for financial support within the framework of the INAM research institute development. Open Access funding enabled and organized by Projekt DEAL.

CONFLICT OF INTEREST

The authors declare no financial or commercial conflict of interest.

DATA AVAILABILITY STATEMENT

Additional information is available in the supplementary material of this article.

ORCID

Benedikt Christopher Wolz https://orcid.org/0000-0001-7295-1997
Florian Vollnhals https://orcid.org/0000-0001-5743-019X
Lasse Kling https://orcid.org/0000-0003-1246-8228
Silke Christiansen https://orcid.org/0000-0002-4908-4087

REFERENCES

1. Hummler K, Smith L, Caramto R, et al. On the technology and ecosystem of 3D/TSV manufacturing. Proceedings of the SEMI Advanced Semiconductor Manufacturing Conference; 2011:1-6; IEEE, Saratoga Springs, New York, NY.
2. Jing X, Yu D, Wan L. Non-destructive testing of through silicon vias by high-resolution X-ray/CT techniques. Proceedings of the 14th Electronics Packaging Technology Conference (EPTC); 2012:533-536; IEEE.
3. Kong L, Lloyd J, Liehr M, Rudack A, Arkalgud S, Diebold A. *Metrology, Inspection, and Process Control for Microlithography XXVI*. Vol 8324. International Society for Optics and Photonics; 2012:832412.
4. Li Y, Goyal D. *3D Microelectronic Packaging: From Fundamentals to Applications*. Springer; 2017.
5. Sonawane D, Kumar P. New insights into fracture of Si in Cu-filled through silicon via during and after thermal annealing. *Eng Fract Mech*. 2020;238:107281.
6. Athikulwongse K, Yang J-S, Pan DZ, Lim SK. Impact of mechanical stress on the full chip timing for through-silicon-via-based 3-D ICs. *IEEE Trans Comput Aided Des Integr Circuits Syst*. 2013;32(6):905.

7. Gambino JP, Adderly SA, Knickerbocker JU. An overview of through-silicon-via technology and manufacturing challenges. *Microelectron Eng*. 2015;135:73.
8. Garrou P, Bower C, Ramm P. *Handbook of 3D Integration, Volume 1: Technology and Applications of 3D Integrated Circuits*. John Wiley & Sons; 2011.
9. Wolf MJ, Dretschkow T, Wunderle B, et al. High aspect ratio TSV copper filling with different seed layers. Proceedings of the 2008 58th Electronic Components and Technology Conference; 2008:563-570; IEEE.
10. Malta D, Vick E, Goodwin S. Fabrication of TSV-based silicon interposers. Proceedings of the International 3D Systems Integration Conference (3DIC); 2010:1-6; IEEE, Munich, Germany.
11. Kraft J, Schrank F, Teva J, et al. 3D sensor application with open through silicon via technology. Proceedings of the 61st Electronic Components and Technology Conference (ECTC); 2011:560-566; IEEE, Lake Buena Vista, FL.
12. Cassidy C, Kraft J, Carniello S, et al. Through silicon via reliability. *IEEE Trans Device Mater Reliab*. 2012;12(2):285.
13. Liljeholm J, Ågren P, Svedin N, Baghchehsaraei Z, Ebefors T. 3D MEMS wafer level packaging exemplified by RF characterized TSVs \& TGVs and integration of bonding processes. Proceedings of the 11th International Wafer-Level Packaging Conference (IWLPC); 2014:11-13; San Jose, CA.
14. Jiang T, Im J, Huang R, Ho PS. Through-silicon via stress characteristics and reliability impact on 3D integrated circuits. *MRS Bull*. 2015;40(3):248.
15. Ryu S-K, Lu K-H, Im J, Huang R, Ho PS. Stress-Induced Delamination Of Through Silicon Via Structures. *AIP Conf Proc*. 2011;1378:153-167.
16. Zschenderlein U, Vogel D, Auerswald E, Hölck O, Rajendran H, Ramm P, Pufall R, Wunderle B. Residual stress investigations at TSVs in 3D micro structures by HR-XRD, Raman spectroscopy and fibDAC. Proceedings of the 2014 IEEE 64th Electronic Components and Technology Conference (ECTC); May 27, 2014:1134-1142; IEEE.
17. Merkle AP, Gelb J. The ascent of 3D X-ray microscopy in the laboratory. *Micros Today*. 2013;21(2):10.
18. Wang T, De Wolf I, Gu A, Estrada R, Kelly S. Application of 3D X-ray microscopy for 3D IC process development. Proceedings Under International Wafer Level Packaging Conference.(IWLPC); 2016:1-6; San Jose, CA.
19. de Veen P, Bos C, Hoogstede D, Revenberg CTA, Liljeholm J, Ebefors T. X-ray inspection of TSV defects with self-organizing map network and Otsu algorithm. *Microelectron Reliab*. 2015;55(9-10):1644.
20. Pahwa RS, Nwe MTL, Chang R, et al. Deep learning analysis of 3D X-ray images for automated object detection and attribute measurement of buried package features. Proceedings of the IEEE 71st Electronic Components and Technology Conference (ECTC); 2021:2196-2204; IEEE.
21. Orozco A, Talanova E, Jeffers A, et al. Non-destructive 3D failure analysis work flow for electrical failure analysis in complex 2.5 D-based devices combining 3D magnetic field imaging and 3D X-ray microscopy. ISTFA 2018: Proceedings from the 44th International Symposium for Testing and Failure Analysis. ASM International; 2018:32.
22. White R, Kelly S. Correlative, multi-scale, lab-based X-ray tomography: from millimeters to nanometers. *Microsc Microanal*. 2020;26(S2):1002.
23. Meyer A, Grimm G, Hecker M, Weisheit M, Langer E. Non-destructive 3D failure analysis work flow for electrical failure analysis in complex 2.5 D-based devices combining 3D magnetic field imaging and 3D X-ray microscopy. 39th International Symposium for Testing and Failure Analysis (ISTFA); November 3–7, 2013:12-16; San Jose, CA.
24. Vartanian VH, Allen RA, Smith L, Hummler K, Olson S, Sapp BC. Metrology needs for through-silicon via fabrication. *J Micro/Nanolithogr MEMS MOEMS*. 2014;13(1):011206.
25. Parkhi OM, Vedaldi A, Zisserman A. Deep face recognition. Proceedings of the British Machine Vision Conference (BMVC); 2015:41.1-41.12; BMVA Press, Swansea, UK.
26. Aubreville M, Knipfer C, Oetter N, et al. Deep learning algorithms out-perform veterinary pathologists in detecting the mitotically most active tumor region. *Sci Rep*. 2017;7(1):1.
27. Jaremenko C, Ravikumar N, Affronti E, Merklein M, Maier A. Determination of forming limits in sheet metal forming using deep learning. *Materials*. 2019;12:7.
28. Jaremenko C, Affronti E, Merklein M, Maier A. Temporal and spatial detection of the onset of local necking and assessment of its growth behavior. *Materials*. 2020;13:11.
29. Yin X, Chen Y, Bouferguene A, Zaman H, Al-Hussein M, Kurach L. A deep learning-based framework for an automated defect detection system for sewer pipes. *Autom Constr*. 2020;109:102967.
30. Du W, Shen H, Fu J, Zhang G, He Q. Approaches for improvement of the X-ray image defect detection of automobile casting aluminum parts based on deep learning. *NDT E Int*. 2019;107:102144.
31. Russakovsky O, Deng J, Su H, et al. Imagenet large scale visual recognition challenge. *Int J Comput Vis*. 2015;115(3):211.
32. He K, Zhang X, Ren S, Sun J. Deep residual learning for image recognition. Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition; 2016:770-778; Las Vegas, NV.
33. Everingham M, Van Gool L, Williams CK, Winn J, Zisserman A. The pascal visual object classes (voc) challenge. *Int J Comput Vis*. 2010;88(2):303.
34. Lin T-Y, Maire M, Belongie S, et al. *In European conference on computer vision*. Springer; 2014:740-755.
35. Mundhenk TN, Konjevod G, Sakla WA, Boakye K. *In European Conference on Computer Vision*. Springer; 2016:785-800.
36. Marzahl C, Aubreville M, Bertram CA, et al. Deep learning-based quantification of pulmonary hemosiderophages in cytology slides. *Sci Rep*. 2020;10(1):1.

37. Ren S, He K, Girshick R, Sun J. (Preprint) arXiv:1506.01497; 2015.
38. Redmon J, Divvala S, Girshick R, Farhadi A. You only look once: unified, real-time object detection. Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition; 2016:779-788; Las Vegas, NV.
39. Liu W, Anguelov D, Erhan D, et al. European Conference on Computer Vision; 2016:21-37; Springer, Amsterdam, Netherlands.
40. Lin TY, Goyal P, Girshick R, He K, Dollár P. Focal loss for dense object detection. Proceedings of the IEEE International Conference on Computer Vision; 2017:2980-2988; IEEE, Venice, Italy.
41. Marzahl C, Bertram CA, Wilm F, et al. Learning to be EXACT, cell detection for asthma on partially annotated whole slide images; 2021. arXiv preprint arXiv:2101.04943.
42. Aubreville M, Bertram CA, Donovan TA, Marzahl C, Maier A, Klopfleisch R. A completely annotated whole slide image dataset of canine breast cancer to aid human breast cancer research. *Sci Data*. 2020;7(1):1.
43. Aubreville M, Bertram CA, Marzahl C, et al. Deep learning algorithms out-perform veterinary pathologists in detecting the mitotically most active tumor region. *Sci Rep*. 2020;10(1):1.
44. Nguyen N-D, Do T, Ngo TD, Le D-D. An evaluation of deep learning methods for small object detection. *J Electr Comput Eng*. 2020;2020:3189691.
45. Gelb J, Yun W, Feser M, Tkachuk A. X-ray microscopy for interconnect characterization. *AIP Conf Proc*. 2009;1173:145-148.
46. Zhang X, Chai T, Lau JH, et al. Development of through silicon via (TSV) interposer technology for large die (21×21mm) fine-pitch Cu/low-k FCBGA package. Proceedings of the 59th Electronic Components and Technology Conference; 2009:305-312; IEEE, San Diego, CA.
47. Sylvester Y, Hunter L, Johnson B, Estrada R. International 3D Systems Integration Conference (3DIC); 2013:1-7; IEEE, San Francisco, CA.
48. Pahwa RS, Ho SW, Qin R, et al. Machine-learning based methodologies for 3D X-Ray measurement, characterization and optimization for buried structures in advanced IC packages. Proceedings of the 2020 International Wafer Level Packaging Conference (IWLPC); 2020; IEEE.
49. Pahwa RS, Gopalakrishnan S, Su H, et al. Automated void detection in TSVs from 2D X-ray scans using supervised learning with 3D X-ray scans. Proceedings of the 2021 IEEE 71st Electronic Components and Technology Conference (ECTC); 2021:842-849; IEEE.
50. Pahwa R, Nwe TL, Chang R, et al. Deep learning analysis of 3D X-ray images for automated object detection and attribute measurement of buried package features. Proceedings of the 22nd Electronics Packaging Technology Conference (EPTC). IEEE, Singapore, 2020 221–227.
51. Cho DH, Seo SM, Kim JB, Rajendran SH, Jung JP. A review on the fabrication and reliability of three-dimensional integration technologies for microelectronic packaging: through-si-via and solder bumping process. *Metals*. 2021;11(10):1664.
52. Guan Y, Ma S, Zeng Q, Chen J, Jin Y. Fabrication and characterization of annular copper through-silicon via for passive interposer applications. *IEEE Trans Semiconduct Manuf*. 2018;31(2):270.
53. Schindelin J, Arganda-Carreras I, Frise E, et al. Fiji: an open-source platform for biological-image analysis. *Nat Methods*. 2012;9(7):676.
54. Jiang H, Lu N, Yao L. A high-fidelity haze removal method based on hot for visible remote sensing images. *Remote Sens*. 2016;8(10):844.
55. Barrett JF, Keat N. Artifacts in CT: recognition and avoidance. *Radiographics*. 2004;24(6):1679.
56. Boas FE, Fleischmann D. CT artifacts: causes and reduction techniques. *Imaging Med*. 2012;4(2):229.
57. Marzahl C, Aubreville M, Bertram CA, et al. EXACT: a collaboration toolset for algorithm-aided annotation of images with annotation version control. *Sci Rep*. 2021;11(1):1.
58. Lin TY, Dollár P, Girshick R, He K, Hariharan B, Belongie S. Feature pyramid networks for object detection. Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition (CVPR); 2017:2117-2125; Honolulu, HI.
59. Kingma DP, Ba J. Adam: a method for stochastic optimization; 2014. (Preprint) arXiv:1412.6980.

SUPPORTING INFORMATION

Additional supporting information may be found online in the Supporting Information section at the end of this article.

How to cite this article: Wolz BC, Jaremenko C, Vollnhals F, Kling L, Wrege J, Christiansen S. X-ray microscopy and automatic detection of defects in through silicon vias in three-dimensional integrated circuits. *Engineering Reports*. 2022;4(12):e12520. doi: 10.1002/eng2.12520